5.5 GHz Low Voltage and High Linearity RF CMOS Mixer Design

Senhg-Feng Lu[1] and Jyh-Chyurn Guo[2]

Institute of Electronics, National Chiao-Tung University, 1001 Ta-Hsueh Rd, Hsinchu, Taiwan, R.O.C.

[1]sflu@seed.net.tw

[2]jcguo@mail.nctu.edu.tw

***Abstract*—A CMOS mixer was design with a new circuit scheme to realize low voltage and high linearity simultaneously. A double balanced Gilbert cell was adopted as the basic topology and TSMC 0.18μm 1P6M CMOS process was employed for the on-chip RF circuit fabrication. The proposed new circuit scheme consists of LC-tanks as a capacitively coupled resonator for low voltage and multi-stage parallel RC networks for linearity improvement. Furthermore, multi-gated structure is applied at the RF input as a transconductance amplifier to enhance conversion gain and linearity. The new circuit scheme enables a successful low voltage operation at 1-V for 0.18μm technology. The measured circuit performance demonstrates superior linearity with IIP3 of 11 dBm and P_{1dB} of 2.2 dBm. The conversion gain can be maintained at 8.1 dB in a wide frequencies of 5GHz to 6.8GHz.**

I. Introduction

Mixer is one of the most important elements in RF front-end constituting the modern communication system. The well known Gilbert cell as shown in Fig.1 is the most generally used mixer architecture due to its advantages in port-to-port isolation and spurious output rejection. However, the traditional Gilbert cell mixers generally suffer a limitation in voltage scaling due to the cascade structure with three stacked transistors in series with a resistor. To realize low voltage operation, capacitively coupled resonating elements, e.g. LC tanks were proposed and demonstrated with the applications in RF circuits [1]. However, poor linearity featured by low IIP3 (-6dBm) appears as a critical weakness and demands a significant improvement. In this paper, a new circuit scheme adopting multi-stage parallel RC networks is proposed and implemented to achieve superior linearity.

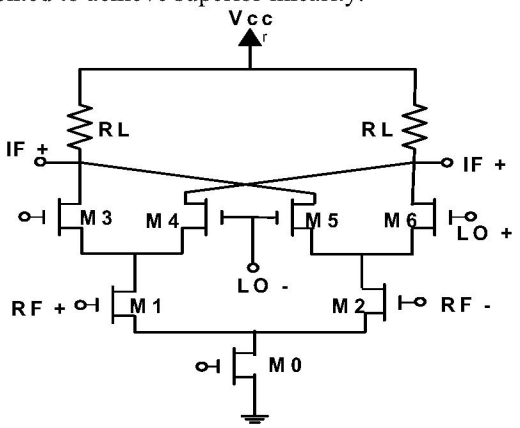

Fig. 1 CMOS Gilbert Cell mixer architecture

II. Circuit Design Principle

A 5.5 GHz down-conversion mixer aimed for high linearity at very low voltage to 1-V was designed with a new circuit scheme. The full circuit is composed of eight circuit blocks as shown in Fig.2. They are arranged with three on-chip and five off-chip elements, respectively. The three on-chip elements incorporate a pair of multiple-gate RF amplifiers [2], local switches (LO), and load IF circuits, denoted by the solid-line box. The off-chip circuits represented by dash-line box cover five elements, such as parallel LC-tanks, bypass capacitors, RF baluns, LO baluns, and a measuring circuit. QFN package is adopted to integrate the on-chip and off-chip circuits together. Fig. 3 displays the full circuit schematics in which the circuit topology corresponding to each functional block in Fig.2 is clearly defined.

To realize a low voltage design, capacitively coupled LC tanks first proposed by Manku et al. [1] are employed in this down-conversion mixer design. As shown in Fig.3, a pair of LC tanks are deployed at drain terminal of RF transconductance stage for 1-V supply voltage. One more pair of LC tanks are allocated at the source terminal of LO switches and ended to the ground. Ideally for inductors free from series resistances, the LC tanks can enable a short path at DC and an open path at resonance. In practice, the existence of series resistances in general inductors leads to a very low impedance at DC state whereas a very high impedance under RF operation. In this way, the DC voltage drop across the stacked structure with RF and LO stages in Fig.3 can be reduced to nearly a single stage to minimize the power dissipation. As for RF operation at resonance, the LC-tanks becomes a nearly open path and the bypass capacitor can pass the RF signal across RF and LO stages.

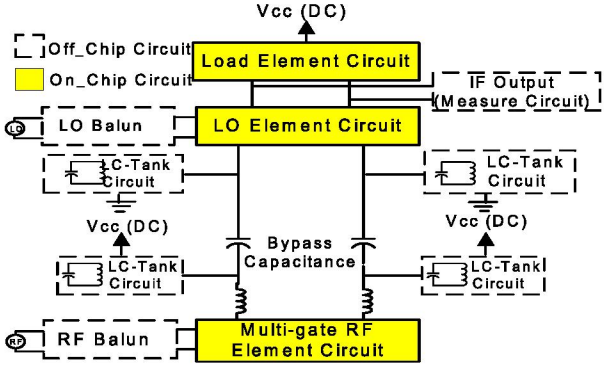

Fig. 2 CMOS RF mixer circuit block diagram

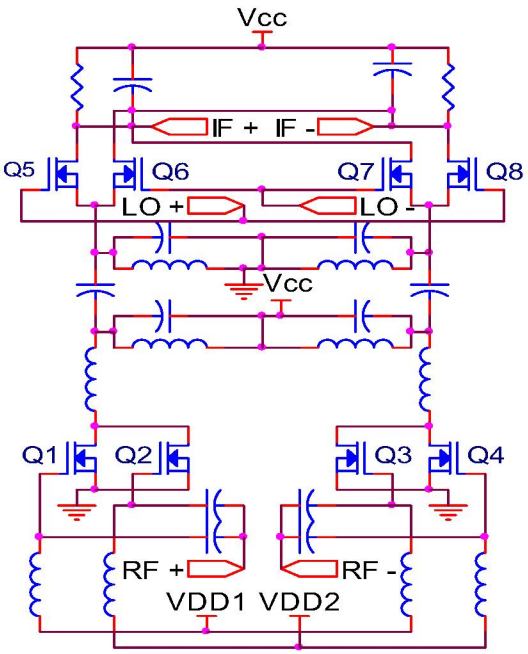

Fig. 3 The circuit schematics of a double balanced RF CMOS mixer with RF stage, LO switches, LO bias, IF load, LC-tanks, bypass capacitor, and baluns

Regarding a major target for high linearity, multi-gate transistors [2] were designed in the RF transconductance amplifiers for verification. The third-order nonlinear term cancellation realized by gate bias tuning on the multi-gated structure can help improve linearity. Besides, a new design with multi-stage parallel RC networks was implemented at the IF output to further enhance linearity. Simulation as shown in Fig.4 indicates that the multi-stage parallel RC networks adopted at IF stage, acting as a high-pass filter can effectively suppress the higher order harmonic components and push out the third order intercept point. Through this mechanism, the linearity defined by IIP3 can be significantly improved. As to design for higher conversion gain (CG), inductive degeneration was implemented by an on-chip inductor at RF output [3]. Note that an inductor of 3.799 nH was used in this design to optimize the output matching and improve CG.

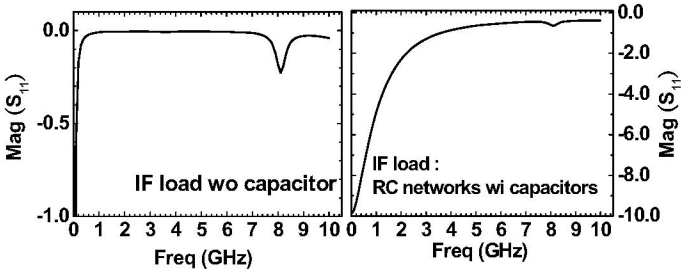

Fig 4 (a) IF stage with simple resistor network without capacitor (b) IF stage with parallel RC networks – the parallerl RC serves as a high-pass filter to effectively filter out higher order harmonics and improve lineariy

Eventually, the full circuit has to be mounted on PCB for measurement. The critical points to be considered are the parasitic inductance and resistance existing with the bond wires and the parasitic capacitance originated from the bonding pads. Fig. 5 presents the bond-wire package model. The series inductance is approximately 1nH/mm. For a bond wire with a length generally exceeding that of the on-chip inductor, it will impose a significant influence on the circuit performance. Due to the fact, the package model of bond-wire must be taken into account in the full circuit simulation. Fig. 6 illustrates the chip layout of the double balanced CMOS mixer in this design and Fig.7 specifies the pin assignment for bonding pads on board .

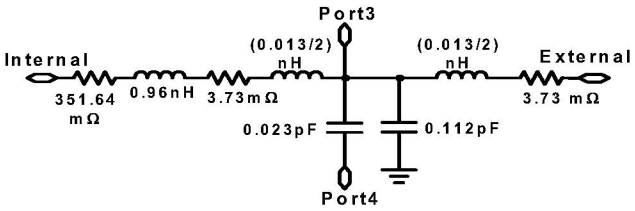

Fig. 5 A package model for the bonding wires and pads

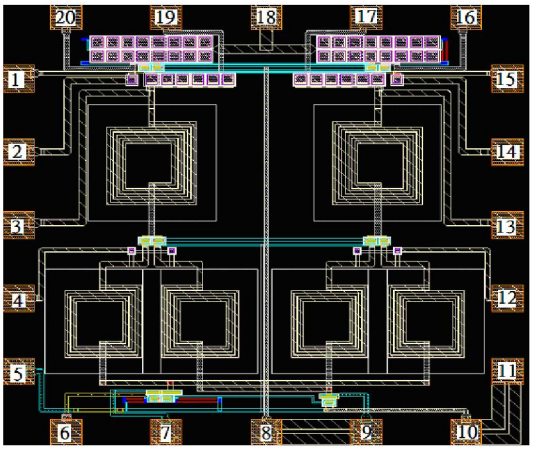

Fig. 6 Chip layout of a double balanced Gilbert mixer

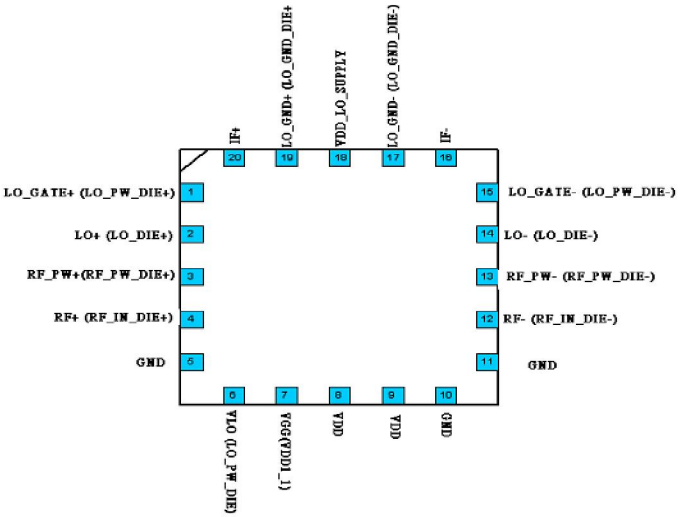

Fig. 7 Pin assignment for mixer chip on board bonding pads

III. Results and Discussion

A. *Simulation Results*

0.18um MOSFET model was employed for on-Si-chip circuit simulation and SPIL QFN package model was

integrated with core MOSFET model for a full circuit simulation. Fig.8(a) and (b) present the CG, P_{1dB}, and IIP3 under varying RF power, simulated using SS corner model, under 1-V and 25°C operation. Table 1 summarizes the full circuit simulation results using typical and corner models (TT, SS, FF) for MOSFETs as well as QFN package model for bonding wires and pads. The operation condition for the low voltage mixer is a supply voltage at 1-V and temperature at 25°C. The key performance parameters include conversion gain (CG), gain compression (P_{1dB}), the third-order intercept point (IIP3), and power consumption.

The simulation predicted a good performance of high CG, high linearity, and low power consumption. The power consumption at 1-V can be push to 2~3.7mW. The high linearity is featured by IIP3 of 8.2~12 dBm and 1dB output power compression (OP_{1dB}) of 4.89~6.22 dBm. CG can achieve 18.7~24.2. The high linearity is realized through the multi-stage RC networks at IF load.

TABLE I
Simulation results for a mixer on QFN chip operating under 1.0V and 25 °C
(TT : Typical, SS : Slow, FF : Fast)

Performance Parameters	SS	TT	FF
Conversion Gain (dB)	18.7	24.2	19.8
OP_{1dB} (dBm)	6.22	5.8	4.89
IIP3 (dBm)	12	10	8.2
Power Consumption (mW)	2.03	2.74	3.71
RF/LO : 5.5/5.499GHz, LO power : 2.5 dBm			

B. *Measurement Results*

The measured P_{1dB} and IIP3 are demonstrated in Fig. 9(a) and (b). The superior linearity with IIP3 of 11 dBm and P_{1dB} of 2.2 dBm proves the success of harmonic suppression through the high-pass filter realized by multi-stage parallel RC networks at IF load. IIP3 as high as 11 dBm at LO power of 2.5dBm matches very well with the simulation result of 12 dBm shown in Table 1. Fig. 10 (a) and (b) present the measured CG vs. input power and RF frequency in which CG above 8.1 dB can be maintained over a wide range of input power to 0dBm and frequencies in 5~6.8GHz. The degradation compared with simulation suggests a deviation from the desired optimal matching incorporating the circuit elements on PCB, such as LC tanks and balun. Improvement can be achieved by an extensive calibration on the package model and that for on-board circuit elements. Table 2 summarizes the measured performance parameters, such as CG, P_{1dB}, IIP3, and power consumption. The measured power consumption appears higher than simulation prediction. Process variation induced drift in resistances and IR drop is considered a potential reason responsible for the increased DC power. Fortunately, the power consumption keeps low at around 4 mW attributed to the sufficiently low voltage to 1.0V.

TABLE 2
Measurement Results under supply voltage at 1.0V, Temp = 25°C

Performance Parameters	Measured Results
Conversion Gain	8.1 dB @0dBm
P_{1dB}	2.2 dBm
IIP3	11 dBm
Power Consumption	4.1mW
RF/LO : 5.501/5.5GHz, LO power : 2.5 dBm	

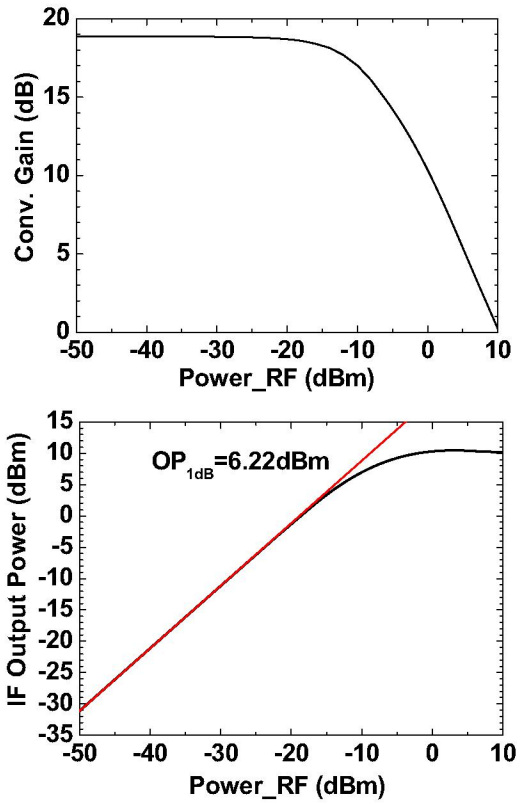

Fig. 8 (a) Simulated conversion gain and IIP3 under 1.0V and 25°, SS corner model was used for simulation

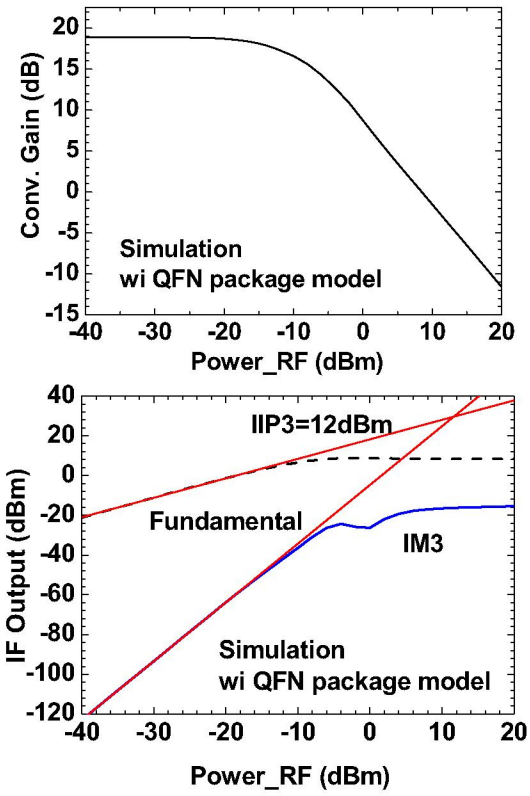

Fig. 8 (b) Simulated conversion gain and IIP3 under 1.0V and 25°C. SS corner model for MOSFET and QFN package model for bonding wires and pads were adopted for the full circuit simulation.

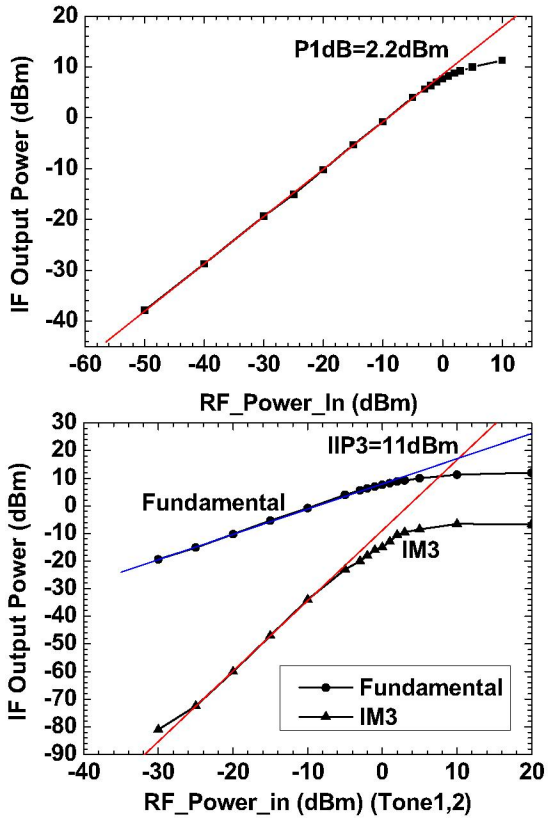

Fig. 9 Measured linearity (a) P-1dB and (b) IIP3

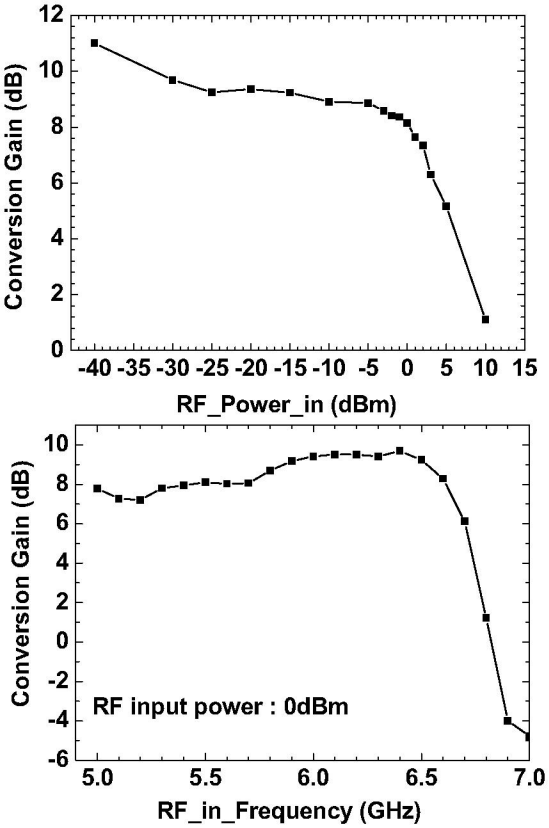

Fig. 10 (a) Measured conversion gain vs. RF input power
(b) Measured conversion gain vs. RF input frequency

IV. Conclusion

A 5.5 GHz down-conversion mixer has been fabricated in 0.18 um RF CMOS technology. The new circuit scheme enables a successful low voltage operation at 1.0V and low power consumption of around 4mW. This low voltage mixer demonstrates superior linearity with IIP3 of 11 dBm and P_{1dB} of 2.2 dBm. The conversion gain can be maintained at 8.1 dB over a broadband operation in 5GHz to 6.8 GHz.

The superior linearity in terms of high IIP3 and P_{1dB} proves the advantage realized by mutli-stage parallel RC networks at IF output. The success of low voltage operation validates a new design adopting LC-tanks at RF and LO stages. The major challenge remained with this work is a certain deviation between the whole chip simulation and measurement result. It is because that simulation accuracy is acceptable for on chip balun and LC tank design; however, a fully qualified simulation tool is lacking for balun and LC tank design, which is on PCB through the method of SMD. The PCB layout can be improved by considering the characteristic wavelength of microstrip lines. Regarding balun circuit design, a replacement of conventional design using passive components by active components [4,5] can further improve the circuit performance and reduce the chip area.

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