92% High Efficiency and Low Current Mismatch Interleaving Power Factor Correction Controller With Variable Sampling Slope and Automatic Loading Detection Techniques

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***Abstract*—This paper proposes the dual nondeadtime variable sampling slope technique to carry out precise phase sensing and suppress phase error in interleaving power factor correction (PFC) controller over a whole ac switching cycle for low current mismatch. Furthermore, the proposed automatic loading detection (ALD) technique can keep efficiency higher than 92% over a wide load range due to accurately controlling the ON/OFF of dual phases. The test circuit fabricated in the TSMC 0.5-μm 800-V UHV process shows that the highly integrated interleaving PFC can deliver a high power of 180 W and a high efficiency of 95% at an output power of 180 W.**

***Index Terms*—Automatic loading detection (ALD), dual nondeadtime variable sampling slope (DNVSS), interleaving power factor correction (PFC).**

I. Introduction

In today's power consumer markets, portable electronics should be designed with the advantages of small volume and light weight. Meanwhile, enhancing efficiency and minimizing power loss are important topics for consumer applications. Unfortunately, the power module in portable electronics, including adapter and the portable mobile power, occupies large volume and has heavy weight as depicted in Fig. 1. To reduce volume and weight of the power module, the interleaving power factor correction (PFC) with the boundary control mode (BCM) technique as depicted in Fig. 2 is utilized to get the advantages of compact size, high energy utilization, and high power conversion efficiency at the same time for green power requirement [1]–[11]. With the help of PFC, the ac line voltage and current can be in phase to improve the energy utilization. On the other hand, the interleaving technique can reduce the external pass components and keep high efficiency over a wide load range by changing the number of phases according to the output loading condition.

The conventional interleaving PFC controller in Fig. 2 uses one error amplifier (EA) to set up the output power level through

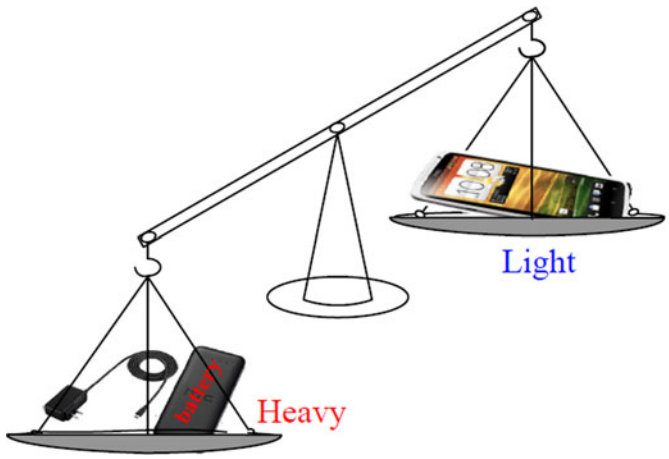

Fig. 1. Large volume and heavy weight of the power module compared to portable electronics.

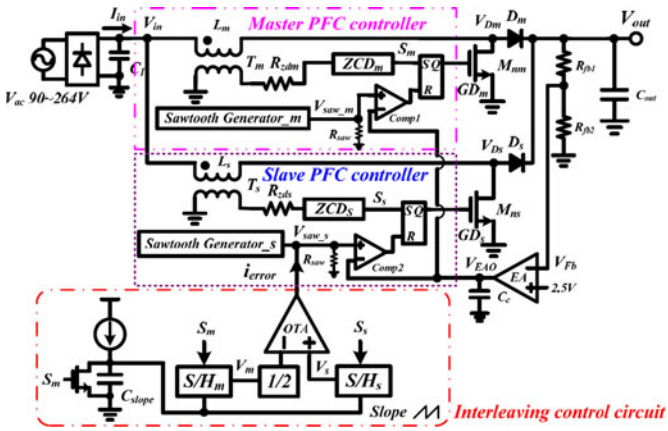

Fig. 2. Conventional interleaving PFC with the BCM control.

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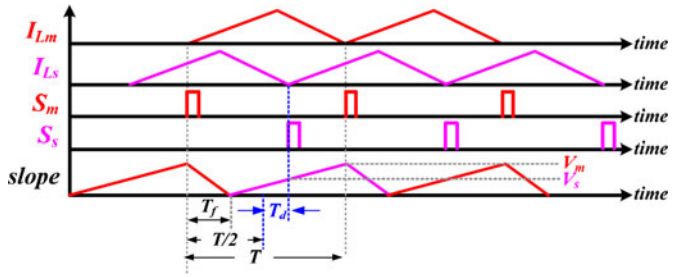

Fig. 3. Timing diagrams of the conventional interleaving control circuit in the PFC scheme.

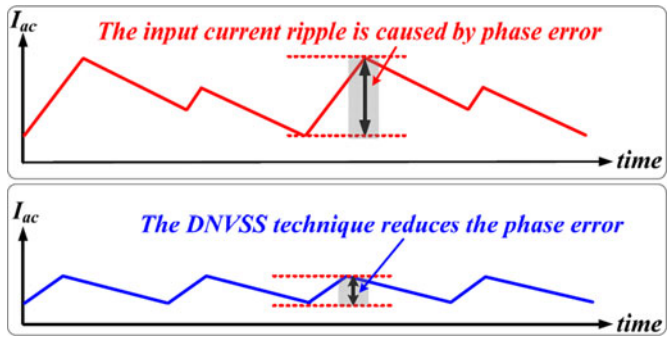

Fig. 4. Improved input current ripple with DNVSS technique.

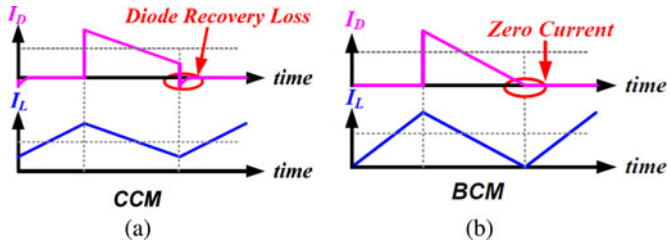

Fig. 5. Inductor and the diode currents in (a) CCM and (b) BCM.

the on-time period, which is determined by the comparison result of the error signal $V_{\rm EAO}$ and the sawtooth signal [12]–[18]. In the BCM control, the off-time period is determined by the detection of zero inductor current (ZCD) [19]. That is to say, the power N-type MOSFET is periodically turned ON by the zero current switching (ZCS) mechanism. The advantage is the reduction of switching power loss because power loss caused by the diode reverse recovery can be effectively eliminated. Therefore, an accurate ZCD circuit is needed in the ZCS mechanism for high efficiency.

On the other hand, to achieve the interleaving control, the sawtooth signal *slope* is used to convert the phase error between two phases to the voltage difference. Then, the phase error in voltage domain will be transferred to the error current signal $i_{\rm error}$ by an operational transconductance amplifier (OTA). $i_{\rm error}$ flowing through the resistor $R_{\rm saw}$ can easily pull up or down the dc level of sawtooth signal $V_{\rm saw_s}$ in the slave phase by ΔV so as to adjust the phase shift between the master and slave phases.

Ideally, due to negative feedback control, the sampling voltage of master phase V_m should be twice that of the slave phase V_s in steady state. However, the falling time T_f of $C_{\rm slope}$ in the conventional interleaving control circuit is not equal to zero because only one sawtooth generator is used in Fig. 2. Consequently, an undesired time delay T_d induces an incorrect starting time in the slave phase as shown in Fig. 3. In other words, the phase shift between the slave phase and the master phase is T_d larger than half switching period, which is an ideal and desired value that can fairly control each phase. Without fairly controlling each phase, the advantage of input current ripple cancellation contributed by the interleaving control will disappear owing to the existence of T_d. Therefore, the phase control of the slave phase needs to account the effect of T_d for improving the accuracy of phase sensing and equally controlling energy from each phase.

The input current ripple is enlarged to show the effect of T_d in Fig. 4. With a larger value of T_d, the input inductor needs to be larger to restrict the input current ripple for system specification. Thus, T_d should be small enough to decrease the input current ripple. To further improve the input current ripple, the DNVSS technique is utilized in this paper. The DNVSS technique not only decreases the value of T_d automatically but also reduces the input current ripple as shown in Fig. 4. Consequently, small input inductor can be used because the input current ripple can be restricted by the proposed DNVSS technique.

Moreover, the PFC system utilizes the boost topology for continuous input current that can be manipulated with average current mode control techniques to force input current to track changes in ac voltage. Besides, compared to the continuous conduction mode (CCM), the benefit of the BCM is the reduced reversed-recovery losses caused by the boost diode as shown in Fig. 5. Thus, the efficiency can be enhanced at light-load states. The efficiency is defined as the ratio of output power $P_{\rm out}$ to input power $P_{\rm in}$ as expressed in (1). $P_{\rm loss}$ is the sum of power loss as expressed in (2). $P_{\rm con}$ and $P_{\rm sw}$ are the conduction and switching losses, respectively. $P_{\rm sys}$ is the power loss in the controller composed of analog and digital circuits

$$\eta = \frac{P_{\rm out}}{P_{\rm in}} = \frac{P_{\rm out}}{P_{\rm out} + P_{\rm loss}}, \text{ where } P_{\rm in} = P_{\rm out} + P_{\rm loss} \quad (1)$$

$$P_{\rm loss} = P_{\rm con} + P_{\rm sw} + P_{\rm sys}. \quad (2)$$

The conventional interleaving PFC has high efficiency at heavy loads but low efficiency when load drastically decreases. Especially, the switching power loss dominates the total power loss when the system enters the standby mode. As we know, the standby power efficiency is one of the important concerns. Besides, because of the variable frequency in the BCM control, switching loss increases seriously and the efficiency drastically decreases from heavy to light load. Therefore, the design of the interleaving PFC controller needs to effectively reduce the switching loss at the light loads for power saving. In other words, the number of the phases should be adaptively controlled to save much power loss at light loads. In this paper, the DNVSS techniques are proposed to get precise phase shift for better ripple cancellation. Thus, small external EMI filter, small size input inductor, and restrained current mismatch can be guaranteed. Besides, the automatic loading detection (ALD) is proposed to control the number of the phases for enhancing conversion efficiency over a wide output power range.

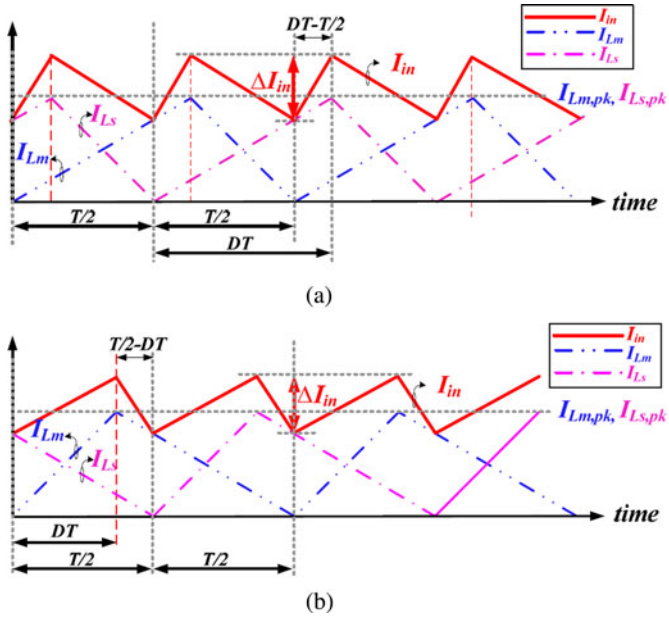

Fig. 6. Inductor current waveform of the interleaving BCM controller (a) when $D > 0.5$ and (b) when $D < 0.5$.

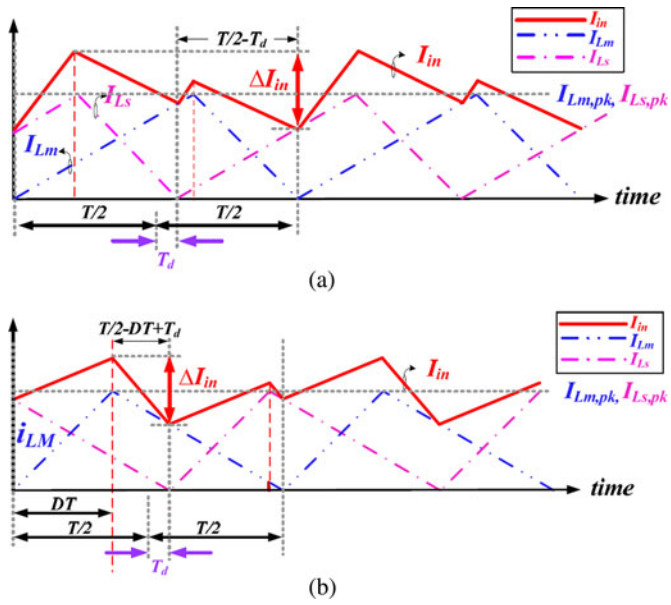

Fig. 7. Conventional interleaving with time delay T_d (a) when $D > 0.5$ and (b) when $D < 0.5$.

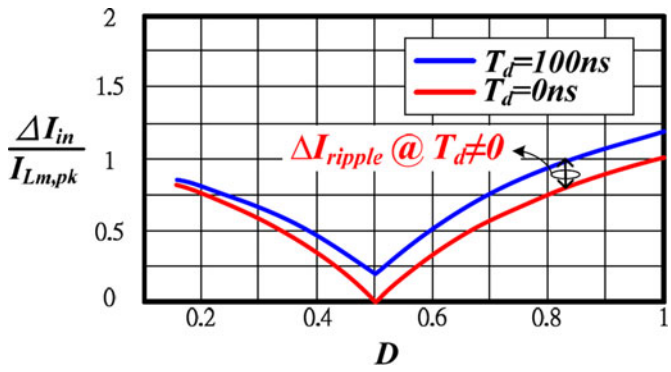

Fig. 8. Ratio of the input current ripple to inductor current ripple with different duty and T_d.

The organization of this paper is as follows. Section II introduces the design concept based on the phase error and the efficiency. Section III introduces the proposed interleaving PFC controller with the DNVSS and ALD techniques. The circuit implementation is shown in Section IV. Experiment results shown in Section V can prove the advantages of the proposed PFC with the DNVSS and the ALD techniques. Finally, conclusions are made in Section VI.

II. Design Concept Based on the Phase Error and the Efficiency

A. Phase Error

Fig. 6(a) and (b) shows the operation of ideal inductor current ripple cancellation when the duty is >50% and <50%, respectively. The input current ripple can be reduced effectively and the ratio of input current to the inductor current can be shown in the following equation, when $D > 0.5$:

$$\frac{\Delta I_{\text{in}}}{I_{Lm,pk}} = \frac{2D-1}{D}. \tag{3}$$

Contrarily, as $D < 0.5$, the ratio of input current to the inductor current is shown in

$$\frac{\Delta I_{\text{in}}}{I_{Lm,pk}} = \frac{1-2D}{1-D}. \tag{4}$$

According to the derivations of (3) and (4), a well-designed interleaving PFC system can ensure effectively reduced input current ripple. Thus, the advantage is that the output capacitor size can be reduced.

However, the ripple cancellation contributed by the interleaving control will be deteriorated by T_d as illustrated in Fig. 7. In the conventional architecture as shown in Fig. 2, C_{slope} is charged to generate the sawtooth signal *slope*, which can sample the phase shift. However, the discharging time T_f that is needed for the next phase sampling cycle changes the charging period of C_{slope} from "T" to "$T - T_f$" as illustrated in Fig. 3. Besides, because of the negative feedback loop, S_s is adjusted to raise at the middle of charging period of C_{slope} so that V_s is half of V_m. As a result, an exact phase shift T_d can be produced. As $D > 0.5$, the line current ripple is increased to the value as shown in

$$\frac{\Delta I_{\text{in}}}{I_{Lm,pk}} = \frac{2D-1+(2T_d/T)}{D}, \text{ where } D > 0.5. \tag{5}$$

Similarly, the ratio of input current to the inductor current is shown in the following equation, if D is smaller than 0.5:

$$\frac{\Delta I_{\text{in}}}{I_{Lm,pk}} = \frac{1-2D+(2T_d/T)}{1-D}, \text{ where } D < 0.5. \tag{6}$$

Therefore, Fig. 8 can describe how the ratio of input current ripple to the inductor current ripple varies with the change in duty cycle under different phase error T_d. If T_d is neglected,

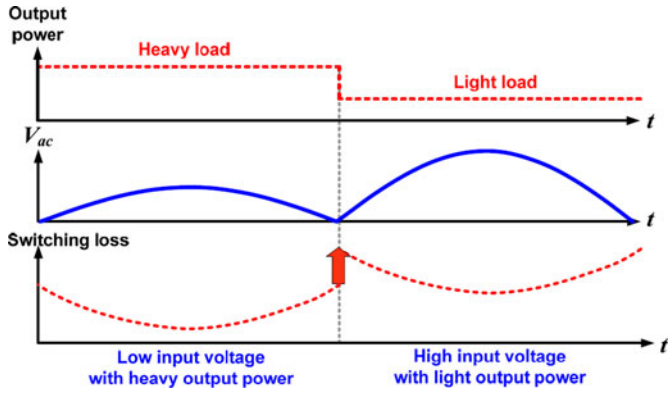

Fig. 9. Operation frequency of the conventional interleaving PFC.

$\Delta I_{\rm in}/I_{Lm,pk}$ can be viewed as an ideal value. As the value of T_d increases, $\Delta I_{\rm in}/I_{Lm,pk}$ is increased about $\Delta I_{\rm ripple}$. The performance of the interleaving PFC becomes worse than that under ideal condition. In conclusion, small phase error can decrease $\Delta I_{\rm in}/I_{Lm,pk}$.

Here, the DNVSS technique is proposed to get precise phase shift for better ripple cancellation in an interleaving PFC system. Thus, the time delay T_d can be effectively restricted to a small value. Meanwhile, small external EMI filter and restrained current mismatch can be guaranteed.

B. Efficiency Issue

The conventional interleaving PFC controller with the BCM control can effectively supply large output power. However, the major drawback is the efficiency problem at light loads. The switching frequency varies widely with the line voltage and the output power in the BCM control. Thus, switching power loss increases seriously and the efficiency drastically decreases if the load changes from heavy to light. Especially at high line voltage and light-load condition, high switching power loss results in obvious efficiency decrease as shown in Fig. 9, which shows that the efficiency gradually decreases due to the switching power loss when the output power changes from heavy to light. Thus, the deteriorated efficiency at light loads needs to be improved.

To achieve high conversion efficiency, the interleaving PFC controller needs to turn OFF the slave channel automatically at light loads for avoiding high switching frequency. However, the output voltage of the error amplifier $V_{\rm EAO}$, which is usually used to indicate the load condition in conventional dc–dc converters, cannot be used as a loading indication signal [20], [21]. The reason is that both output power and line voltage will affect the value of $V_{\rm EAO}$ in the ac–dc converters.

For example, as depicted in Fig. 10, if $V_{\rm EAO}$ is selected as the transition point to decide single- or dual-phase operation, the transition power for different line voltages will also be different. Here, 90 $V_{\rm ac}$ will transit at point A of 90 W while 264 $V_{\rm ac}$ will transit at point B of 180 W, which is too high for the PFC system without any power saving advantage. Therefore, the ALD technique is proposed to accurately decide the transition power at a universal input ac voltage for enhancing conversion efficiency. Switching power loss and power conversion efficiency at light loads can be effectively improved. Fig. 11 illustrates the efficiency of a conventional interleaving PFC architecture. Therefore, after the implementation of the proposed ALD technique, which can accurately switch the operation from the interleaving to single phase at light loads in the interleaving PFC system, the performance of efficiency and EMI effect can be greatly improved.

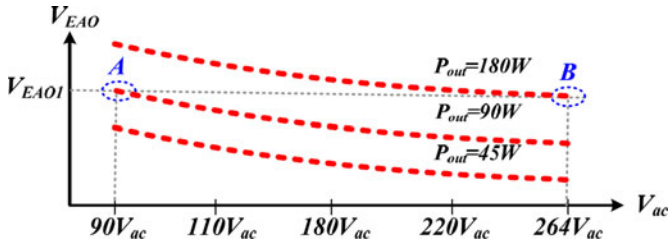

Fig. 10. Output power information between $V_{\rm EAO}$ and $V_{\rm ac}$.

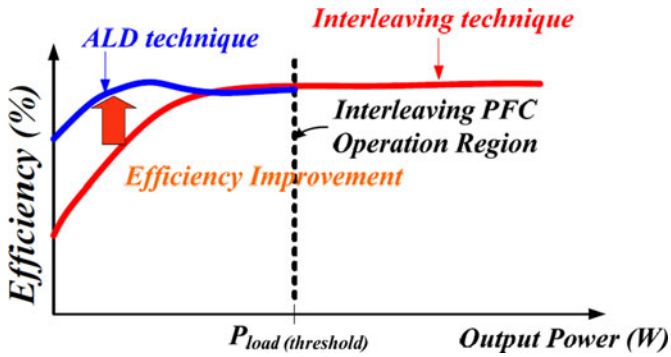

Fig. 11. Proposed interleaving PFC controller with the ALD technique.

III. Proposed Interleaving PFC Controller With the DNVSS and the ALD Techniques

Fig. 12 illustrates that $i_{\rm error}$ pulls up or down the dc level of the sawtooth signal $V_{\rm saw_s}$ in the slave phase according to the value of ΔV. In Fig. 12(a), if the phase difference between two phases is less than 180°, $V_{\rm saw_s}$ is pulled down about ΔV so that the on-time period of the slave phase power MOSFET M_{ns} can be extended. Contrarily, $V_{\rm saw_s}$ is pulled up by ΔV to shorten the on-time period as depicted in Fig. 12(b) [22]–[28].

Therefore, a negative feedback loop is needed to ensure the phase correction within one switch cycle as long as the amount of revised phase Δt_r, as expressed in (7), is equal to the phase error Δt

$$\Delta t_r = \Delta t \cdot S_{\rm slope} \cdot g_m \cdot R_{\rm saw} \cdot \frac{1}{S_{\rm saw\_s}} \cdot \frac{V_{\rm out}}{V_{\rm out} - V_{\rm in}} \qquad (7)$$

where g_m is the transconductance of the OTA. $S_{\rm slope}$ and the $S_{\rm saw_s}$ are the slopes of the sampling slope, *slope*, and the slave sawtooth signal, $V_{\rm saw_s}$, respectively.

A. Proposed DNVSS Technique

In order to realize precise phase correction, Δt_r is required to be close to Δt. Hence, the condition determined in the following

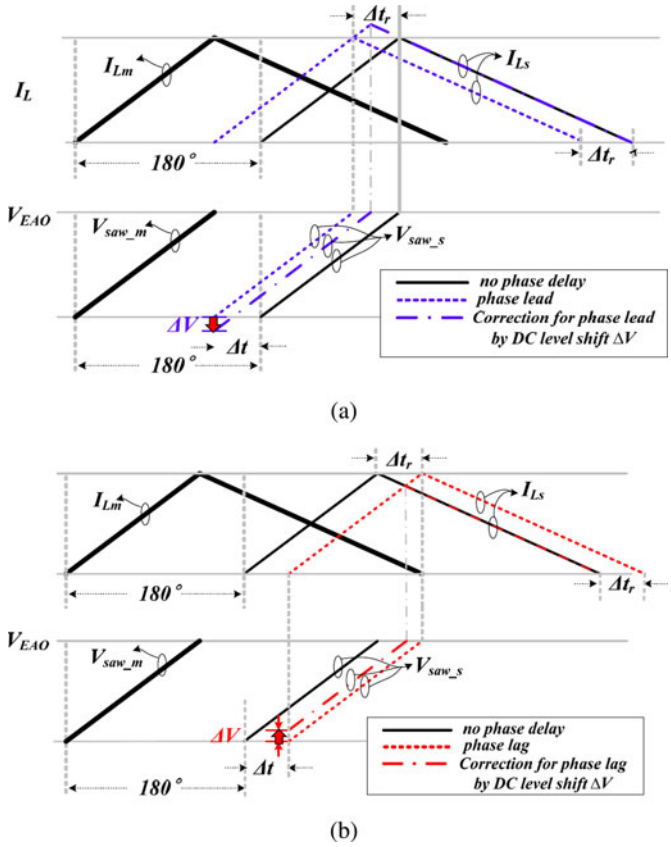

Fig. 12. Corrected interleaving scheme. (a) Correction by the dc level shift ΔV for phase lead. (b) Correction by the dc level shift ΔV for phase lag.

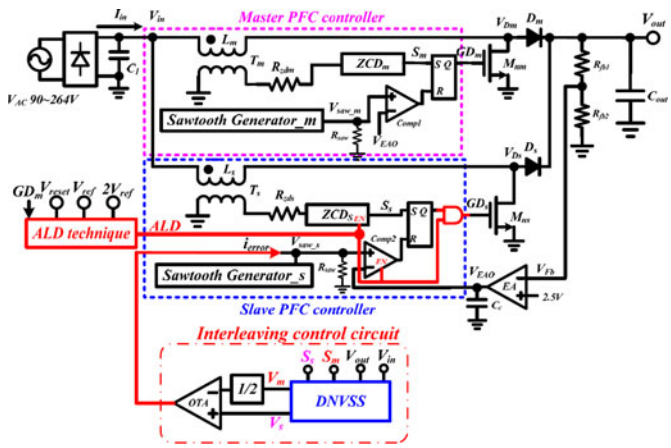

Fig. 13. Proposed interleaving circuit contains the DNVSS and ALD techniques.

equation must be satisfied:

$$S_{\text{slope}} \cdot g_m \cdot R_{\text{saw}} \cdot \frac{1}{S_{\text{saw\_s}}} \cdot \frac{V_{\text{out}}}{V_{\text{out}} - V_{\text{in}}} \approx 1. \qquad (8)$$

However, the term of $V_{\text{out}}/(V_{\text{out}} - V_{\text{in}})$ varies with the ac line voltage. That is, it is hard to satisfy the requirement of (8) for the whole ac switching cycle. Thus, the proposed interleaving PFC controller with the DNVSS technique as depicted in Fig. 13 produces two interleaving ramp signals that can be proportional to the value of "V_{out} –V_{in}" to alleviate the effect of the variation

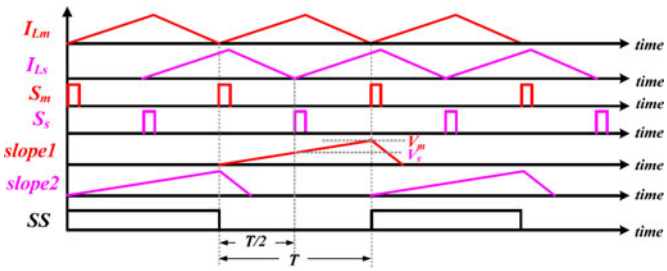

Fig. 14. Interleaving scheme with the proposed DNVSS technique.

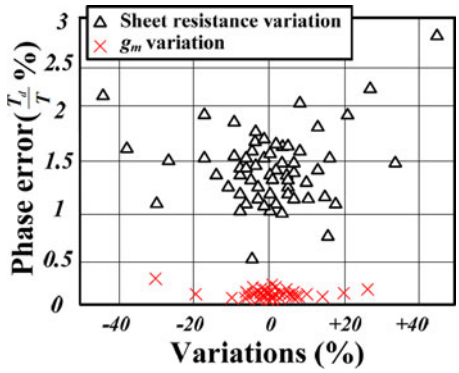

Fig. 15. Monte Carlo analysis of the variation of resistance R_{saw} and the transconductance of the OTA g_m.

at V_{in}. Consequently, it forces that (8) can be guaranteed for the whole ac switching cycle. In other words, it can ensure that Δt_r is close to Δt.

To solve nonideal effect of T_f as shown in Fig. 3, as illustrated in Fig. 14, the DNVSS generates two interleaving ramp signals *slope1* and *slope2* alternatively to let T_f no longer influence the sampling voltages V_m and V_s. Thus, the phase shift between two phases can be precisely sensed without the effect of T_f at C_{slope}. Two inductor currents I_{Lm} and I_{Ls} have 180° phase difference for each other. The slope-selection signal *SS*, which is synchronous to the master sampling signal S_m, can select one of *slope1* and *slope2* to convert the time difference to voltage difference for achieving high-performance interleaving operation.

However, inevitably process variation in R_{saw} and g_m can be larger than 40% and 30%, respectively, to affect the precision on the implementation of (8). Fortunately, the operational transconductance amplifier OTA in Fig. 13 helps suppress the influence caused by mismatches of R_{saw}, g_m and the NDVSS circuit. The phase error between the master and the slave is analyzed by Monte Carlo analysis as shown in Fig. 15. T is the switching period and T_d represents the time delay deviating from $T/2$ of the master as illustrated in Fig. 7. During large sheet resistance variation of R_{saw}, the phase error can be kept under 3% by the NDVSS technique. Furthermore, the variation of g_m can be suppressed under 0.5%.

B. Proposed ALD Technique

The architecture of the proposed interleaving PFC controller with ALD technique is shown in Fig. 13. The controller can

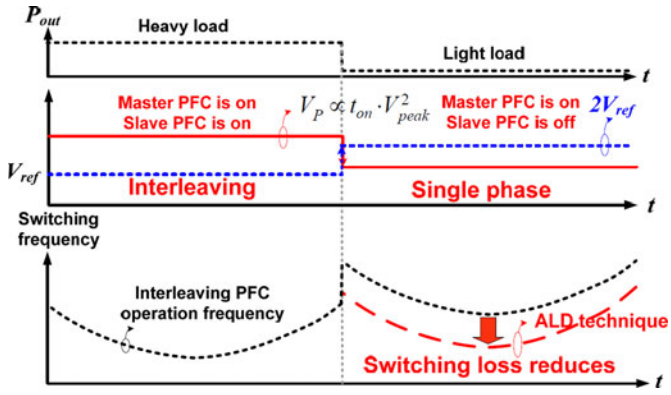

Fig. 16. Operation frequency with the ALD technique.

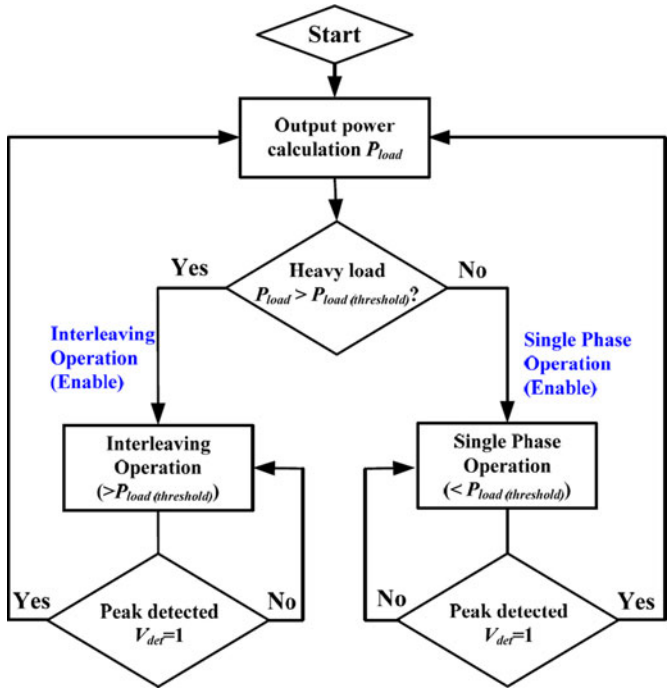

Fig. 17. Flowchart of the ALD technique.

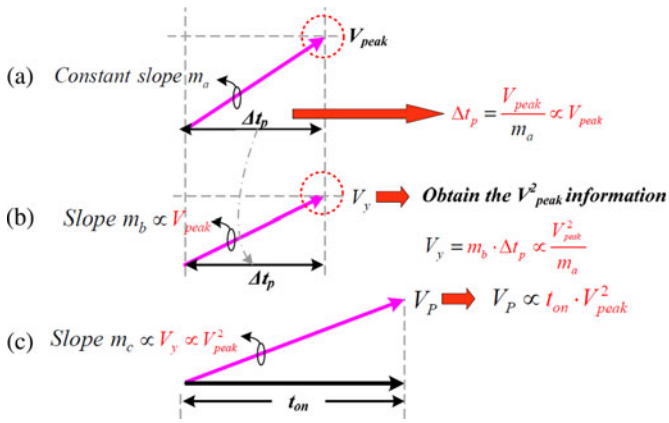

Fig. 18. Process flow of the ALD technique.

be divided into two different operations. The primary operation guarantees that the system operates normally with the interleaving controller. The secondary operation forces the system operates with the master PFC controller which can raise the efficiency at light loads as shown in Fig. 11. The efficiency is improved due to the decrease of the switching frequency and switching power loss as shown in Fig. 16. The expression of the output power information can be described as $P_o = \frac{t_{\rm on} \cdot V_{\rm peak}^2 \cdot \eta}{4 \cdot L_p}$.

Here, L_p is the primary inductor and $V_{\rm peak}$ is the peak value of the line voltage. η is the efficiency and P_o is the output power. In steady state, the output power information can be simply obtained by line voltage and on-time value because L_p and η are kept constant. Thus, the output power information can be represented by V_p as shown in the following equation, which is used to compare with $V_{\rm ref}$ to decide when the slave phase should be turned OFF:

$$V_P \propto t_{\rm on} \cdot V_{\rm peak}^2. \tag{10}$$

However, when the slave phase is turned OFF, the whole output load is supplied by the master phase, Thus, the current (or $t_{\rm on}$) in the master phase becomes twice that in the interleaving operation. Therefore, the reference voltage should be changed from $V_{\rm ref}$ to $2V_{\rm ref}$ as illustrated in Fig. 16. If the power level V_p in (10) of the interleaving PFC is smaller than the reference, the ALD technique will set the ALD to a low level to turn OFF the slave channel as illustrated in Fig. 16.

The flow diagram of the ALD technique is shown in Fig. 17. Basically, the steady-state operation of a primary modulator is similar to that of the interleaving PFC controller. When the output power is smaller than the threshold output power $P_{\rm load(threshold)}$, the single-phase operation is triggered to turn OFF the slave channel for improving efficiency at light loads. That is, the PFC system will be modulated by the single-phase modulation to reduce switching power loss. Once the output power is pulled back and larger than $P_{\rm load(threshold)}$, the system will automatically switch to the interleaving PFC operation.

For implementing the derivation of (10), Fig. 18 shows the signal generation flow of the power level signal V_p. Fig. 18(a) uses a constant slope m_a to determine the time duration Δt_p in the following equation by the line peak voltage $V_{\rm peak}$:

$$\Delta t_p = \frac{V_{\rm peak}}{m_a}. \tag{11}$$

In Fig. 18(b), using one slope m_b proportional to $V_{\rm peak}$ in (11) integrates the time duration Δt_p to get the reference voltage V_y, which is expressed in the following equation and proportional to the square of the peak line voltage:

$$V_y = m_b \cdot \Delta t_p \propto \frac{V_{\rm peak}^2}{m_a}, \text{ where } m_b \propto V_{\rm peak}. \tag{12}$$

Finally, as depicted in Fig. 18(c), the power level signal V_p, which can decide the transition point between the interleaving and single-phase operation, can be derived by the integration with the slope m_c decided by V_y in (12) for the on-time duration $t_{\rm on}$.

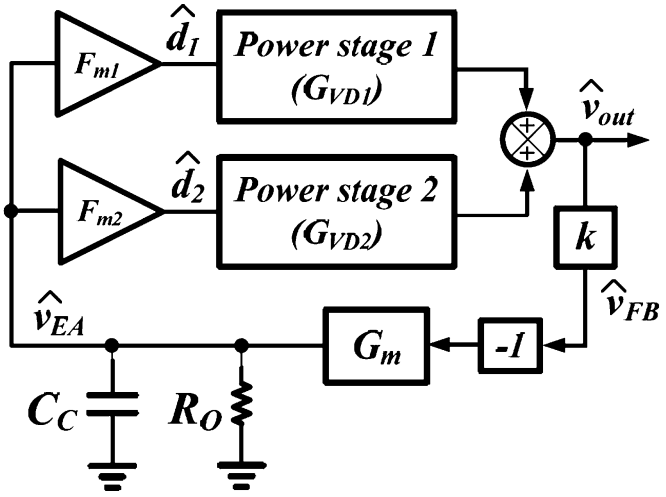

Fig. 19. Small-signal model of the proposed interleaving PFC with DNVSS and ALD techniques.

C. Design Procedure

As shown in Fig. 9, the minimum switching frequency occurs at the peak value of the ac line voltage. To avoid the system operating in the audio band, the minimum frequency has to be carefully designed. According to the law of energy conservation, the inductance formula can be derived as follows:

$$L_b = \frac{V_{\text{peak}}^2 \times (V_{\text{out}} - V_{\text{peak}}) \times \eta}{4 \times P_{\text{out}} \times V_{\text{out}} \times f_{s,\min}} \tag{13}$$

where V_{peak} is the peak value of the input ac voltage, P_{out} is the output power, $f_{s,\min}$ is minimum switching frequency, and η is the conversion efficiency.

Here, the minimum switching frequency $f_{s,\min}$ is defined to be 35 kHz which is higher than the maximum audio frequency 20 kHz. Considering both maximum and minimum input ac line voltages, a 400 μH inductance is chosen and the maximum switching frequency is 255 kHz because the minimum off-time is implemented in the chip for reducing the switching power loss [29].

The output capacitor C_{out} is used to guarantee a well-regulated output voltage for the following dc/dc converter stage. Once the input ac voltage turns OFF, the load current is provided by the energy stored in C_{out}. After a time interval, which is defined as the output voltage hold-up time t_{hold}, the output voltage falls below the minimum operating voltage of the following dc/dc converter stage. To meet the requirement of t_{hold}, C_{out} has to be properly selected. The formula of the output capacitor can be derived as follows:

$$C_{\text{out}} = \frac{2 \times P_{\text{out}} \times t_{\text{hold}}}{V_{\text{out}}^2 - V_{\text{out,min}}^2}. \tag{14}$$

D. System Stability Analysis

The small-signal model of the proposed interleaving PFC with the DNVSS and the ALD techniques is shown in Fig. 19 [29], [32]. Both power stages of the master and the slave are connected to V_{out} for providing high energy. The duty-to-output transfer functions of the master and the slave are G_{VD1} and G_{VD2}, respectively. The output voltage V_{out} is sensed by a voltage divider with the gain of k to obtain the feedback voltage V_{FB} as expressed in (15). The negative feedback loop is controlled by the error amplifier *EA* with the transconductance of G_m and the output resistance of R_o. The capacitor C_C is placed at the output of the error amplifier for frequency compensation. Through comparing V_{EA} with the sawtooth signals, the duty cycles d_1 and d_2 can be modulated to control the power stages. The modulation gains of the master and the slave are F_{m1} and F_{m2}, respectively

$$k = \frac{R_{fb2}}{R_{fb1} + R_{fb2}}. \tag{15}$$

At light loads, the ALD technique turns OFF the slave controller automatically to maintain high efficiency. Therefore, only F_{m1} and G_{VD1} appear in the small-signal model. A large compensation capacitor C_C is designed to suppress the system bandwidth beneath 20 Hz and to prevent 60/120 Hz noise coupled from the ac source to V_{out}. Since the poles and zero at the power stage are much higher than the system bandwidth, the PFC can be viewed as a one-pole system.

At heavy loads, both master and slave PFCs are activated. With the NDVSS technique, the phase error between the master and the slave is minimized and the interleaving operation of the proposed PFC can be assured. Therefore, the control loops of the master and slave are identical with the help of NDVSS. In other words, $F_{m1} = F_{m2} = F_m$ in (16) and $G_{VD1}(s) = G_{VD2}(s) = G_{VD}(s)$ in (17) are derived. Consequently, the proposed interleaving PFC performs a one-pole system with the dominant pole of $\omega p_{(\text{dominant})}$. The closed-loop gain is derived in (18)

$$F_m = \frac{1}{V_M} \tag{16}$$

$$G_{VD}(s) = \frac{V_{\text{out}}}{1-D} \frac{\left(1 - s(L_p/(1-D)^2 R_L)\right)}{1 + s(L_p/R_L)s^2 L_p C_{\text{out}}} \tag{17}$$

$$T(s) \approx -kF_m G_m R_o \frac{V_{\text{out}}}{1-D} \frac{1}{1 + (s/\omega_{P(\text{dominant})})}, \quad \text{where } \omega_{P(\text{dominant})} = \frac{1}{R_o C_C} \tag{18}$$

where V_M, which relies on input line voltage and load current, is the amplitude of $V_{\text{saw\_m}}$ and $V_{\text{saw\_s}}$.

Fig. 20 illustrates the frequency response of the proposed interleaving PFC with the DNVSS and the ALD techniques. Two complex poles, which are constituted by the primary inductor L_p and the output capacitor C_{out} at the power stage, are located at 965 Hz. Since 965 Hz is much higher than the bandwidth of 20 Hz, the phase margin of the system is 90°. In practice, the mismatch exists between the primary inductors of master and slave, L_m and L_s. For instance, if L_s is larger than L_p by 15%, the complex poles are moved from 965 to 900 Hz. However, 900 Hz is much higher than the bandwidth of 20 Hz. In consequence, the proposed PFC behaves as a one-pole system

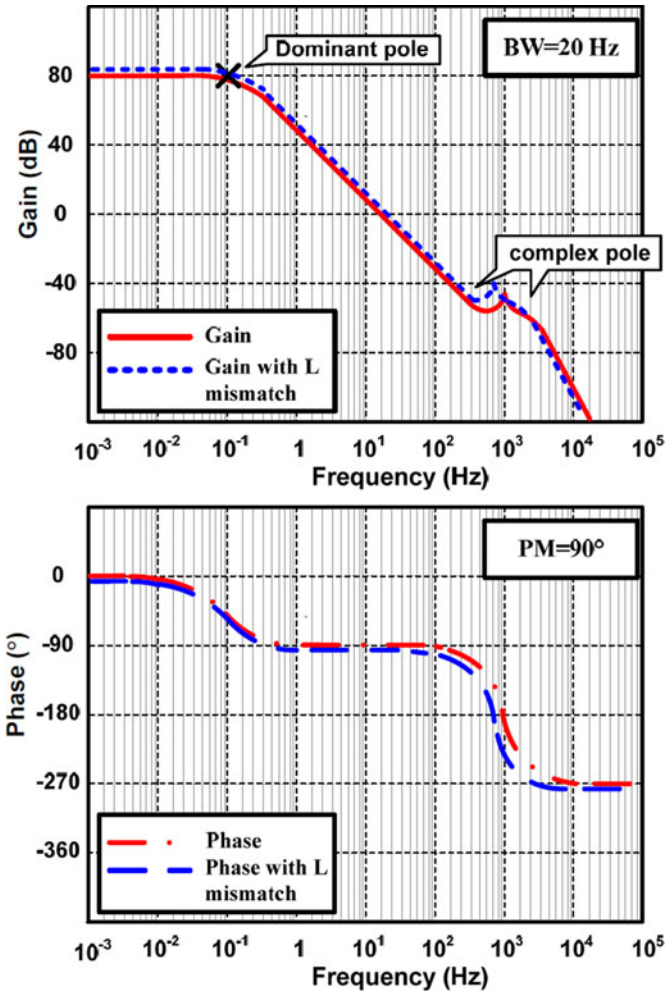

Fig. 20. Frequency response of the proposed interleaving PFC with DNVSS and ALD techniques.

and the stability is not obviously influenced by the mismatches at the power stage.

IV. Circuit Implementation

A. Proposed DNVSS Circuit

The proposed DNVSS technique is composed of variable sampling slope (VSS) generator and dual nondeadtime control as shown in Fig. 21. The VSS generator generates two ramp signals *slope1* and *slope2* with an adaptive slope, which is proportional to "$V_{\rm out}$ –$V_{\rm in}$," in order to alleviate the effect of $V_{\rm in}$ as mentioned in (8). Owing to a wide range of $V_{\rm in}$, the VSS circuit performs the subtraction function by the current mirror.

Due to high-voltage stress at $V_{\rm in}$ and $V_{\rm out}$, the resistors $R_1 - R_4$ are used as the voltage divider to sense $V_{\rm in}$ and $V_{\rm out}$ and to scale down those values to an acceptable voltage level for the integrated chip. However, $V_{\rm in}$ has a zero minimum voltage and would disable the circuit. To prevent this situation, transistors M_1 and M_2 work as the level shifter so that the circuit avoids the zero voltage happening at $V_{\rm in}$. Here, a simple transconductance formed by $M_{3,4}$ with $R_{5,6}$ can convert the voltage information $V_{\rm out}$ and $V_{\rm in}$ to the current information $I_{\rm out}$ and $I_{\rm in}$, respectively.

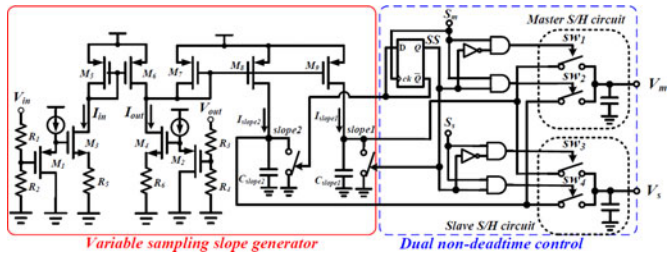

Fig. 21. Proposed DNVSS circuit.

Finally, $S_{\rm slope1,2}$ can be expressed in the following equation, where$C_{\rm slope1,2}$ is the output capacitor:

$$S_{\rm slope1,2} = \frac{I_{\rm slope1,2}}{C_{\rm slope1,2}} = (V_{\rm out} - V_{\rm in}) \cdot \frac{R_{2,4}}{R_{1,3}+R_{2,4}} \cdot \frac{1}{R_{5,6}} \cdot \frac{1}{C_{\rm slope1,2}}. \quad (19)$$

Substituting for $S_{\rm slope1,2}$ into (8) from (19) gives (20) since $S_{\rm slope1,2}$ is proportional to the value of "$V_{\rm out}$ –$V_{\rm in}$"

$$\frac{R_{2,4}}{R_{1,3}+R_{2,4}} \cdot \frac{1}{R_{5,6}} \cdot \frac{1}{C_{\rm slope1,2}} \cdot g_m \cdot R_{\rm saw} \cdot \frac{1}{S_{\rm saw\_s}} \cdot V_{\rm out} \approx 1. \quad (20)$$

Equation (20) indicates that $V_{\rm in}$ will not affect the interleaving operation. In other words, Δt_r in (7) is no longer affected by $V_{\rm in}$. Besides, the dual nondeadtime control generates two nondeadtime ramp signals. As shown in Fig. 21, the ramp signals *slope1* and *slope2* are generated by the $C_{\rm slope1}$ and the $C_{\rm slope2}$, respectively. Moreover, which ramp signal is selected is determined by the slope-selection signal *SS* synchronized with the master sampling signal S_m. Then, the *S/H* circuit samples the *slope1* and the *slope2* to produce V_m and V_s, respectively. The voltage difference between V_m and V_s which can represent the phase shift between two phases is converted to the current signal $i_{\rm error}$ by the OTA. If the phase shift is larger than 180°, $i_{\rm error}$ raises the dc level of $V_{\rm saw\_s}$ so that the charging period of the slave is shortened. Once the condition set by (20) is satisfied, the phase shift can be regulated to have 180° within one switching cycle.

Fig. 22 shows the simulation waveforms of *slope1* and *slope2* generated by the DNVSS technique. Due to the dual nondeadtime control, *slope1* and *slope2* arise alternatively so that there is no deadtime generated by the discharging period of the capacitor. Meanwhile, *slope1* and *slope2* are proportional to the value of "$V_{\rm out}$ –$V_{\rm in}$" owing to the VSS generator. Within a fixed charging period, the peak voltage of *slope1* or *slope2* presents the function of "$V_{\rm out}$ –$V_{\rm in}$."

B. Peak Detection Circuit

The peak detection circuit as depicted in Fig. 23 is used to detect the peak value of the line voltage $V_{\rm in}$. The output of the comparator *COM1* can turn ON/OFF the switch s_1. As s_1 turns ON, $V_{\rm peak}$ samples $V_{\rm in}$. Once $V_{\rm in}$ decreases, s_1 is turned OFF and the voltage of C_P keeps the peak value of $V_{\rm in}$. Meanwhile, *COM2* will generate the high-level signal to confirm

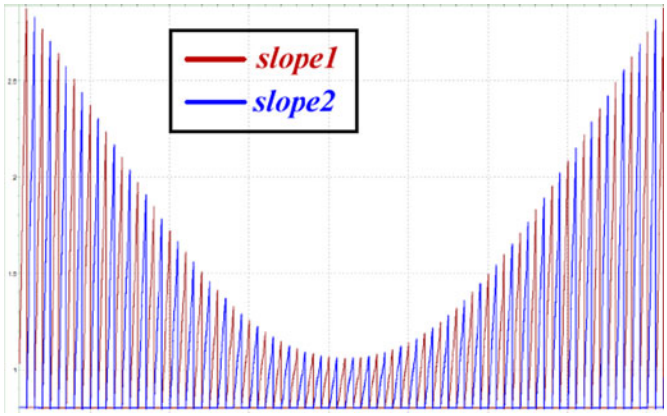

Fig. 22. Simulation waveforms of *slope1* and *slope2* generated by the DNVSS.

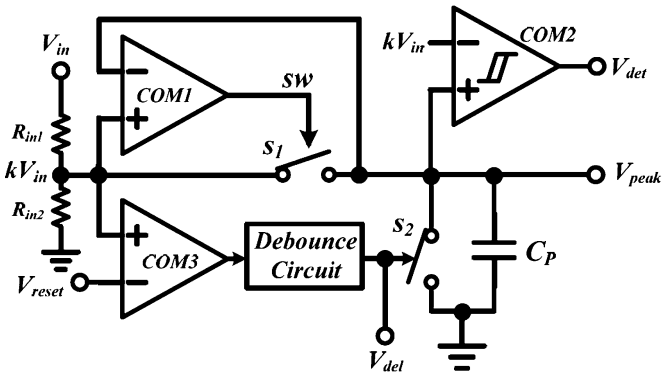

Fig. 23. Schematic of a peak detect circuit.

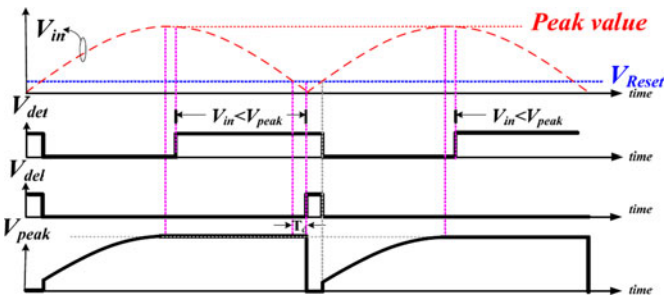

Fig. 24. Timing diagrams of the peak detect circuit.

that the peak value is ready. Furthermore, if the condition that $V_{\rm in}$ is lower than a designed reference voltage $V_{\rm Reset}$ lasts for a debounce time T_d, the signal $V_{\rm del}$ will be set high to reset $V_{\rm peak}$ for the consequent line voltage detection. As a result, $V_{\rm peak}$ will keep the peak value of $V_{\rm in}$ within one ac switching cycle as illustrated in Fig. 24.

C. ALD Circuit

Fig. 25 shows the ALD circuit to turn OFF the slave phase at light loads for power saving. When $V_{\rm det}$ is set high in the

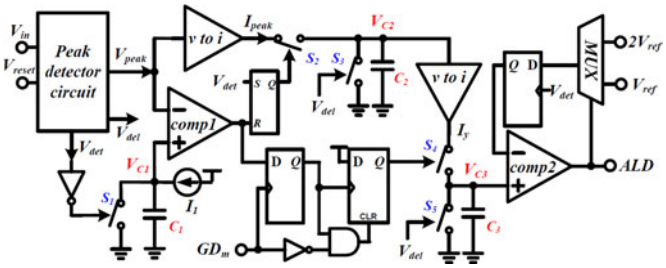

Fig. 25. Schematic of the ALD circuit.

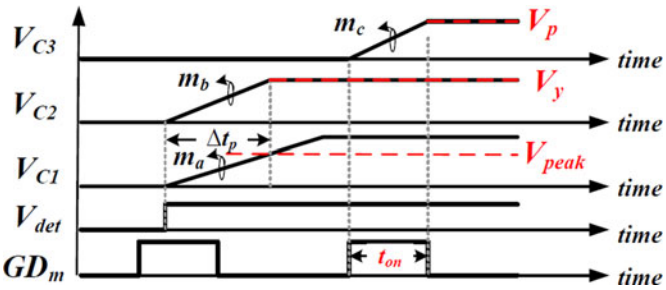

Fig. 26. Timing diagram of the ALD circuit.

beginning of the detection, capacitors C_1 and C_2 are charged by the constant current I_1 and the peak current $I_{\rm peak}$, respectively.

As depicted in Fig. 26 based on the derivation of (12), m_b (the slope of V_{C2}) and V_y are proportional to $V_{\rm peak}$ and the square of $V_{\rm peak}$, respectively. The capacitor C_3 is charged by the current I_y (proportional to V_y) at the first positive edge of GD_m (the PWM signal of the master channel) after V_{C2} is charged to the value of V_y. Consequently, V_p, which is proportional to the product of $t_{\rm on}$ and $V_{\rm peak}^2$, is obtained at the negative edge of GD_m. As mentioned in (9), the output power is proportional to the product of $t_{\rm on}$ and $V_{\rm peak}^2$. Therefore, the slave phase is turned ON or OFF according to the comparison result of V_p and the predefined reference voltage which is $V_{\rm ref}$ or $2V_{\rm ref}$ decided by the signal ALD as illustrated in Fig. 16. If V_p is less than $V_{\rm ref}$ in the interleaving operation, the ALD is set to low to turn OFF the slave phase. Simultaneously, the reference voltage will be updated to $2V_{\rm ref}$ when the next peak value of the line voltage is detected.

V. Experiment Results

The interleaving PFC controller with the DNVSS and ALD techniques was fabricated in the TSMC 0.5-μm 800-V UHV LDMOS process. The specifications of the interleaving PFC are listed in Table I. The output voltage of the PFC controller is 400 V for the next-stage PWM dc–dc converter. The chip micrograph is shown in Fig. 27(a). The sensitive analog circuits such as bandgap reference circuit and error amplifier EA are carefully isolated by double guard rings for switching noise immunity. The driver, which drives the power MOSFET M_{nm} and M_{ns} in Fig. 13, is placed near I/O pads to conduct a large amount of current. The prototype and experimental environment

TABLE I
DESIGN SPECIFICATIONS

Technology	TSMC 0.5μm 800V UHV LDMOS
Die area (with test pads)	2.15mm × 2.6mm
AC input voltage range V_{ac}	90~264V_{ac}
Output voltage (V_{OUT})	400V
Minimum Switching frequency (f_{SW})	>35kHz
Output power	180W
Primary inductor (L_p) of master and slave phase	400μH
Primary winding turns (N_p) of master and slave phase	58T
Auxiliary winding turns (N_{auxm}) of master and slave phase	5T
Output capacitor (C_{out})	68μF/450V
Compensation capacitor (C_c)	1μF
Output ripple (ΔV_{out})	19V

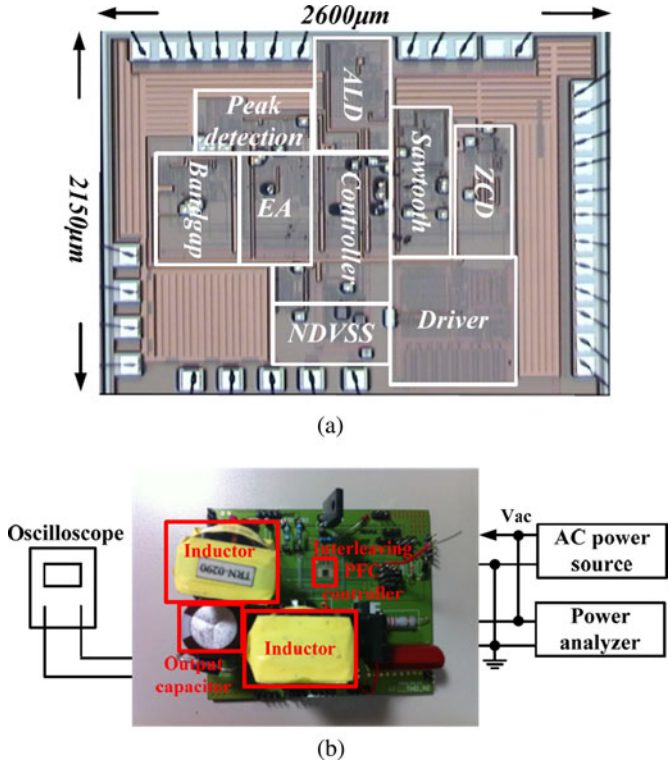

Fig. 27. (a) Chip micrograph. (b) Prototype and experimental environment of the interleaving PFC system.

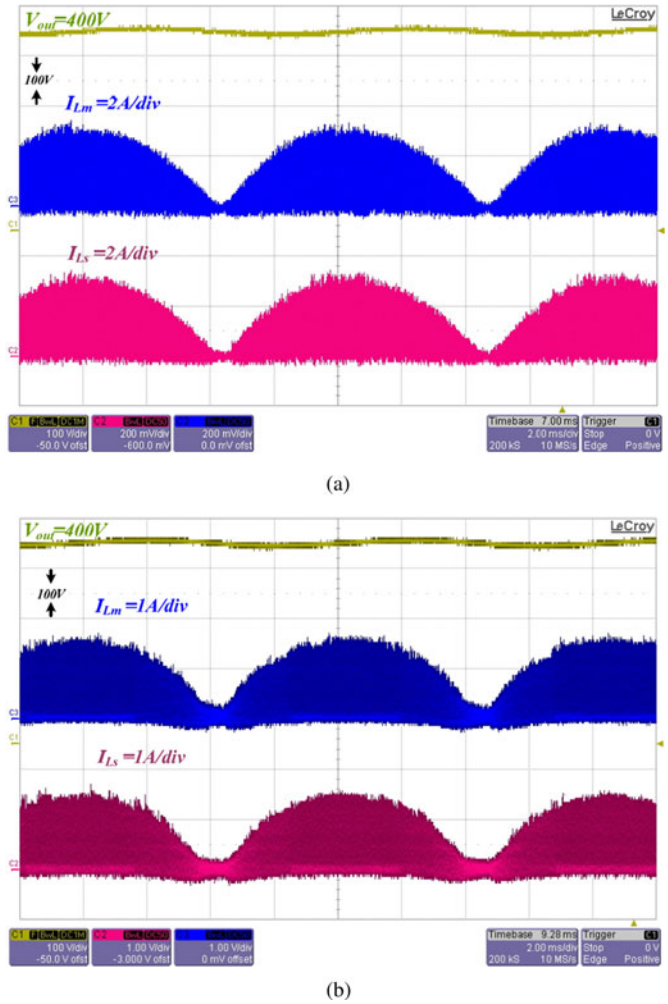

Fig. 28. Measured output voltages and input current with the load of 180 W at (a) $V_{\rm in}$ = 90 $V_{\rm ac}$ and (b) $V_{\rm in}$ = 220 $V_{\rm ac}$.

of the interleaving PFC system are shown in Fig. 27(b). The ac line voltage is provided by the ac power source. The power factor, THD, and waveforms can be measured by the power analyzer and the oscilloscope.

Fig. 28(a) and (b) shows the measured waveforms at full load at 90 and 220 $V_{\rm ac}$ input voltages, respectively. Two inductor currents of two phases are I_{Lm} and I_{Ls}. Simultaneously, $V_{\rm out}$ is regulated at 400 V with the load of 180 W. The measured interleaving current shows the DNVSS operation in Fig. 29. The DNVSS technique can have the advantage of ripple cancellation owing to zero T_d between the two phases. That is to say, a good interleaving control is achieved by the DNVSS technique. Meanwhile, Fig. 30 shows the function of the input current which can suppress the input current ripple effectively. Therefore, the input EMI filter and the size of output capacitor can be reduced effectively. Fig. 31 shows the measured waveforms of the output voltage and the line current at the input line rms voltage of (a) 90 V, (b) 110 V, (c) 220 V, and (d) 240 V.

Fig. 32 shows the measure results with the line voltage of 90 $V_{\rm ac}$. Experimental results of interleaving PFC with the ALD technique design shows the output power steps from 45 to 180 W

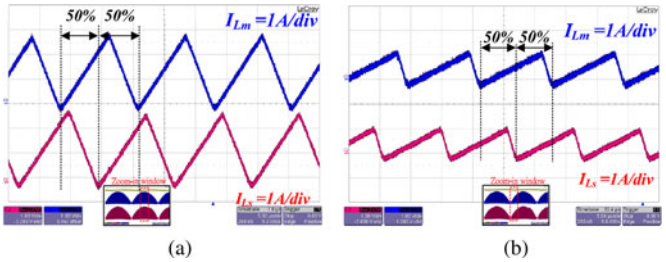

Fig. 29. Measured inductor current waveforms with 180° phase shift under interleaving controls at $V_{\rm in} = 90\ {\rm V_{ac}}$. (a) Zoom-in waveforms at high ac input voltage. (b) Zoom-in waveforms at low ac input voltage.

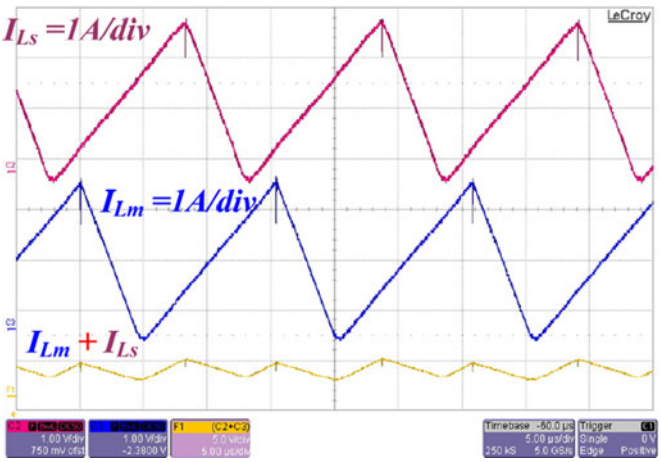

Fig. 30. Measured input current ripple with the output power of 180 W.

[as shown in Fig. 32(a)] or vice versa [as shown in Fig. 32(b)]. The ALD technique will turn OFF the slave PFC controller from heavy to light load for high efficiency. Meanwhile, the interleaving system will restart again when the output load changes from light to heavy load. The phase management can effectively enhance the efficiency of the power conversion system. Fig. 33 shows the efficiency improvement contributed by the ALD technique. The maximum improved efficiency is 6% at light load of 40 W. Fig. 34 shows the measured minimum efficiency with different ac line voltages and temperatures considering inductance mismatch. The inductance mismatch of the slave is normalized to the inductance of the master, i.e., L_s/L_m. Since the inductance mismatch of the slave slightly degrades the efficiency in interleaving operation, the minimum efficiency happens on the transition point between single-phase and interleaving operation. In spite of this circumstance, the light load efficiency is still greatly improved.

The measured harmonic currents with the input line rms voltages of 90 and 110 V at the output power of 90 W are shown in Fig 35. The EN61000-3-2 class D regulation at the output power of 90 W is also shown in Fig. 35. It can be seen that the EN61000-3-2 class D regulation is met with enough design margin. Fig. 36 shows the comparison diagrams of the measured power factor and THD at the output power of 90 W with different input line rms voltages. Obviously, the power factor

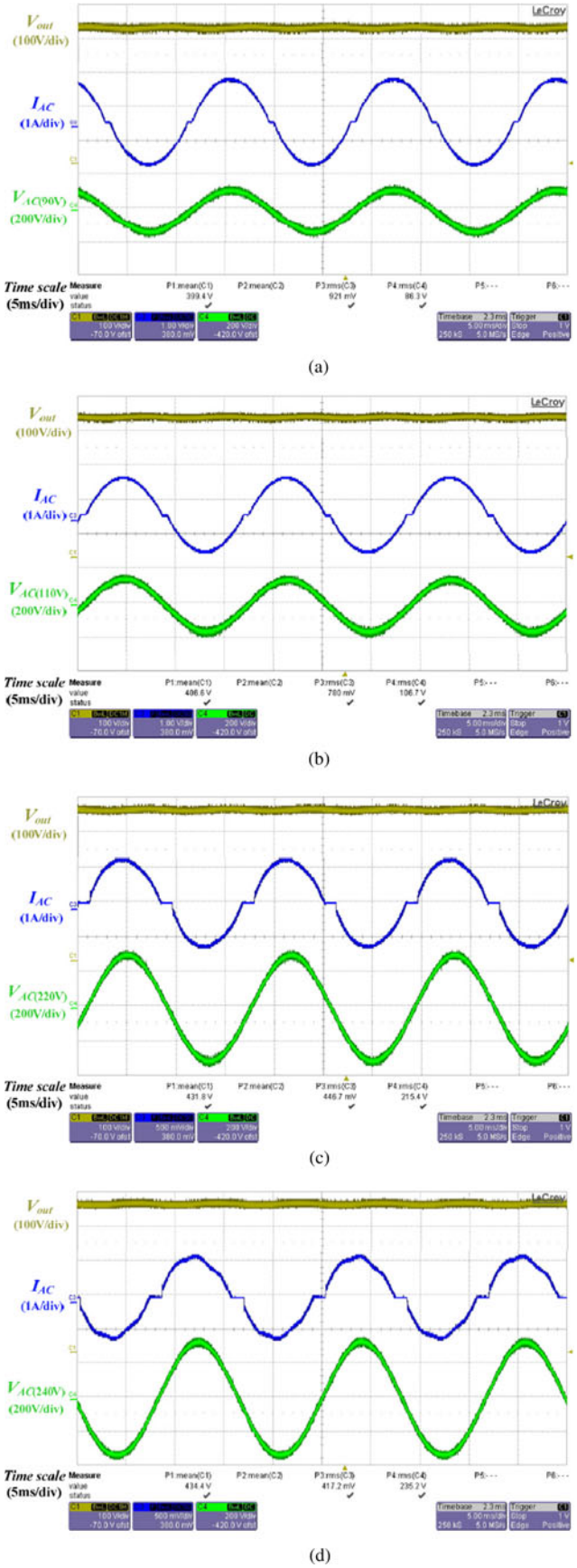

Fig. 31. Measured waveforms of the output voltage and the line current at the input line rms voltage of (a) 90 V, (b) 110 V, (c) 220 V, and (d) 240 V.

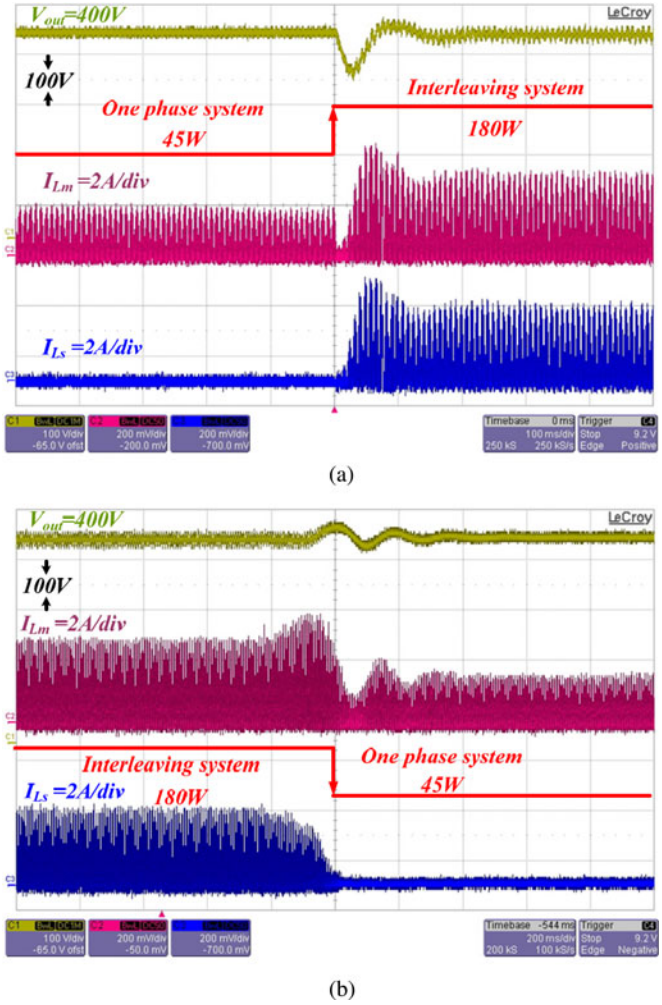

Fig. 32. Waveforms of the proposed interleaving PFC with the ALD technique when the output load changes from 45 to 180 W in (a) and vice versa in (b).

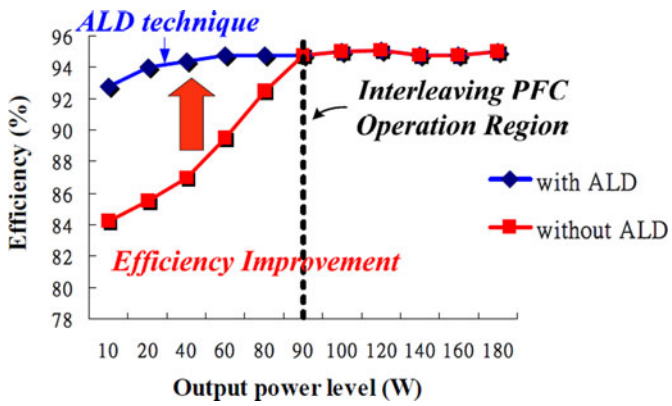

Fig. 33. Efficiency improvement contributed by the ALD technique.

and THD are not affected by the proposed DVSS and ALD techniques. The comparison table is shown in Table II. The proposed method can achieve high efficiency at light loads and high PF at the same time.

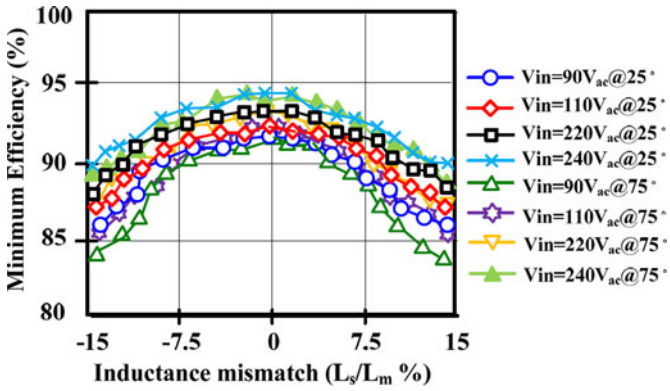

Fig. 34. Minimum efficiency considering inductance mismatch with different ac line voltages and temperatures.

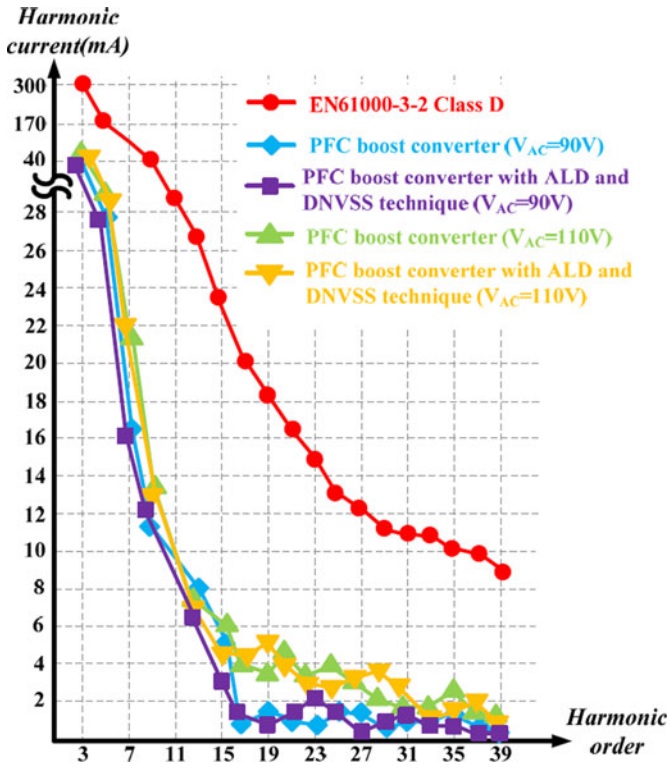

Fig. 35. Measured harmonic currents and EN61000-3-2 class D regulation at the output power of 90 W.

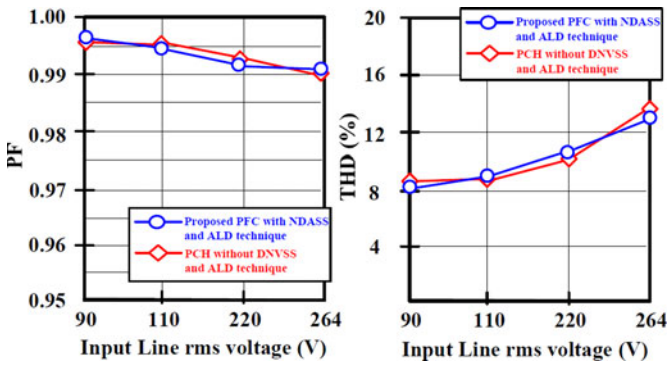

Fig. 36. Comparison diagrams of the measured power factor and THD at the output power of 90 W with different input line rms voltages.

TABLE II
COMPARISON TABLE WITH THE PRIOR ARTS

	This work	[27]	[28]	[30]	[31]
Input line voltage	90~264V_{ac}	70~270V_{ac}	90~265V_{ac}	220V_{ac}	90V_{ac}
Output voltage	400V	400V	400V	400V	N/A
Circuit integrated	Fully integrated	N/A	System level	System level	System level
Efficiency (light load)	94%	88%	92%	89%	91.5%
Control method	Interleaving with ALD	Natural interleaving	Phase shifter	Average current mode	Phase shedding
Power factor	0.99	N/A	0.99	0.98	N/A

VI. CONCLUSION

In this paper, the proposed interleaving PFC with the DNVSS and the ALD techniques is presented. With the DNVSS technique, precise phase sensing can be carried out and phase regulation can be achieved over the whole ac switching cycle. As a result, the input current ripple is greatly reduced. Furthermore, a high efficiency of 95% at an output power of 180 W can be achieved by the ALD technique. The power efficiency can be always kept higher than 92% over a wide load current range. Light load efficiency can be raised about 6% higher than that of a conventional interleaving PFC design. The test circuit fabricated in the TSMC 800-V UHV process demonstrates the performance of the highly integrated interleaving PFC controller.

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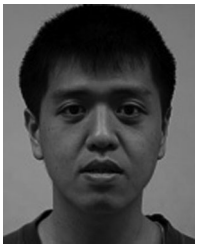

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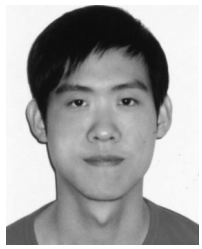

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