

A Triangular Connection Hopfield Neural Network Approach to Analog-to-Digital Conversion

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Abstract— A Hopfield-type neural network approach which leads to an analog circuit for implementing the A/D conversion is presented. The solution of the original symmetric connection Hopfield A/D converter sometimes may reach a “spurious state” that does not correspond to the correct digital representation of the input signal. An A/D converter based on the model of nonsymmetrical neural networks is proposed to obtain the stable and correct encoding. Due to the infeasible conventional RC-active implementation, a cost-effective switched-capacitor implementation by means of Schmitt triggers is adopted. It is capable of achieving high performance as well as a high convergence rate. Finally, a simulation using a tool called SWITCAP is conducted to verify the validity and performance of the proposed implementation.

I. INTRODUCTION

ARTIFICIAL neural networks contain a large number of identical computing neurons with specific interconnection strengths between neurons. The massively parallel processing power of the neural network lies in the cooperation of highly interconnected computing neurons. References [1], [2] demonstrated that their networks have the potential to produce real-time solutions to optimization problems. It also has been shown that Hopfield-type neural networks can solve a number of difficult optimization problems in a time determined by system RC time constants, not times determined by complexity.

From a design point of view, the Hopfield neural networks with the symmetric connections are especially convenient for the A/D conversion task. Due to the nature of the energy function, the solution of this symmetric network is highly dependent on its initial state. The energy function may decrease and then settle to one of the equilibrium points called the “spurious state” that does not correspond to the correct digital representation of the input signal. Reference [3] proposed a network with additional self-correction circuitry to eliminate this spurious state. However, a more systematic approach to solving the problem of spurious states is based on a particular class of nonsymmetric neural networks. Reference [4] showed that this structure of neural network has no spurious state, and the dynamic behavior of the structure is characterized by a unique equilibrium point which is the global minimum. In

Manuscript received May 19, 1993; revised March 25, 1994.

This work was supported in part by the National Science Council, Republic of China, under contract NCS81-0404-E-009-622.

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IEEE Log Number 9406572

other words, the system will converge toward this point for every choice of initial conditions. In designing an effective A/D converter, the choice of nonsymmetrical networks is not restrictive from a biological point of view. Section III shows that the triangularly connected network is the most appropriate structure for implementing the A/D conversion. Since a stable encoding doesn't mean correct encoding, one may design the connection strengths T_{ij} between neurons so that this global equilibrium point coincides with the desired output for a given input signal. Reference [5] introduced the conditions to ensure the correctness of the stable encoding and to determine the connection strengths. The concept of Cattermole's method is based on pulse code modulation. More recently [6], referring to the previous work of Cattermole, have proposed the realization of A/D converters that are modified with respect to the original Hopfield neural network, in order to avoid the incorrect conversion of the Hopfield A/D. In section III, we will determine appropriate connection strengths of the triangular connection network for correct A/D encoding on the basis of Cattermole's method. Usually, Hopfield neural networks are realized by conventional RC-active designs which are not the best suited for monolithic implementation, especially taking into account that accurate resistor ratios and large RC values are required for the design. This drawback can be overcome by using switched-capacitor techniques [7]–[11] which have good linearity and monotonicity in spite of circuit configuration.

Section V presents a cost-effective switched-capacitor implementation by means of multi-input Schmitt triggers to the triangularly connected A/D converters. Moreover, the Schmitt triggers with hysteresis can also avoid the unpredicted noise perturbation and instability resulting from the high-gain nonlinear amplifiers. Experimental results and comparisons will be discussed in the last section.

II. SYMMETRIC HOPFIELD NEURAL NETWORK

The Hopfield model [1], [2] is a popular model of a continuous neural network of n interconnected nodes. Each node is assigned a potential, $u_j(t)$, $j = 0, 2, \dots, (n-1)$ as its state variable. Each node receives external input bias $I_i(t)$, and internal inputs from other nodes in the form of a weighted sum of firing rates $\sum_j T_{ij}g_j(\lambda_j u_j)$, where $g_j(\cdot)$ is a monotonically increasing sigmoidal bounded function converting the potential to firing rate. The equations of motion are

$$C \frac{du_i}{dt} = -\frac{u_i}{R} + \sum_{j=1}^{n-1} T_{ij}V_j + I_i$$

$$V_i = g_i(\lambda_i u_i) \quad (1)$$

where T_{ij} is the conductance connected between the i th neuron input and the j th neuron output, V_i is the i th neuron output voltage, I_i is the input current to the i th neuron, $-\frac{u_i}{R}$ is the current flow due to finite transmembrane resistance R , λ_i 's are the amplifier gains, and $g_i(\lambda_i u_i)$ is typically identified as $\frac{1}{2}(1 + \tanh(\lambda_i u_i))$.

References [1], [2] have shown that in the case of symmetric connections ($T_{ij} = T_{ji}$), the equations of motion for this network of analog processors always lead to a convergence to stable states, in which the output voltages of all amplifiers remain constant. In addition, when the diagonal elements (T_{ii}) are 0 and the amplifier gains λ_i 's are high, the stable states of a network comprised of n neurons are the minima of the computational energy or Lyapunov function

$$E = -\frac{1}{2} \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} T_{ij} V_i V_j - \sum_{i=0}^{n-1} I_i V_i. \quad (2)$$

The state space over which the analog circuit operates is the n -dimensional hypercube defined by $V_i = 0$ or 1. However, it has been shown that the high-gain limit networks with vanishing diagonal connections ($T_{ii} = 0$) have minima only at the corners of this space [2]. Under these conditions the stable states of the network correspond to those locations in the discrete space consisting of the 2^n corners of this hypercube which minimize E .

In order to utilize the concept of Hopfield network, the design of an A/D conversion could be reformulated as minimizing a quadratic programming problem subject to the corresponding binary variables which are the best digital representations of an analog signal X . In other words, the best digital representation is obtained by finding the binary variables V_i which minimize the quadratic metric:

$$E = \frac{1}{2} \left(X - \sum_{i=0}^{n-1} V_i 2^i \right)^2. \quad (3)$$

However, there is no guarantee that the values of V_i will be close to 0 or 1 to be identified as digital logic levels by minimizing (3). To eliminate this problem, one may add one additional term to the E function. Its form can be chosen as

$$\frac{1}{2} \sum_{i=0}^{n-1} (2^i)^2 [(1 - V_i)V_i]. \quad (4)$$

Hopfield [2] showed that the complete energy function for the A/D conversion can be expanded and rearranged into the form

$$E = -\frac{1}{2} \sum_{j=0}^{n-1} \sum_{i \neq j}^{n-1} T_{ij} V_i V_j - \sum_{i=0}^{n-1} I_i V_i \quad (5)$$

where

$$\begin{aligned} T_{ij} &= -2^{(i+j)} \\ I_i &= (-2^{(2i-1)} + 2^i X). \end{aligned} \quad (6)$$

Unfortunately, [3] showed that the energy of a symmetric Hopfield network has many local minima, and the resultant

network output does not correspond to the digital representation of the analog signal X . In the next section, a more systematic approach based on the concept of a nonsymmetric neural network is proposed to eliminate the local minima.

III. A TRIANGULARLY CONNECTED HOPFIELD NETWORK WITH APPLICATION TO A/D CONVERSION

In this section, we would like to describe the global stability feature of a triangularly connected neural network proposed in [4]. In general, two essential stability properties (uniqueness of the equilibrium point and global attractivity) are considered in the network. The following theorem is presented to provide the validity of both properties.

Theorem 1 A system of first-order nonlinear differential equations is

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{f}(\mathbf{x}) \quad (7)$$

where $\mathbf{A} = (a_{ij})$ is an $n \times n$ constant matrix with $a_{ij} = 0$ for $i > j$, $\mathbf{x} = (x_0, \dots, x_{n-1})^t \in R^n$, and $\mathbf{f} : R^n \rightarrow R^n$ is a continuous vector function $\mathbf{f} = (f_0, f_1, \dots, f_{n-1})^t$ such that $f_{n-1}(x) = \text{constant}$ and $f_i(\mathbf{x}) = f_i(x_{i+1}, x_{i+2}, \dots, x_{n-1})$, $i = 0, \dots, (n-2)$.

If the linear system $\dot{\mathbf{x}} = \mathbf{A}\mathbf{x}$ is asymptotically stable, then the system (7) has only one equilibrium point $\mathbf{x}^e = (x_0^e, \dots, x_{n-1}^e)^t$ which is globally attractive in R^n [4].

According to Theorem 1, the equations of a lower triangularly connected Hopfield network can be obtained as a particular case of system (7). For the purpose of simplicity, the matrix \mathbf{A} and f_i in Theorem 1 are given by

$$\begin{aligned} \mathbf{A} &= \text{diag} \left(\frac{-1}{\tau_i} \right) \\ f_i &= \frac{1}{C_i} \{ [\mathbf{T}\mathbf{g}]_i \} + \bar{I}_i \end{aligned} \quad (8)$$

where $\tau_i = R_i C_i$, $\mathbf{T} = (T_{ij})$ is an upper triangular connection matrix with $T_{ij} = 0$, for $i \geq j$ and $0 \leq i, j \leq n-1$, $\mathbf{g} = (g_1, g_2, \dots, g_n)^t$ and $g_i : R \rightarrow R$ are continuous functions. C_i, R_i and \bar{I}_i are real constants with $C_i, R_i > 0$. $[\mathbf{T}\mathbf{g}]_i$ is the i -th component of the resulting vector of $\mathbf{T} \cdot \mathbf{g}$.

By substituting (8) into (7), the system dynamics of the triangularly connected network are obtained:

$$\begin{aligned} C_i \frac{du_i}{dt} &= \frac{-1}{R_i} u_i + \sum_{j=i+1}^{n-1} T_{ij} g_j(u_j) + \bar{I}_i, \\ i &= 0, 1, \dots, (n-1). \end{aligned} \quad (9)$$

Notice that the variables x_i in (7) are replaced by the new variables u_i , respectively.

Since \mathbf{A} of (8) is negative definite, it can be shown that $\dot{\mathbf{u}} = \mathbf{A}\mathbf{u}$ is asymptotically stable. Thus, from Theorem 1, system (9) is globally attractive, and its associated equilibrium point $\mathbf{u}^e = (u_0^e, u_1^e, \dots, u_{n-1}^e)^t$ is determined by the following equations uniquely:

$$\frac{1}{R_i} u_i^e = \sum_{j=i+1}^{n-1} T_{ij} g_j(u_j^e) + \bar{I}_i, \quad i = 0, 1, \dots, (n-1). \quad (10)$$

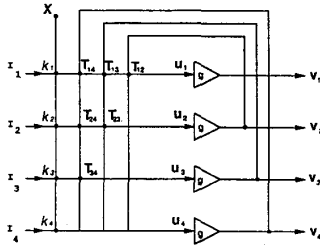


Fig. 1. Triangular Hopfield network for the 4-bit A/D converter.

Considering the circuit realization of system (9), the system dynamics should be rewritten in a state equation formulation as:

$$C_i \frac{du_i}{dt} = \frac{-1}{R_i} u_i + \sum_{j=i+1}^{n-1} T_{ij} V_j + \bar{I}_i \quad (11.a)$$

and

$$V_i = g(u_i) \quad (11.b)$$

where u_i and V_i are now the neural state variables and the output variables respectively and $i = 0, 1, \dots, (n-1)$.

Undoubtedly, system (11) is really identical to the dynamics of a Hopfield neural network characterized by an upper triangular connection $\{T_{ij}\}$. In designing the A/D conversion based on (11), the term \bar{I}_i is subdivided into a constant biasing term I_i and a term depending on an input signal X :

$$\bar{I}_i = I_i + k_i X \quad (12)$$

where $k_i \in R$. This leads to the triangularly connected network shown in Fig. 1 in the case $n = 4$. Meanwhile, the parameter values T_{ij} , I_i and k_i in Fig. 1 are still unknown. It should be mentioned that the procedure of determining those values by Avitabile [4] is truly unclear. A possible solution to determine those values is introduced by using the concept of Cattermole [5].

In order to investigate the encoding procedure and determine the connection strengths T_{ij} and bias I_i of an upper triangularly connected Hopfield network for an A/D conversion with n bits, [5] suggested that the nonlinear decision functions $g_i(\cdot)$ could be modelled as digital comparators:

$$b_i = \begin{cases} 0 & \text{if } X < t_i \\ 1 & \text{if } X > t_i \end{cases} \quad i = 0, 1, \dots, (n-1) \quad (13)$$

where b_i is the i -th bit used to represent the input signal X , and the thresholds t_i are given by

$$t_i = (1 - b_i)2^i + \sum_{j=i}^{n-1} b_j 2^j. \quad (14)$$

Moreover, [5] showed that the decision scheme defined in (13) and (14) can ensure the stability and correct encoding of an A/D conversion. In (14), the index $i = n-1$ corresponds to the most significant bit (MSB), and the index $i = 0$ corresponds to the least significant bit (LSB) respectively. Equations (13) and (14) prove that the decision on the i -th bit depends on the decisions for the more significant bits

($i+1, i+2, \dots, n-1$) but not on the decisions for the lesser significant bits. Therefore, the MSB must settle before the next digit decision and so on, down to the LSB.

Next, it determines the parameter values T_{ij} , I_i and k_i from the equilibrium point when the network stops corresponding to the digital representation of the input signal obtained from (13) and (14). With a suitable change of indexes in (11), the equilibrium equation becomes

$$\frac{1}{R_i} u_i^e = \sum_{j=i+1}^{n-1} T_{ij} V_j^e + \bar{I}_i, \quad i = n-1, \dots, 0. \quad (15)$$

Notice that the index $i = (n-1)$ for the MSB and $i = 0$ for the LSB.

In the extreme case, the gain of the sigmoidal decision functions $g_i(\cdot)$ in the Hopfield network is chosen to be a sufficiently large value. Therefore, those functions can be modelled as digital comparators as mentioned in (13), that is,

$$V_i^e = g_i(u_i^e) = \begin{cases} 0 & \text{if } u_i^e < 0 \\ 1 & \text{if } u_i^e > 0. \end{cases} \quad (16)$$

Substituting (12) and (15) into (16), we have

$$V_i^e = \begin{cases} 0 & \text{if } \sum_{j=i+1}^{n-1} T_{ij} V_j^e + I_i + k_i X < 0 \\ 1 & \text{if } \sum_{j=i+1}^{n-1} T_{ij} V_j^e + I_i + k_i X > 0. \end{cases} \quad (17)$$

While reaching the equilibrium point, the i -th steady-state output variable V_i^e would be identical to the desired i -th digit b_i determined by (13) and (14) when the values of parameters involved in (17) are identical to those of (13) and (14). Consequently, the connection strengths, bias and k_i become

$$T_{ij} = -2^j \quad \text{for } j \geq i+1, \quad I_i = -2^i \quad \text{and } k_i = 1 \quad (18)$$

where $i = n-1, \dots, 0$.

Since the network uses resistors to implement the connection strengths $R_{ij} = 1/|T_{ij}|$, the settling time of each digit would depend on the sum of weighting resistors associated with the digit. From (18), it turns out that the sum of resistors for any digit is smallest for the MSB progressing to the largest for the LSB. Therefore, the settling time of the more significant bit is faster than the lesser significant bit. The order of decreasing significance would ensure the correct encoding of A/D conversion. Unfortunately, the network based on Cattermole's work uses the discontinuous digital comparators which can not meet the continuous assumption in Theorem 1. A possible expression for $g_i(\cdot)$ is the sigmoidal function suggested in [2]. The accurate digital representation may be achieved by increasing the amplifier gain of the function. Indeed, the high-gain amplifiers would suffer from the potential instability and unpredicted noise perturbation. An alternative solution is to use more realistic Schmitt triggers with hysteresis instead of the high-gain amplifiers. The steepness of the characteristic as shown in Fig. 2 for $u_i = +u$ and $u_i = -u$ is extremely high due to the effect of the positive feedback. Moreover, since the hysteresis and noise are presented on the input u_i , the original equilibrium points characterized by the input stable variables $u_i = +u$ and $u_i = -u$ become unstable. The new stable equilibrium points are now characterized by the output voltages $V_i = +1$ or $V_i = 0$. Reference [7] showed that

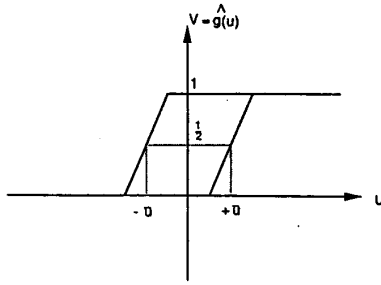


Fig. 2. Input-output characteristic of a Schmitt trigger with hysteresis.

the lower triangular neural-based A/D converter by means of Schmitt triggers can avoid the above-mentioned problems.

IV. THE CORRECT ENCODING OF THE NEURAL-BASED A/D CONVERSION

It is known that a particular encoding scheme which satisfies the assumption in Theorem 1 will reach a stable equilibrium solution. But this stable code doesn't guarantee that the solution is correct. In other words, all correct codes are stable, but not all stable codes are correct. It is quite interesting to give a proof of correct coding for the encoding network based on [5], which introduced the conditions to generate the correct outputs $b_j = V_j^e$ (either zero or one) of each comparator; they are described in Theorem 2.

Theorem 2 The binary weighted sum of all n comparator output digits b_j is to correctly encode the input X when the following condition is satisfied:

$$0 \leq X - \sum_{j=0}^{n-1} b_j 2^j < 1 \tag{19}$$

and, since $2^i > \sum_{j=0}^{i-1} 2^j$ for $i \geq 1$, the constraint on the $(n - i)$ most significant digits is:

$$0 \leq X - \sum_{j=i}^{n-1} b_j 2^j < 2^i \quad 0 \leq i \leq n - 1. \tag{20}$$

Notice that a new variable X should be changed as $X' + \frac{1}{2}$ while minimizing the encoding error in the least squares sense. Observing (13) and (14), the decision for the $(n - i)$ most significant digit would be shown to satisfy the condition described in (19). From (14), the decision function

$$D_i = X - t_i = X - (1 - b_i)2^i - \sum_{j=i}^{n-1} b_j 2^j \tag{21}$$

is introduced to decide the output V_j according to (13), that is:

$$b_i = \begin{cases} 0 & \text{if } D_i < 0 \\ 1 & \text{if } D_i > 0 \end{cases} \quad i = 0, 1, \dots, (n - 1). \tag{22}$$

Equation (22) implies that $D_i|_{b_i=0} = X - 2^i - \sum_{j=i}^{n-1} b_j 2^j < 0$ and $D_i|_{b_i=1} = X - \sum_{j=i}^{n-1} b_j 2^j > 0$. Therefore, it has been shown that the condition in (20) is satisfied by applying the Cattermole encoding method.

Next, [6] showed that the Cattermole encoding satisfies the condition (19). By using the fact that the decision for the more

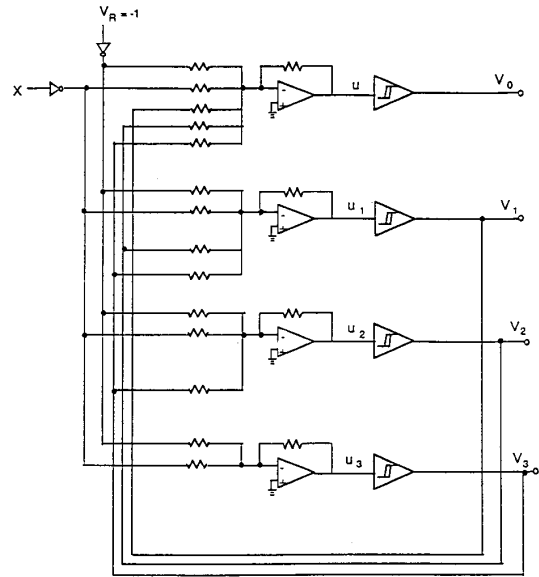


Fig. 3. Triangular structure for the 4-bit A/D converter by means of Schmitt triggers.

significant digit is determined before the lesser significant digit decision, this implies that the Cattermole-based neural network guarantees the stability and correctness of encoding an input signal.

V. SWITCHED-CAPACITOR REALIZATION FOR NEURAL-BASED A/D CONVERTER

In the realization of the Tank and Hopfield neural network [1], [2], they use the conventional RC-active design techniques. However, the RC-active design is not the best suited for monolithic implementation since accurate resistor ratios and large RC values are required for the design. In this paper, we try to overcome this drawback by focusing on the design of implementing the triangularly connected Hopfield network using switched-capacitor techniques [8]-[10]. The switched-capacitor implementation as shown in Fig. 4 is obtained by placing the basic switched-capacitor modules into the triangularly connected neural-based A/D converter in Fig. 3. The details about the schematic realization of each basic module will be discussed in the next section.

A. A Mapping Between Resistor and Switched-Capacitor Networks

The complete schematic for the 4-bit A/D converter is presented in Fig. 3 which contains resistors, amplifiers, and Schmitt triggers. Let us consider the circuit for a specific bit, i.e., the i -th bit, for the sake of simplicity. This leads to the circuit shown in Fig. 4 that contains an inverting summer and a Schmitt trigger. The inverting summer produces an output u_i given by

$$u_i = - \sum_{j=1}^n a_j \frac{R}{R_j} \tag{23}$$

where a_j are the input voltages.

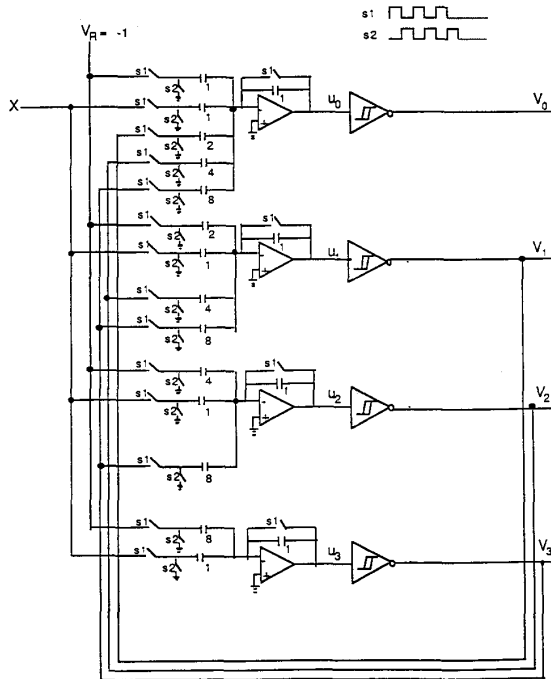


Fig. 4. Simple realization of the triangular neural-based A/D converter using SC summers.

The Schmitt trigger acts as a comparator, and its output is $V_i = 0$ or $V_i = 1$. To avoid the unstable phenomenon caused by the nonideal elements and noise, the Schmitt trigger should include the function of hysteresis. It is to be noted that the width of the hysteresis must be chosen on the basis of a compromise between accuracy of the conversion and the amplitude of the noise imposed upon u_i . A mapping is presented below that takes the summer and Schmitt trigger containing only resistors, op amp and voltage comparator and constructs their corresponding switched-capacitor implementations.

Fig. 5 is a block diagram illustrating the basic structure of a switched-capacitor summer. This circuit is controlled by two nonoverlapping clock phases $s1$ and $s2$. During the clock phase $s1$ the feedback capacitor C_R is discharged while the feed-in (input) capacitors C_1, C_2, \dots and C_k are charged to the input voltages, v_1, v_2, \dots and v_k respectively. When C_i is switched to ground during the clock phase $s2$ the charge from C_i equals $C_i v_i$, where $1 \leq i \leq k$. The total amount of charges will be transferred to the capacitor C_R . Thus, the ideal output voltage during clock phase $s2$ becomes

$$v_o = \sum_{i=1}^n \frac{C_i}{C_R} v_i. \quad (24)$$

To reduce the clock-feedthrough error, an optional offset (V_{off}) can be utilized to compensate the error resulting from the summer of Fig. 5.

B. The Schmitt Trigger Based on Switched-Capacitor

The Schmitt trigger is a comparator with hysteresis which results from positive feedback and is used to compensate the

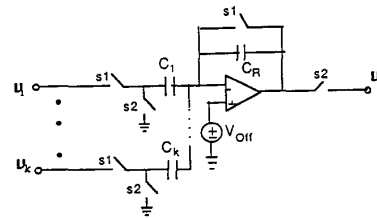


Fig. 5. The realization of SC summer with offset.

noise involved in the A/D converter. The Schmitt trigger is called inverting or clockwise bistable, because the output goes from the high state to the low state when the input voltage becomes larger. The bistable device can be realized easily by using SC techniques [9]. Fig. 6(a) shows an SC Schmitt trigger with a voltage-controlled width of the hysteresis, controlled by a voltage $V_c > 0$. The voltage V_R is given as

$$V_R = \begin{cases} aV_c & \text{for } K = 1 \\ -aV_c & \text{for } K = 0 \end{cases} \quad (25)$$

which generates the switching threshold voltages $V_T^+ = aV_c$ and $V_T^- = -aV_c$, where a is the amplifier gain. This means that V_c controls the width of the hysteresis. The above circuit can be extended to multiple inputs as shown in Fig. 6(b). Fig. 6(b) shows that the circuit is implemented using an SC charge balance comparator and a D -flip-flop or latch [9]. The Schmitt trigger can switch to its high output state $K = 1$ when the weighted sum of input signals $C_1 v_1 + C_2 v_2 + \dots + C_m v_m$ reaches the values $-C_0 V_c$ and $V_c = V_B^-$ where V_B^- corresponds to the lower magnitude of the output of the D -flip-flop or negative power supply voltage. Analogously it can switch to the low output state $K = 0$ when this sum is lower than $-C_0 V_c$ and $V_c = V_B^+$ where V_B^+ corresponds to the positive supply voltage. Moreover, Fig. 6(c) produces the two different output state voltages simultaneously. There are two possible approaches to implement the 4-bit neural-based A/D converter shown in Fig. 4. One of the feasible implementations is realized by four SC summers and single-input Schmitt triggers directly. Meanwhile, this hardware implementation does not seem to be cost effective. To reduce the implementation cost, it is found that a multi-input SC Schmitt trigger is particularly suitable for implementing the triangularly connected neural-based A/D converter. The schematic of cost-effective SC implementation is illustrated in Fig. 7.

VI. COMPUTER SIMULATION

To verify the effectiveness of the Schmitt trigger-based switched-capacitor implementation, a triangularly connected neural-based A/D converter of four bits is considered in the following example. The implementation shown in Fig. 7 is controlled by two clock phases $s1$ and $s2$. The circuit is reset during clock phase $s1$, and the outputs are available at the negative terminals during clock phase $s2$. The values of ca-

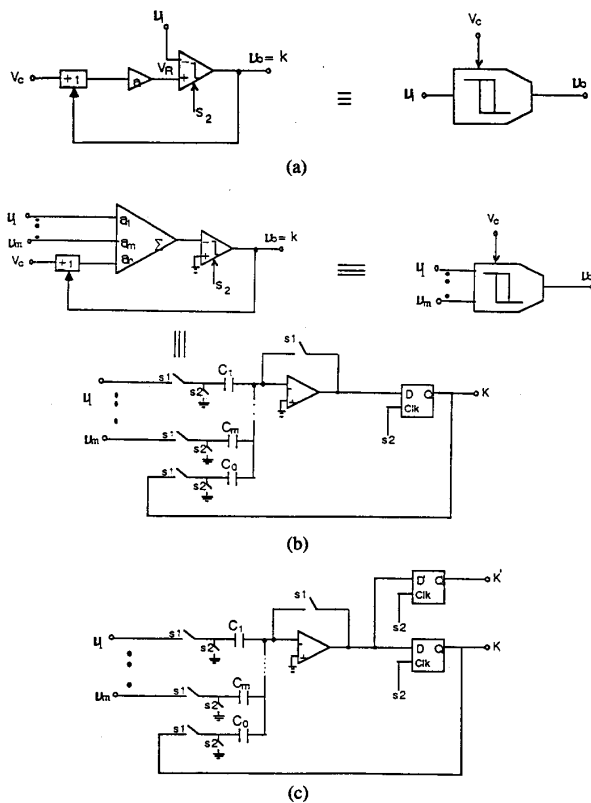


Fig. 6. The realization of multi-input Schmitt trigger using SC circuits. (a) Functional diagram of the SC Schmitt trigger with controlled hysteresis. (b) SC Schmitt trigger with multiple inputs. (c) Two-output-state multi-input Schmitt trigger.

capacitors are determined according to the connection strengths T_{ij} defined in (18). The reference voltage V_R together with appropriate values for capacitors is used to provide the value of each bias I_i defined in (18).

We have simulated the switched-capacitor neural-based A/D converter using a simulation tool called SWITCAP. The switching clock period is 1n sec. Fig. 8 shows the time evolution of each resultant output digit when the input signal is equal to 11. It is seen that the most significant bit (MSB) settles down before the next digit decision. The least significant bit takes about 10 clock periods to arrive at the stable state. The computation time for the neural-based A/D converter is identified as 10 ns. The voltage transfer curve for the original Hopfield A/D converter is shown in Fig. 9. The input signal range should correspond to each output value in order to ensure the correct encoding. Unfortunately, two different input signal ranges may have the same output value. This phenomenon is caused by the local minima in the original Hopfield energy function. Fig. 10 shows the simulated voltage transfer characteristics of the triangularly connected neural-based A/D converter. In this case, a monotonically increasing analog input voltage was applied. Simulation results of the triangularly connected network show good output characteristics since the output value corresponds to the correct digital representation of each analog input signal.

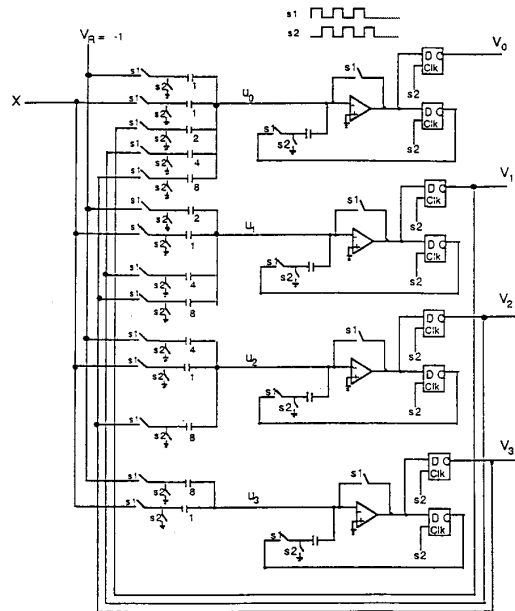


Fig. 7. The SC implementation for the triangular neural-based 4-bit A/D converter by means of multi-input Schmitt triggers.

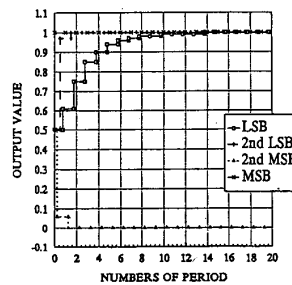


Fig. 8. The transient responses of the four amplifier outputs of the triangular 4-bit A/D converter by means of multi-input SC Schmitt triggers when $X = 11$.

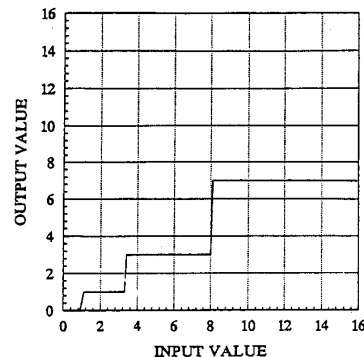


Fig. 9. Transfer characteristics of a symmetric 4-bit Hopfield A/D converter.

VII. CONCLUSION

This paper presents the development of an A/D conversion based on the triangularly connected Hopfield network. The

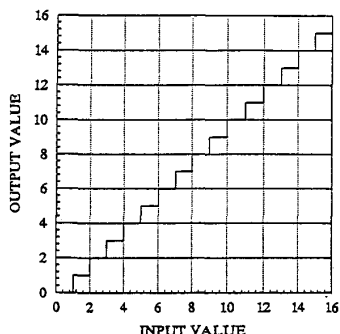


Fig. 10. Transfer characteristics of the triangular neural-based 4-bit A/D converter by means of multi-input Schmitt triggers.

novel technique has been developed to eliminate local minima involved in the original Hopfield neural-based A/D converter with a symmetric connection. Since the encoding with a unique global minimum energy function doesn't imply the correct encoding, the values of connection strengths and bias should be determined according to Cattermole's suggestions in order to guarantee the correctness of encoding. Section V shows that the network by means of switched-capacitor multi-input Schmitt triggers is identified as the cost-effective implementation for the lower triangular neural network. Results of simulation show that the speed of reaching a steady-state solution depends essentially on the system time constant. Moreover, it should result that the settling time of the more significant bit is faster than that of the lesser significant bit.

REFERENCES

- [1] J. J. Hopfield, "Neurons with graded response have collective computational properties like those of two-state neurons," *Proc. Natl. Acad. Sci., U.S.A.* vol. 81, pp. 3088-3092, 1984.
- [2] D. W. Tank and J. J. Hopfield, "Simple Neural Optimization network: An A/D converter, signal decision circuit, and a linear programming circuit," *IEEE Tran. on Circuit and Systems*, vol. 33, pp. 533-541, 1986.
- [3] B. W. Lee and B. J. Sheu, "Design of a Neural-based A/D Converter Using Modified Hopfield Network," *IEEE Tran. on Solid-State Circuits*, vol. 24, no. 4, August 1989.
- [4] G. Avitabile, M. Forti, S. Manetti and M. Marini, "On a Class of Nonsymmetric Neural Network with Application to ADC," *IEEE Tran. on Circuit and Systems*, vol. 38, pp. 202-208, 1991.
- [5] K. W. Cattermole, *Principles of Pulse Code Modulation*, London, England: Iliffe, 1969.
- [6] M. J. S. Smith and C. L. Portmann, "Practical design and analysis of a simple neural optimization circuit," *IEEE Trans. on Circuits and Systems*, vol. 36, pp. 42-50, Jan. 1989.
- [7] G. D. Cataldo and G. Palumbo, "A Theoretical Approach to the Design of A/D Converter by means of Schmitt Triggers," *IEEE Tran. on Circuits and Systems*, vol. 39, no. 2, pp. 126-129, Feb. 1992.
- [8] A. Rodriguez-Vazquez, R. Dominguez-Castro, A. Rueda, J. L. Huertas and E. Sanchez-Sinencio, "Nonlinear Switched-Capacitor 'Neural'

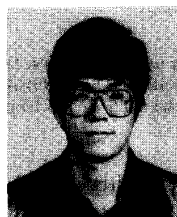
Networks for Optimization Problems," *IEEE Tran. on Circuit and Systems*, vol. 37, no. 3, March 1990.

- [9] R. Unbehauen and A. Cichocki, *MOS Switched-Capacitor and Continuous-Time Integrated Circuits and Systems*, Springer-Verlag, 1989.
- [10] Y. P. Tsvividis and D. Anastassiou *Switched-Capacitor Neural Networks*, Electronics Letters, 27th August 1987 vol. 23 no. 18
- [11] A. Rueda, J. L. Huertas and R. Dominguez-Castro, "Switched-Capacitor Neural Networks For Linear Programming," *Electronics Letters*, 14th April 1988 vol. 24, no. 8.



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