Appl Phys A (2013) 112:817–820
DOI 10.1007/s00339-013-7680-9

Applied Physics A
Materials Science & Processing

High performance IGZO/TiO_2 thin film transistors using Y_2O_3 buffer layers on polycarbonate substrate

H.H. Hsu · C.Y. Chang · C.H. Cheng

Received: 13 February 2013 / Accepted: 20 March 2013 / Published online: 29 March 2013

Abstract In this work, we fabricate IGZO TFT devices on flexible substrate at room temperature. The IGZO/TiO_2 TFT has small subthreshold swing of 0.16 V/dec, but suffers large gate leakage and negative threshold voltage. However, the TiO_2 TFT with Y_2O_3 buffer layers shows improved characteristics including a low threshold voltage of 0.55 V, a small sub-threshold swing of 0.175 V/decade and high field-effect mobility of 43 cm^2/Vs. Such good performance can be attributed to the enhanced capacitance density and lowered gate leakage owing to the integration of large band gap Y_2O_3 and low-temperature higher-κ TiO_2.

1 Introduction

The zinc oxide-based thin film transistors (TFTs) have been studied extensively due to its promising application on low-cost and large-area display. Furthermore, amorphous InGaZnO (α-IGZO) TFTs [1–11] present the potential for the fabrication of high drive current on plastic substrate after Nomura et al. reported the flexible TFTs using α-IGZO channel [1, 2]. Even so, currently developing flexible TFT still suffers large operating voltage and low device mobility. In addition to the above mentioned issues, low threshold voltage and small sub-threshold swing are also necessary for high speed operation. Fortunately, these transistor characteristics can be improved by modify the device process, such as IGZO composition, channel thickness, and high-κ gate dielectrics [12–14]. It is worth to note that high κ materials cannot have high dielectric constant (κ value) at room temperature (RT) process due to incomplete dielectric activation. The low κ value caused by high intrinsic defects and large leakage current cannot be overcome at room-temperature process, even adopting commercial dielectrics such as ZrO_2 ($\kappa \sim 18$) [15] and HfO_2 ($\kappa \sim 16$) [16]. However, a low thermal budget of $<300°C$ for TiO_2 annealing to reach a very high κ value of >50 has been demonstrated in MIM capacitors [17, 18]. To investigate the feasibility of the RT flexible device, we fabricated high performance IGZO TFT utilizing single-layer TiO_2 and trilayer $Y_2O_3/TiO_2/Y_2O_3$ on flexible substrate. The room-temperature-processed trilayer TFT can simultaneously achieve a small sub-threshold swing of 0.175 V/decade, a low threshold voltage of 0.55 V, and a high field-effect mobility of 43 cm^2/Vs under a drive voltage below 2 V.

2 Experiments

The TFT device was fabricated on the 300-nm thick insulating SiO_2 grown on a flexible PC (polycarbonate) substrate. A 35-nm-thick TaN bottom gate electrode was deposited by sputtering. Subsequently, the TiO_2 (56 nm and 112 nm) and $Y_2O_3/TiO_2/Y_2O_3$ (33 nm/30 nm/33 nm) were deposited using electron beam evaporation at room temperature. Such a physical vapor deposition with low thermal budget is preferred for the application of the gate dielectric stack, especially for ultrathin interface formation [19] or low-temperature flexible process [20]. Then the 25-nm thick IGZO active layers were deposited using radio frequency

H.H. Hsu · C.Y. Chang
Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan

C.H. Cheng (✉)
Department of Mechatronic Technology, National Taiwan Normal University, Taipei 106, Taiwan
e-mail: chcheng@ntnu.edu.tw
Fax: +886-2-23583074

(RF) sputtering from an IGZO target in a gas mixture with 30 % O_2. Finally, 300-nm thick Al was thermally evaporated to form source and drain metals where the channel size was 521 μm × 32 μm. The metal-insulator-metal (MIM) capacitors were also fabricated side-by-side to characterize the gate capacitance and leakage current. The deposited TiO_2 and Y_2O_3 and IGZO films were characterized by atomic force microscopy (AFM), transmission electron microscopy (TEM), and energy dispersive X-ray (EDX). The finished TFT devices were characterized by current–voltage (I–V) and capacitance–voltage (C–V) measurements using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter, respectively.

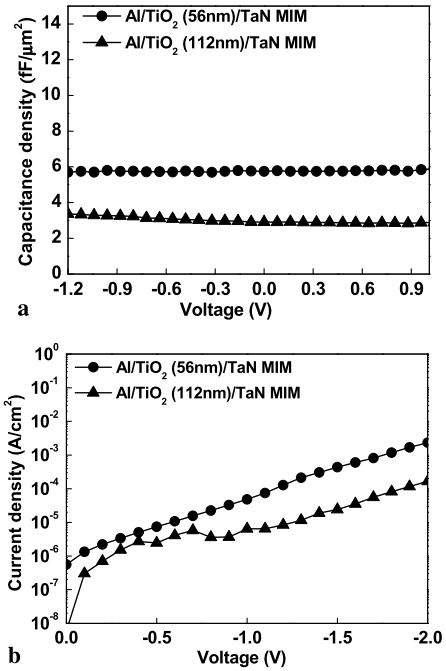
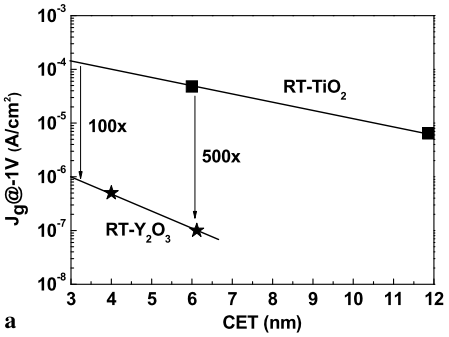


Fig. 1 C–V and I–V characteristics of Al/TiO_2/TaN MIM capacitors with 56-nm and 112-nm thick TiO_2 on flexible PC substrate

3 Results and discussion

Figure 1(a) and 1(b) show the capacitance–voltage (C–V) and current–voltage (I–V) characteristics of Al/TiO_2/TaN metal-insulator-metal (MIM) capacitors with different thicknesses. The capacitance densities of 5.7 fF/μm^2 and 2.9 fF/μm^2 at 100 kHz are obtained for 56-nm and 112-nm thick TiO_2 MIM capacitors, respectively. This means that the very high κ value of 38 can be extracted from these TiO_2 dielectrics processed at RT. The large gate capacitance density may benefit transistor characteristics especially for increasing drive current and lowering operation voltage. Besides, the leakage currents of 6.4×10^{-6} A/cm^2 and 4.8×10^{-5} A/cm^2 at −1 V are also measured for 56-nm and 112-nm thick TiO_2, respectively. The large gate leakage should be originated from oxygen vacancies in n-type TiO_2 with narrow band gap (3.05 eV) [21]. The reaction



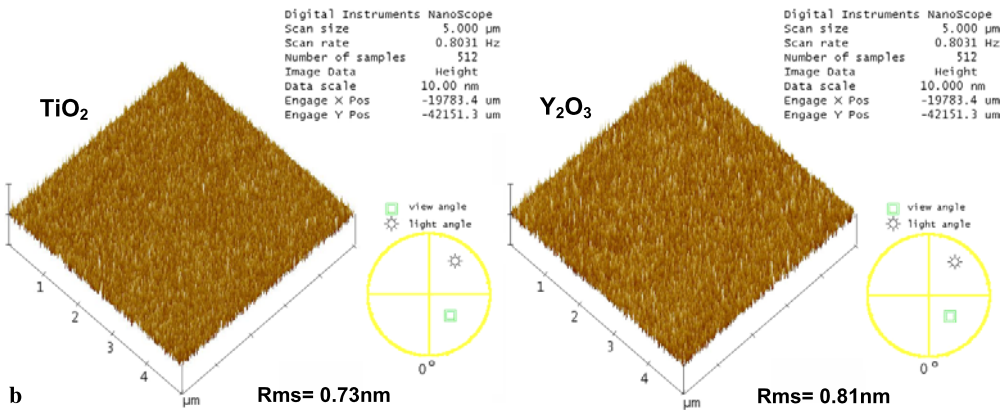
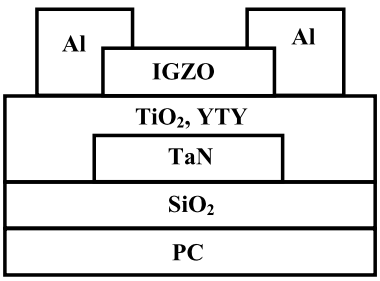


Fig. 2 (**a**) CET verse gate leakage (CET-J_g) characteristics of TiO_2 and Y_2O_3 MIM capacitors. (**b**) AFM images of TiO_2 and Y_2O_3 dielectrics on TaN substrate

equation is expressed as the following: $V^{2+}_{\text{Ti-Ox}} + 2e^- + \text{Ti–O}_x \rightarrow \text{Ti–O}^*_x$. Here, the $V^{2+}_{\text{Ti-Ox}}$ is the oxygen vacancy in RT-TiO_2, which is responsible for leakage paths under biasing. Although the intrinsic leakage issue can be further reduced by increasing dielectric thickness, this may scarify the capacitance density.

Figure 2(a) shows the plot of capacitance equivalent thickness (CET) versus gate leakage current for RT TiO_2 and Y_2O_3. The RT-processed Al/TiO_2 gate stacks show high gate leakage of $>10^{-4}$ A/cm^2 as the extrapolated CET scales down to 3 nm. However, the Y_2O_3 with large band gap of 6 eV [21] shows a leakage current of $<10^{-7}$ A/cm^2 at 6-nm CET that is 500× lower than that of TiO_2. Also, the gate leakage at −1 V for Y_2O_3 MIM capacitor still can maintain >2 orders of magnitude lower than that of TiO_2 one when the CET is continuously scaled down from 6 nm to 3 nm. In other words, the TiO_2 can reach higher κ value, yet leakage issue is not allowed for the low-power application. The introduction of Y_2O_3 is a powerful scheme for lowering off-state power, in contrast to single-layer TiO_2. In addition, it is preferred to have a flat gate stack to prevent bottom gate leakage from rough plastic substrate for flexible TFT application. From the AFM analysis shown in Fig. 2(b), the surface roughness (root mean square; Rms) for TiO_2 and Y_2O_3 dielectrics on TaN substrate are only 0.73 nm and 0.81 nm, respectively.

a



b

Fig. 3 (**a**) Photograph and (**b**) cross-sectional schematic structure of flexible and transparent IGZO TFTs using TiO_2 and YTY dielectrics

To perform a deep investigation on transistor characteristics, we fabricated flexible IGZO TFT using the TiO_2 and trilayer dielectric with Y_2O_3 buffer layers. The photograph and schematic structure of flexible and transparent IGZO TFT are shown in Fig. 3(a) and 3(b). Noteworthy is that the TFT characteristics can be controlled by the composition of the IGZO active layer. In Fig. 4, the corresponding EDX analysis of IGZO thin film confirms the presence of In, Ga, and Zn elements, where the composition ratio is close to that of sputter target. In addition to composition control of IGZO, the channel carrier concentration is also determined by oxygen vacancies in IGZO layer and thereby the oxygen concentration control is important for RT process.

The output I_d–V_d and transfer I_d–V_g characteristics of TiO_2 and Y_2O_3/TiO_2/Y_2O_3 (YTY) TFTs were shown in Fig. 5(a) and (b), respectively. The IGZO/TiO_2 TFT shows a small subthreshold swing of 0.16 V/decade and very low operating voltage of 1 V, but suffers small I_{on}/I_{off} ratio of $<10^4$ and negative threshold voltage of −0.3 V. This small subthreshold swing is ascribed to both interface charge density and high gate capacitance:

$$\text{Sub-threshold Swing} = \frac{KT}{q} \times \ln 10 \times \left(1 + \frac{C_{\text{dep}} + C_{\text{it}}}{C_{\text{HK}}}\right) \quad (1)$$

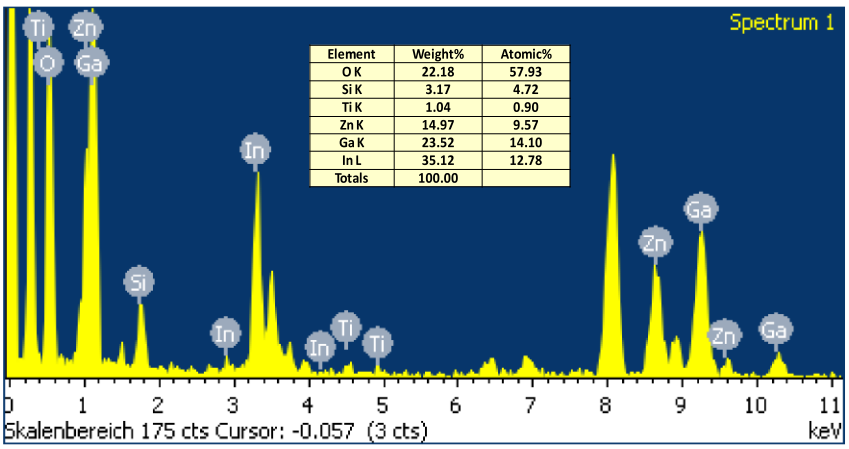


Fig. 4 EDX analysis of amorphous IGZO active layer

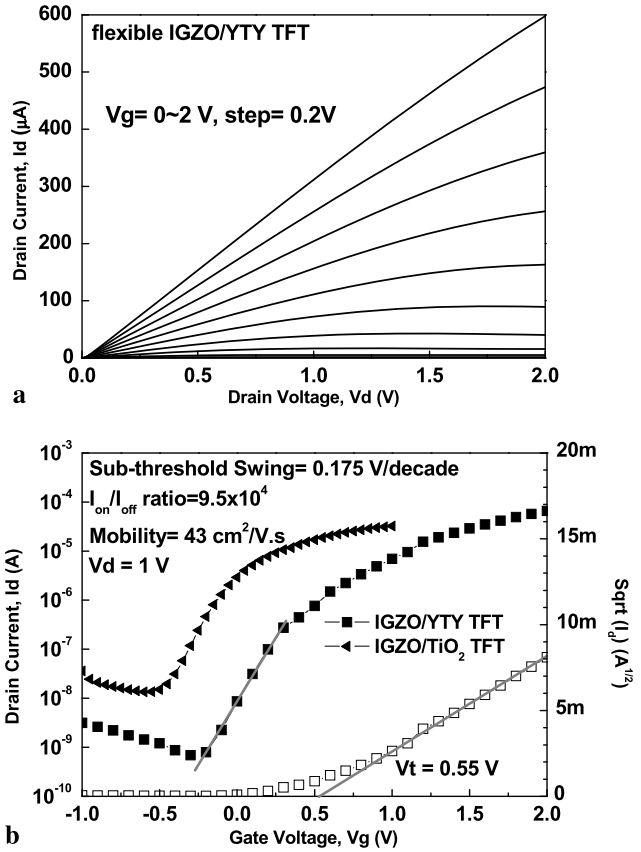


Fig. 5 (**a**) I_d–V_d and (**b**) I_d–V_g characteristics of flexible TFT devices using single-layer TiO_2 and trilayer structure with buffered Y_2O_3

where C_{dep} is the depletion capacitance density of α-IGZO, C_{it} is the capacitance density from charged interface traps and C_{HK} is the gate capacitance density. The high C_{HK} by using TiO_2 ($\kappa \sim 38$) may be useful to lower subthreshold swing. The high capacitance density is also supported by good CET scaling trend (Fig. 2(a)) that is favorable for reaching large drive current under the fabrication of RT TFT device.

To further improve device performance, the Y_2O_3 was used as buffer layer at the interfaces of IGZO/TiO_2 and TiO_2/TaN. From the measured results, the YTY TFT exhibits the improved performance including subthreshold swing of 0.175 V/decade, I_{on}/I_{off} ratio of 9.5×10^4, threshold voltage of 0.55 V and field-effect mobility of 43 cm^2/Vs. Such high mobility is also related to the amorphous structure of TiO_2 and Y_2O_3 with small surface roughness (Fig. 2(b)). Additionally, the small gate swing is further supported by low drive voltage (V_g–V_t) below 2 V, which is important for flexible display applications with a low operation power. The flexible RT TFT still exhibit a very high mobility that is comparable to Si-based IGZO TFT even without an additional passivation layer. From above experimental results, we can understand that a comprehensive consideration for gate stack process is very important to implement a fully-RT-fabricated flexible TFT.

4 Conclusion

The flexible IGZO/TiO_2 TFT using Y_2O_3 buffer layers shows a low threshold voltage of 0.55 V, a small subthreshold swing of 0.175 V/decade and a high field-effect mobility of 43 cm^2/Vs at a very low drive voltage of V_g–$V_t < 2$ V. This device has the potential for the application of high-speed low-power flexible ICs.

References

1. K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, H. Hosono, Science **300**, 1269 (2003)
2. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, Nature **432**, 488 (2004)
3. J.Y. Kwon, K.S. Son, J.S. Jung, T.S. Kim, M.K. Ryu, K.B. Park, B.W. Yoo, J.W. Kim, Y.G. Lee, K.C. Park, S.Y. Lee, J.M. Kim, IEEE Electron Device Lett. **29**, 1309 (2008)
4. J.K. Jeong, Y.-G. Mo, H.D. Kim, H.K. Chung, in *IEEE 21st Annual Meeting of the LEOS. Dig. 63* (2008)
5. P. Barquinha, L. Pereira, G. Goncalves, R. Martins, E. Fortunato, J. Electrochem. Soc. **156**, H161 (2009)
6. A. Suresh, P. Wellenius, J.F. Muth, IEDM Tech. Dig. **587** (2007)
7. S.I. Kim, C.J. Kim, J.C. Park, I. Song, D.H. Kang, H. Lim, S.W. Kim, E. Lee, J.C. Lee, Y. Park, IEDM Tech. Dig. **583** (2007)
8. C.J. Kim, D. Kang, I. Song, J.C. Park, H. Lim, S. Kim, E. Lee, R. Chung, J.C. Lee, Y. Park, IEDM Tech. Dig. **307** (2006)
9. P. Barquinha, A.M. Vila, G. Goncalves, L. Pereira, R. Martins, J.R. Morante, E. Fortunato, IEEE Trans. Electron Devices **55**, 954 (2008)
10. J.B. Kim, C. Fuentes-Hernandez, B. Kippelen, Appl. Phys. Lett. **93**, 242111 (2008)
11. H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, H. Hosono, Appl. Phys. Lett. **89**, 112123 (2006)
12. B.F. Hung, K.C. Chiang, C.C. Huang, A. Chin, S.P. McAlister, IEEE Electron Device Lett. **26**, 384 (2005)
13. M.F. Chang, P.T. Lee, S.P. McAlister, A. Chin, IEEE Electron Device Lett. **29**, 215 (2008)
14. M.F. Chang, P.T. Lee, S.P. McAlister, A. Chin, IEEE Electron Device Lett. **30**, 133 (2009)
15. J.S. Lee, S. Chang, S.M. Koo, S.Y. Lee, IEEE Electron Device Lett. **31**, 225 (2010)
16. K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, H. Hosono, Science **300**, 1269 (2003)
17. C.H. Cheng, S.H. Lin, K.Y. Jhou, W.J. Chen, C.P. Chou, F.S. Yeh, J. Hu, M. Huang, T. Arikado, S.P. McAlister, A. Chin, IEEE Electron Device Lett. **30**, 845 (2008)
18. G.D. Wilk, R.M. Wallace, J.M. Anthony, J. Appl. Phys. **89**, 5243 (2001)
19. W.B. Chen, C.H. Wu, B.S. Shie, Albert Chin, IEEE Electron Device Lett. **31**, 1184 (2010)
20. C.H. Cheng, F.S. Yeh, A. Chin, Adv. Mater. **23**, 902 (2011)
21. J. Robertson, J. Non-Cryst. Solids **303**, 94 (2002)