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Gate-first n-MOSFET with a sub-0.6-nm EOT gate stack

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A B S T R A C T

We report a self-aligned and gate-first TiLaO/La_2O_3 *n*-MOSFET with an equivalent oxide thickness (EOT) of 0.57 nm and low threshold voltage (V_t) of 0.3 V. The small EOT MOSFET can be reached using La-based interfacial layer with strong bond enthalpy (La–O, 799 kJ/mol) to suppress the formation of defect-rich low- interfacial layer and simultaneously block titanium atom inter-diffusion to avoid additional EOT increase. This gate-first low-EOT MOSFET exhibits the potential to integrate with current CMOS process.

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1. Introduction

To gain higher capacitance density and effectively decrease gate leakage, the TiO_2 dielectrics with very high κ value (>80) were proposed for realizing a sub-nm EOT metal-gate/high-κ CMOS [1–13]. However, its narrow bandgap and weak bond enthalpy (Ti–O, 672 kJ/mol) would lead to large gate leakage current and related reliability issue. A solution for solving this dilemma is to employ mixed TiO_2-based dielectrics with La_2O_3 doping [14], [15], but also suffer from thermal issue of Ti atom inter-diffusion that largely degrade EOT at current gate-first process. Although a thin SiO_2 interface layer have been used for 45 nm node technology with a 1 nm EOT [9], this scheme may not work when the EOT is scaled down to 0.6 nm due to the nature of SiO_2 with very low κ value. Since atom inter-diffusion between gate dielectric and Si substrate follows thermodynamics, it may be reduced by using lanthanide-based silicate with good thermal stability and high compatibility for gate-first process [5–8]. To address these issues, we employ the gate dielectric of high-κ TiLaO and compatible La_2O_3 interface layer with high bond enthalpy (799 kJ/mol) close to those of the SiO_2 (800 kJ/mol) and high-κ HfO_2 (802 kJ/mol) [3] for aggressive EOT scaling.

In this paper, the self-aligned *n*-MOSFETs with a small EOT was achieved using higher κ TiLaO and compatible La-based silicate layer to gain a high gate capacitance density and decrease leakage current at a scaled EOT, even with a conventional gate first process.

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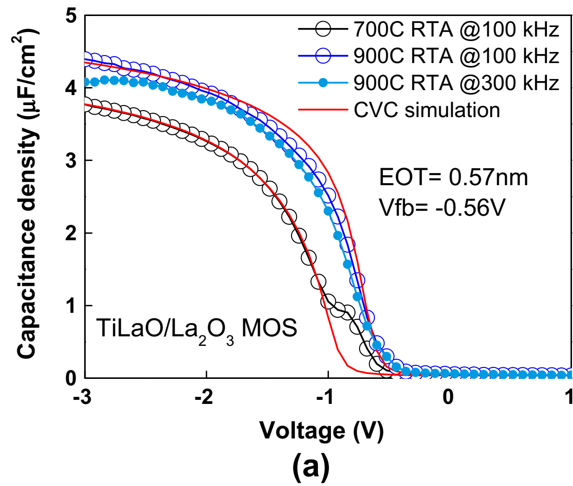
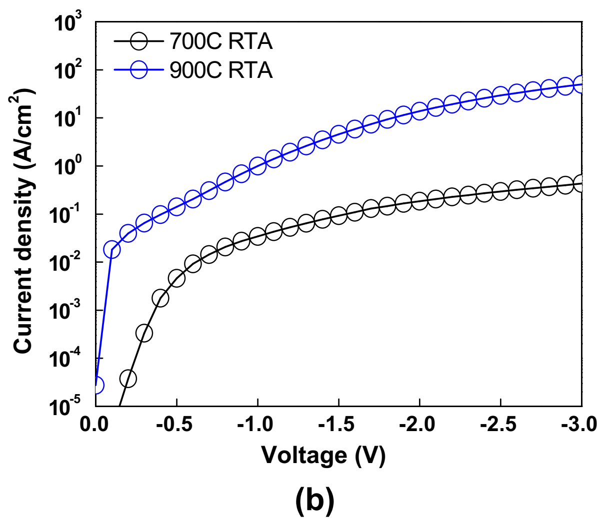
2. Experimental procedure

Standard p-type Si wafers were used in this study. The simple, self-aligned, gate-first TaN/TiLaO/La_2O_3 *n*-MOSFETs were made by depositing TiO_2-doped La_2O_3 on Si substrate using physical-vapor deposition, followed by a post-deposition anneal (PDA) of 400 °C. The adding TiO_2 in TiLaO increases the dielectric constant (κ value), which allows using a thicker layer to decrease the gate leakage current and still maintains the small EOT. Then 150-nm-thick TaN were subsequently deposited on these gate stacks and RTA annealed at 700–900 °C to form the MOS capacitors. For comparison, the same MOS process was also used to fabricate another TaN/TiLaO/[SiO_2 or $LaAlO_3$]/p-Si *n*-MOS capacitors. After patterning, self-aligned As^+ implantation for source-drain doping was applied and activated at 900 °C RTA. After etching non-reacted metal, Al contact metal was added on source-drain to form the *n*-MOSFETs with 10-μm × 100-μm size. The interface reaction was investigated by Transmission Electron microscopy (TEM). The fabricated *n*-MOSFETs were characterized by capacitance–voltage (*C–V*) and current–voltage (*I–V*) measurements. The EOT extractions of experimental *C–V* curves were well fitted by CVC simulators.

3. Results and discussion

Fig. 1(a) and (b) show the *C–V* and *J–V* curves of TaN/TiLaO/La_2O_3/p-Si *n*-MOS devices at various RTA temperatures. High capacitance density of 3.7 μF/cm^2 (extracted EOT = 0.65 nm by CVC simulation), negative V_{fb} of −0.85 V and leakage current of 3.4×10^{-2} A/cm^2 at −1 V were measured after 700 °C RTA, but anomalous hump in the depletion region indicates that it is associ-





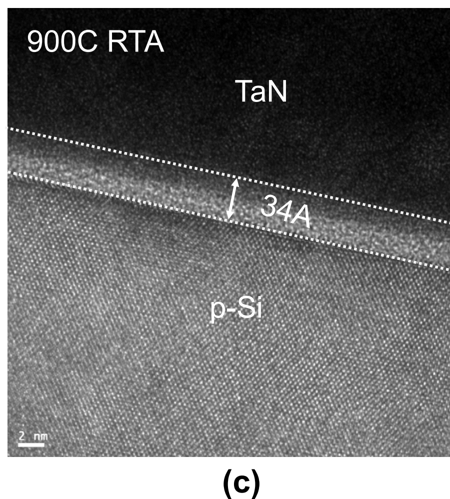
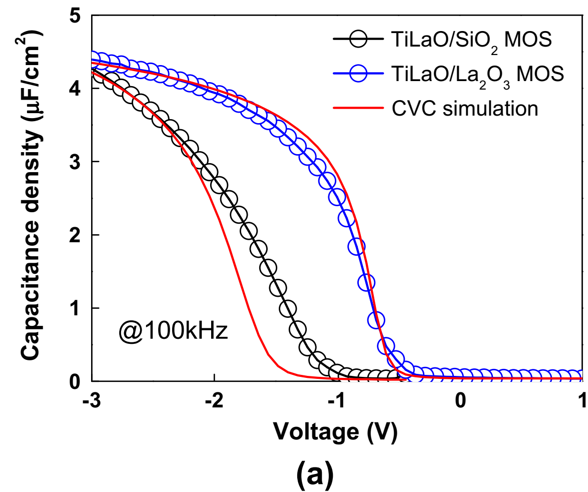


Fig. 1. (a) Capacitance (*C–V*), (b) leakage current (*J–V*) characteristics and (c) cross-sectional TEM picture (900 °C RTA) of TiLaO *n*-MOS capacitors.



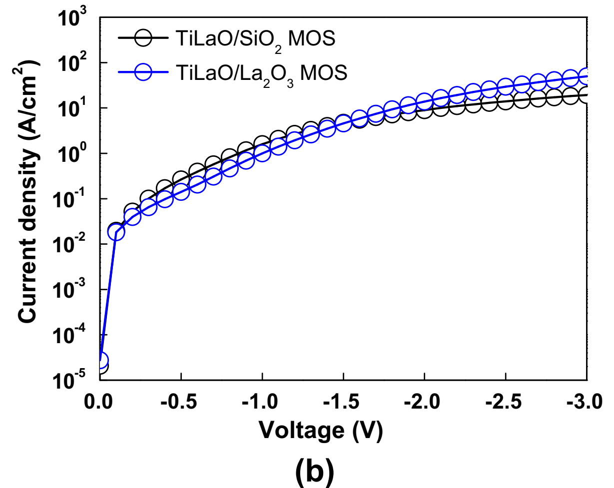


Fig. 2. (a) Capacitance (*C–V*) and (b) leakage current (*J–V*) characteristics of TiLaO/[La_2O_3 or $LaAlO_3$] *n*-MOS capacitors.

ated with high interface states due to the presence of silicon dangling bond defects. The interface defects lead to electron trapping and peak mobility reduction. Such interface silicate formation is unavoidable because of the bond enthalpy of La–O (799 kJ/mol), which is close to Si–O (800 kJ/mol) [3]. Fortunately, the interface quality can be further improved using a higher annealing temperature of 900 °C RTA. The well-behaved *C–V* curves at 900 °C RTA exhibit a very high capacitance density of 4.3 μF/cm^2 and low gate leakage current of 1 A/cm^2 at −1 V, which gives a small EOT of 0.57 nm. Furthermore, the frequency dispersion of *C–V* curves in accumulation is low where only 7% degradation in capacitance density can be observed in the range from 100 kHz to 300 kHz. As shown the TEM image of Fig. 1(c), the thickness of gate stack is about 3.4 nm where the calculated κ value is about 23. Both the increased capacitance density and negative V_{fb} shift from −0.85 to −0.56 V were observed with increasing thermal budget from 700 °C RTA to 900 °C RTA, indicating that the reduction of oxygen vacancies in TiLaO gate dielectric after 900 °C RTA and also means the formation of robust La-silicate interfacial layer at the same time. The high-density gate capacitance exhibits the aggressive scaled EOT of 0.57 nm and acceptable leakage density, which can be applied for 16 nm technology node with a EOT requirement of <0.6 nm.

Additionally, to evaluate thermal stability of lanthanum-based oxides as interface buffered layers at gate-first process, the $LaAlO_3$ dielectric with large bandgap and medium κ value close to La_2O_3

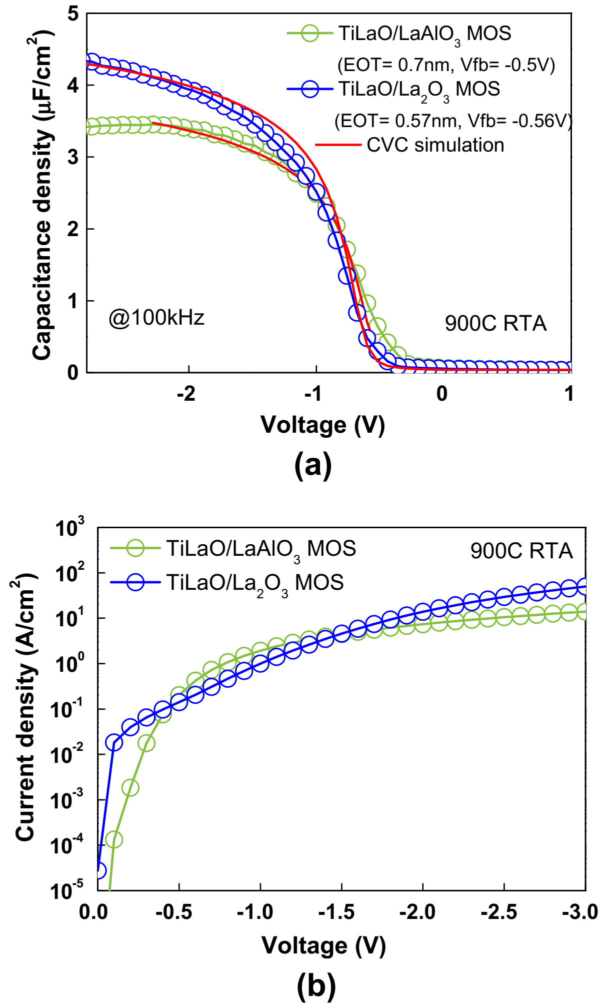


Fig. 3. (a) Capacitance (*C–V*) and (b) leakage current (*J–V*) characteristics of TiLaO/[La_2O_3 or SiO_2] *n*-MOS capacitors at close capacitance density.

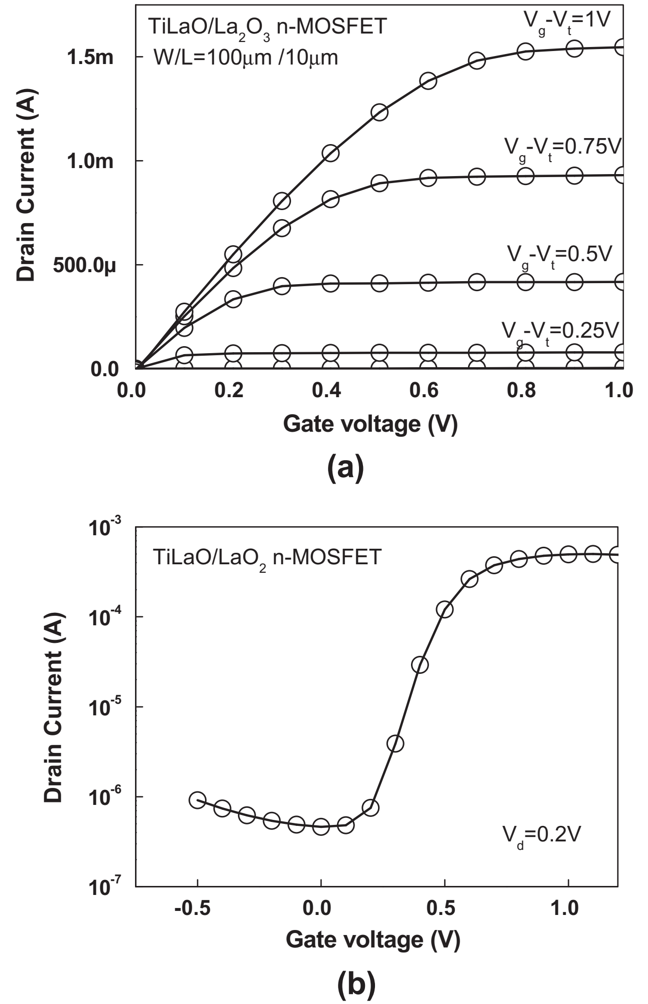


Fig. 4. (a) I_d–V_d and (b) I_d–V_g characteristics of TiLaO/La_2O_3 *n*-MOSFETs.

was integrated with higher-κ TiLaO gate stack. Fig. 2(a) and (b) show the *C–V* and *J–V* curves of TiLaO/[La_2O_3 or $LaAlO_3$] *n*-MOS devices after 900 °C RTA. Compared to TiLaO/La_2O_3 *n*-MOS capacitors, a lower capacitance density of 3.4 μF/cm^2 at a higher leakage current of 1.9 A/cm^2 at −1 V were observed in TiLaO/$LaAlO_3$ ones. According to these MOS results, the $LaAlO_3$ dielectric may have the potential for sub-nm EOT scaling, but ternary structure may face the issue of high temperature instability at a conventional gate-first process.

To further investigate the scaling limitation of traditional SiO_2 at sub-nm EOT CMOS, we also fabricated TiLaO/SiO_2 *n*-MOS devices with close capacitance densities for a performance comparison. Fig. 3(a) and (b) show the *C–V* and *J–V* curves of TiLaO/[La_2O_3 or SiO_2] *n*-MOS capacitors after 900 °C RTA. Although the measured gate leakage currents are similar for both MOS capacitors with close capacitance densities, we clearly observe a very negative V_{fb} of −1.4 V in TiLaO/SiO_2 *n*-MOS device. Such large negative V_{fb} shift is generally believed to be caused by high interface defects and positive charged charges in gate stack. Therefore, the thin SiO_2 buffered layer may not prevent from the formation of unstable Ti-rich silicate interface, resulting in the issues of large V_{fb} roll-off and peak mobility reduction at a high-temperature gate first process.

Fig. 4(a) and (b) show the I_d–V_d and I_d–V_g characteristics of TiLaO/La_2O_3 *n*-MOSFET. In addition to output transistor characteristics, this transistor featuring self-aligned-gate first process and sub-0.6-nm EOT presents a low V_t of 0.3 V. Fig. 5(a) shows the effective mobility derived directly from the I_d–V_g curves. A mobility of 103 cm^2/Vs at 0.8 MV/cm was obtained in TiLaO/La_2O_3 *n*-MOSFET with a 0.57-nm EOT. Besides, the gate leakage current at V_{fb} + 1 V can maintain >3 orders of magnitude lower than that of benchmark SiO_2 while EOT scaling from 1 nm to 0.57 nm, as shown in Fig. 5(b). Such low EOT and V_t can be attributed to the unique negative V_{fb} of La_2O_3 dielectric and robust compatible La-silicate with high bond enthalpy. However, the mobility degradation at small sub-0.6-nm EOT is unavoidable due to a combined effect of remote charge scattering from charged defects in high-κ dielectric and remote phonon scattering [16–18]. Further mobility improvement can be expected in narrow-fin 3D FinFET devices with the integration of high-κ/metal-gate technology.

4. Conclusions

Using a simple self-aligned and gate-first process, we have demonstrated TiLaO/La_2O_3 *n*-MOSFET with a low 0.57 nm EOT and V_t of 0.3 V. This device showed the potential to reach the requirement of sub-0.6-nm EOT for 16 nm technology node.

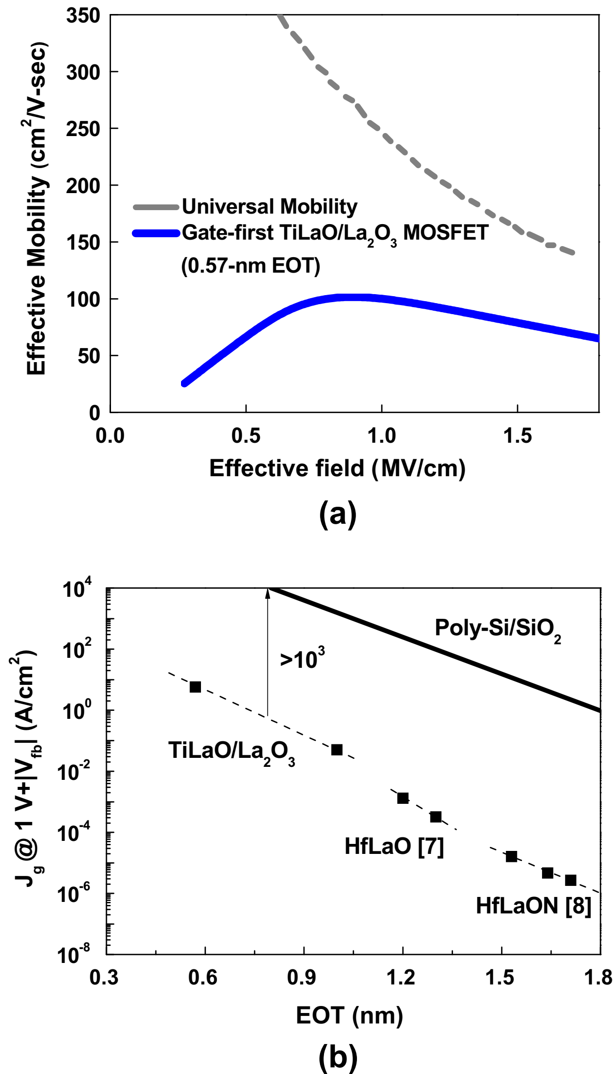


Fig. 5. (a) Electron mobility and (b) EOT verse gate leakage (EOT-Jg) characteristics of TiLaO/La_2O_3 *n*-MOSFETs.

References

[1] H.-H. Tseng, C.C. Capasso, J.K. Schaeffer, E.A. Hebert, P.J. Tobin, D.C. Gilmer, D. Triyoso, M.E. Ramón, S. Kalpat, E. Luckowski, W.J. Taylor, Y. Jeon, O. Adetutu, R.I. Hegde, R. Noble, M. Jahanbani, C. El Chemali, B.E. White, IEDM Tech. Dig. (2004) 821–824.

[2] T. Nabatame, M. Kadoshima, K. Iwamoto, N. Mise, S. Migita, M. Ohno, H. Ota, N. Yasuda, A. Ogawa, K. Tominaga, H. Satake, A. Toriumi, IEDM Tech. Dig. (2004) 83–86.

[3] D.S. Yu, Albert Chin, C.H. Wu, M.-F. Li, C. Zhu, S.J. Wang, W.J. Yoo, B.F. Hung, S.P. McAlister, IEDM Tech. Dig. (2005) 649–652.

[4] C.H. Wu, D.S. Yu, IEEE Electron Device Lett. 27 (2006) 90–92.

[5] X.P. Wang, C. Shen, M.-F. Li, H.Y. Yu, Y. Sun, Y.P. Feng, A. Lim, H.W. Sik, A. Chin, Y.C. Yeo, P. Lo, D.L. Kwong, Symp VLSI Tech. Dig. (2006) 12–13.

[6] C.H. Wu, B.F. Hung, Albert Chin, S.J. Wang, X.P. Wang, M.-F. Li, C. Zhu, Y. Jin, H.J. Tao, S.C. Chen, M.S. Liang, IEDM Tech. Dig. (2006) 617–620.

[7] C.F. Cheng, C.H. Wu, N.C. Su, S.J. Wang, S.P. McAlister, Albert Chin, IEDM Tech. Dig. (2007) 333–336.

[8] C.C. Liao, Albert Chin, N.C. Su, M.-F. Li, S.J. Wang, Symp VLSI Tech. Dig. (2008) 190–191.

[9] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren0, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, K. Zawadzki, IEDM Tech. Dig. (2007) 247–250.

[10] M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta, Y. Watanabe, K. Iwamoto, S. Migita, N. Yasuda, H. Ota, T. Nabatame, A. Toriumi, IEDM Tech. Dig. (2007) 523–526.

[11] S. Datta, G. Dewey, M. Doczy, B.S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, R. Chau, IEDM Tech. Dig. (2003) 653–656.

[12] W. Tsai, L. -Å Ragnarsson, L. Pantisano, P.J. Chen, B. Onsia, T. Schram, E. Cartier, A. Kerber, E. Young, M. Caymax, S. De Gendt, M. Heyns, IEDM Tech. Dig. (2003) 311–314.

[13] S.H. Lin, S.L. Liu, F.S. Yeh, IEEE Electron Device Lett. 30 (2009) 75–77.

[14] S.H. Lin, C.H. Cheng, W.B. Chen, F.S. Yeh, C.P. Chou, S.P. McAlister, IEEE Electron Device Lett. 30 (2009) 999–1001.

[15] C.H. Cheng, H.C. Pan, H.J. Yang, C.N. Hsiao, C.P. Chou, S.P. McAlister, Albert Chin, IEEE Electron Device Lett. 28 (2007) 1095–1097.

[16] L.-A. Ragnarsson, Z. Li, J. Tseng, T. Schram, E. Rohr, M.J. Cho, T. Kauerauf, T. Conard, Y. Okuno, B. Parvais, P. Absil, S. Biesemans, T.Y. Hoffmann, IEDM Tech. Dig. (2009) 663–666.

[17] J. Huang, D. Heh, P. Sivasubramani, P.D. Kirsch, G. Bersuker, D.C. Gilmer, M.A. Quevedo-Lopez, M.M. Hussain, P. Majhi, P. Lysaght, H. Park, N. Goel, C. Young, C.S. Park, C. Park, M. Cruz, V. Diaz, P.Y. Hung, J. Price, H.-H. Tseng, R. Jammy, Symp VLSI Tech. Dig. (2009) 34–35.

[18] K. Choi, H. Jagannathan, C. Choi, L. Edge, T. Ando, M. Frank, P. Jamison, M. Wang, E. Cartier, S. Zafar, J. Bruley, A. Kerber, B. Linder, A. Callegari, Q. Yang, S. Brown, J. Stathis, J. Iacoponi, V. Paruchuri, V. Narayanan, Symp VLSI Tech. Dig. (2009) 138–139.