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Mobility model extraction for surface roughness of SiGe along (110) and (100) Orientations in HKMG bulk FinFET devices

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ABSTRACT

In this work, the FinFET HKMG MOS devices are fabricated on silicon wafer with *p*-substrate. The interface roughness between the SiGe and SiO_2 is experimentally extracted and calculated as a function of root mean square by analysis of high resolution transmission electron microscopy. The surface-roughness dependent mobility model is then incorporated into device simulation to study the mobility of SiGe along (110) and (100) orientations of the devices. We further analyze four devices with different surface roughness along (100) and (100) orientations to demonstrate the influence of surface roughness on the total effective mobility.

1. Introduction

MOS devices scaling is being continued and requires an ultimate thin gate dielectric [1]. In such devices, high mobility alternative channels have been researched to continue on the high performance roadmap, where highly scaled Si channel CMOS has faced various limitations. SiGe, the high mobility channels, potentially provide high injection velocity to achieve projected high performance metrics [2].

Various mobility models of SiGe can reasonably fit the measured dependence of effective mobility on doping concentration and bias in the inversion layer; however, for the FinFET HKMG MOS devices, there are few mobility models that considering the influence of surface roughness between the SiGe and SiO_2. In this work, we fabricate FinFETs on silicon wafer with *p*-substrate and measure the interface roughness between the SiGe and SiO_2 by using high resolution transmission electron microscopy (HRTEM). The influence of surface roughness is then modelled as the spatial parameters of the surface, where the correlation length L and the surface roughness Δ are calculated as a function of root mean square. The surface-roughness dependent mobility model is incorporated into device simulation for SiGe along (110) and (100) orientations of the devices. Four devices with different surface roughness along (100) and (100) orientations are further designed and simulated to show the influence of surface roughness on the total effective mobility.

2. Experiment and extraction

We fabricate the HKMG bulk FinFET on a *p*-substrate, where the advanced 193 nm immersion lithography and optimized etching processes are utilized for SiGe fin and STI formation [3,4]. The photo resistance layer is removed by $HBrO_2$ plasma, the silicon nitride is then etched by $CF_4 + CH_2F_2$ and silicon is etched by $HBrCl_2 + He–O_2$. SiGe is deposited by atomic layer deposition; 2-nm chemical oxide and 3-nm HfO_3 film are deposited by chemical vapor deposition. Finally, we use sputter to form an 8-nm-thick TiN film [5]. To get the two different kinds of surface roughness, the two clean processes are proposed in this experiment; the SAMPLE A is used by HF 100:1 40 s, and NH_4OH 150 s + HF 100:1 40 s clean treatment is used on the SAMPLE B. The HRTEM photos of the fabricated SAMPLE A and the SAMPLE B are shown in Figs. 1 and 2.

The spatial parameters of the surface, the correlation length L and the surface roughness Δ are then calculated [6]. The calculated root mean square surface nano-roughness of the SAMPLE A is 3.37 Å on (110) and 3.04 Å on (100). Their maximum is 6.15 Å and 4.05 Å, respectively. However, the result of the SAMPLE B is 1.59 Å on (110) and 2.11 Å on (100). Their maximum is 2.58 Å and 3.38 Å, respectively, as shown in Table 1. Thus, we further design four different devices with different surface roughness according to the results of the SAMPLE A and SAMPLE B for the device simulation. The simulation device 1 is with the same Δ and L as

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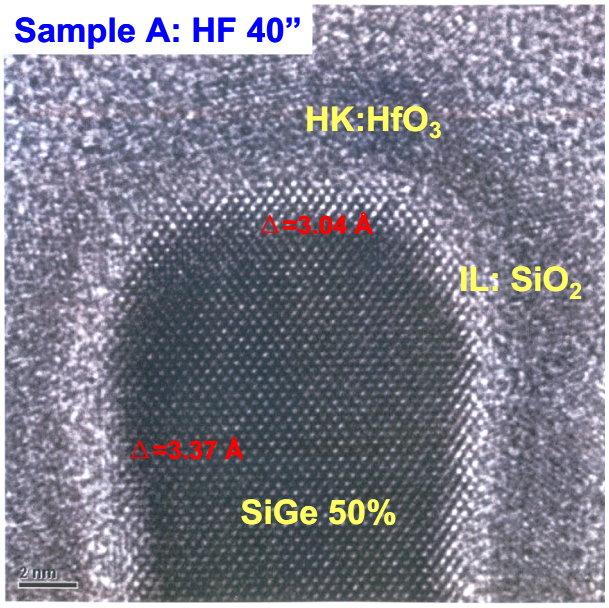

Fig. 1. The HRTEM of the Sample A with the HF 40 s clean treatment on the interface between SiGe and SiO_2 film. The calculated root mean square surface nano-roughness is 3.37 Å on (110) and 3.04 Å on (100). Their maximum is 6.15 Å and 4.05 Å, respectively.

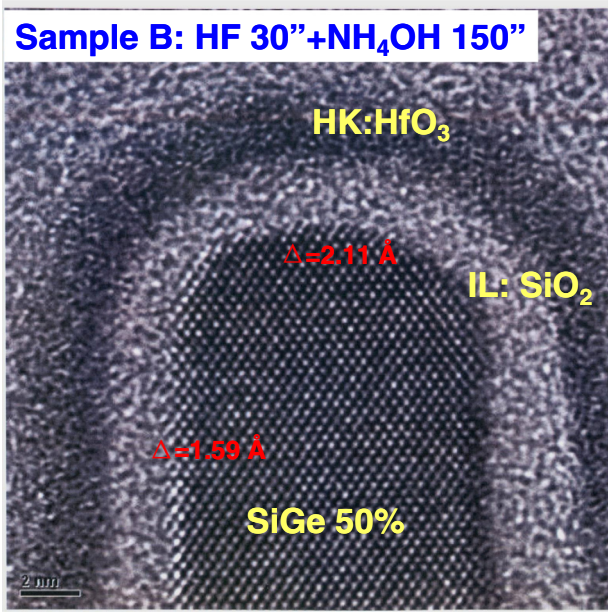

Fig. 2. The HRTEM of the Sample B with the HF 30 s and NH_4OH 150 s clean treatment on the interface between SiGe and SiO_2 film. The calculated root mean square surface nano-roughness is 1.59 Å on (110) and 2.11 Å on (100). Their maximum is 2.58 Å and 3.38 Å, respectively.

the SAMPLE A. The simulation device 4 is with the same Δ and L as the SAMPLE B. The simulation device 2 is with the same Δ and L as the SAMPLE A on (100) and as the SAMPLE B on (110). The simulation device 3 is with the same Δ and L as the SAMPLE B on (100) and as the SAMPLE A on (110).

3. Results and discussion

To evaluate the carrier's mobility, we use the Mathiessen's rule that approximates the total mobility [7,8], at low longitudinal field as the sum of three terms, as expressed in Eq. (1)

Table 1
Surface roughness delta and correlation length of the Sample A and the Sample B. The simulation device 1 is with the same Δ and L as the Sample A. The simulation device 4 is with the same Δ and L as the Sample A. The simulation device 2 is with the same Δ and L as the Sample A on (100) and as the Sample B on (110). The simulation device 3 is with the same Δ and L as the Sample B on (100) and as the Sample A on (110).

Surface orientation	(100)		(110)	
Sample				
	Δ (Å)	L (Å)	Δ (Å)	L (Å)
A	3.04	10.80	3.37	11.10
B	2.11	10.76	1.59	10.76
Simulated				
Device 1	A		A	
Device 2	A		A	
Device 3	B		B	
Device 4	B		B	

$$\frac{1}{\mu_{\text{total}}} = \frac{1}{\mu_{\text{ph}}} + \frac{1}{\mu_{\text{co}}} + \frac{1}{\mu_{\text{sr}}}, \tag{1}$$

where the μ_{ph} is the phonon limited mobility, the μ_{co} is the Coulomb limited mobility, and the μ_{sr} is the surface limited mobility. For the devices at the high field, for example, $E_{\text{eff}} > 0.8$ MV/cm, the surface roughness mobility decreases with increasing the surface roughness. The mobility contribution attributed to surface roughness scattering is given by Eq. (2), where F is the transverse electric field normal to SiGe–SiO_2 interface and the F_{ref} is a reference field [9–11]. Table 2 lists the parameters used in the device simulation.

$$\mu_{\text{sr}} = \left[\frac{(F_{\perp}/F_{\text{ref}})^{A^*}}{\delta} + \frac{F_{\perp}^3}{\eta}\right]^{-1}. \tag{2}$$

At low temperature and high normal electric field, the surface roughness scattering is known to strongly degrade the surface mobility, and it is also strongly dependent on the detail of technology, as Eq. (3), where the δ is a constant that depends on the details of the fabrication technology, such as the oxide growth conditions, the crystal orientation, and so on; therefore, we can correct the parameter by the extracted surface roughness, as Eq. (4) in the device simulation.

$$\mu_{\text{sr}}(E_{\perp}) = \frac{\delta}{E_{\perp}^2}. \tag{3}$$

$$\delta \propto (\Delta \cdot L)^{-2}. \tag{4}$$

As shown in Fig. 3, the plot of the total mobility μ_{total} vs. E_{eff} is the simulation results on the SiGe channel. The total mobility is decreased when the strength of applied electric field is increased. The total mobility the along (100) orientation is higher than that of (100) orientation, but the degradation of mobility versus the strength of applied electric field along (100) orientation is larger

Table 2
The used mobility model parameters.

Parameter	Electrons	Holes	Units
B	3.61E + 07	1.51E + 07	cm/s
C	1.70E + 04	4.18E + 03	$cm^{5/3}/(sV^{2/3})$
τ	0.0233	0.0119	1
κ	1.7	0.9	1
δ	3.58E + 18	4.10E + 15	V/s
A	2.58	2.18	1
α	6.85E-21	7.82E-21	1
ν	0.0767	0.123	1
η	5.82E + 30	2.05E + 30	$V^2/(cm^*s)$
κ	1.7	0.9	1

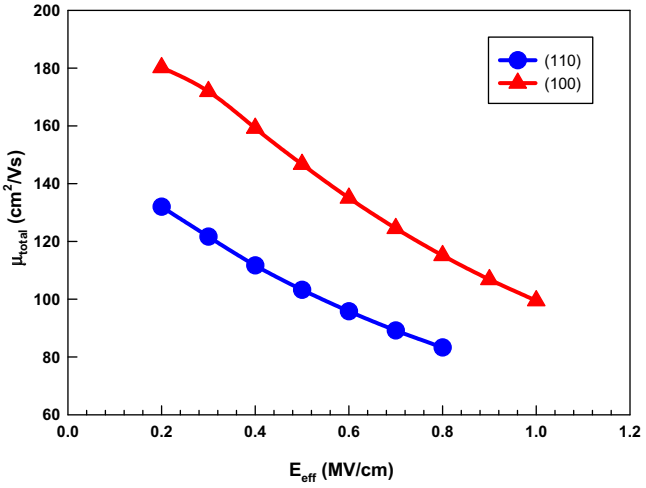

Fig. 3. The simulation results of the electron mobility vs. E_{eff} on SiGe. Red spot line is (100) and blue spot line is (110).

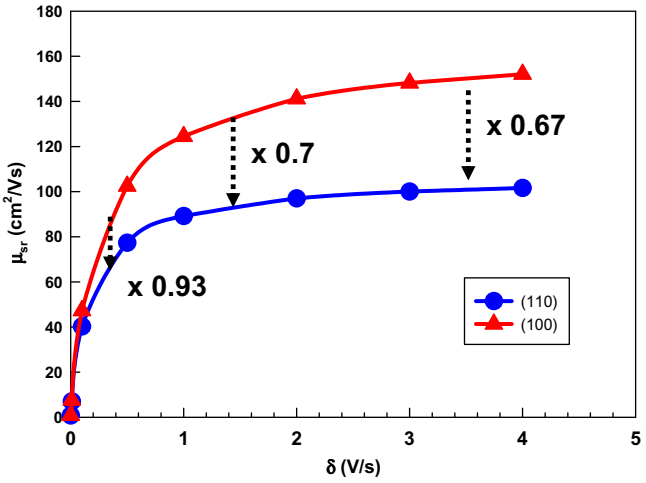

Fig. 4. The simulation results of the electron mobility vs. δ on SiGe. Red spot line is (100) and blue spot line is (110).

than that of (110) orientation. The red spot line is the (100) orientation and the blue spot line is the (110) orientation. Fig. 4 shows the simulation result of the surface limited mobility vs. the δ, defined in Eq. (4), on the SiGe channel, where the red spot line is (100) and the blue spot line is (110). When the δ approaches to zero, the device has largest surface roughness thus the device has the lowest μ_{sr}. When the δ increases (i.e., the surface roughness is reduced), the device attains its largest μ_{sr}. for (110) and (100) orientations. Notably, the mobility along (110) orientation has 93–67% degradations, as marked in Fig. 4, to (100) orientation when the δ increases. Fig. 5 indicates the simulated result of the electron mobility. The results of the designed four devices indicate the simulation device 2 and the simulation device 4 have higher mobility than those of the simulation device 1 and the simulation device 3 due to the surface roughness on (110) dominates the carrier's transport. Notably, the silicon fin height along the orientation of (110) is the major weight of the device's effective width.

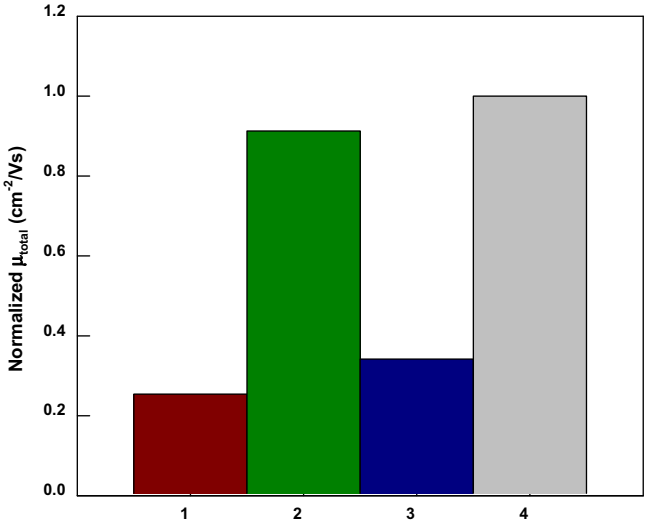

Fig. 5. The normalized μ_{total} with respect to the μ_{total} of the simulation device 4. The simulation device 2's μ_{total} is comparable with to the mobility of the simulation device 4. The mobility of the simulation device 1 and the simulation device 3 is dropped due to their large surface roughness.

4. Conclusions

In this study, we have extracted SiGe/SiO_2 interface roughness along different orientations and modeled the corresponding mobility of the HKMG bulk FinFETs. The parameters of the surface roughness mobility model have been incorporated into device simulation. The influence of surface roughness on the total effective mobility has been demonstrated and the surface roughness along the SiGe surface (110) limits the total effective mobility.

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