

# Realizations of High-Order Switched-Capacitor Filters Using Multiplexing Technique

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**Abstract**—A new SC design methodology using multiplexing technique is proposed to realize arbitrary high-order filters. In this methodology, the filter transfer function is transformed as the combination of biquads and their outputs are computed sequentially by the multiplexing SC biquad circuit. Four basic function SC circuits are introduced and a filter can be implemented by various combinations of these circuits. This makes the proposed method more versatile and practical. Because of the efficient use of multiplexing techniques, the realized high-order filters have less op-amps, switches, and capacitors, and thus small chip area, but at the cost of increasing clock phases. An eighth-order Butterworth low-pass filter design example is presented to demonstrate how to apply the proposed method to the design of high-order filters. Moreover, an eighth-order low-pass filter has been designed and fabricated in 1.2  $\mu\text{m}$  CMOS double-poly double-metal process. Both computer simulation and experimental results have successfully verified the function correctness and the performance of the proposed design method.

## I. INTRODUCTION

SWITCHED-CAPACITOR (SC) technique has been widely applied to the design of analog sampled-data filters. In the conventional design method of SC filters [1]–[3], the number of operational amplifiers (op-amps) is proportional to the order of the realized transfer functions. Thus the realization of high-order filters requires large chip area and power dissipation. Moreover, the noise generated by the op-amps is also increased. To solve this problem, the number of op-amps in SC filters has to be reduced. In this approach, a few new design methods have been proposed [4]–[7]. The recent work [4] has demonstrated a multiplexing scheme which uses any number of op-amps, from 1 to  $N$ , to realize an arbitrary  $N$ th-order filter function. The design method is to use the noninverting stray-insensitive integrator [8] and the multiplexing technique to implement the state-space equations of the form

$$(z-1)\mathbf{X} = \mathbf{A}\mathbf{X} + \mathbf{b}u$$

$$y = \mathbf{c}^T\mathbf{X} + du$$

where the matrices  $\mathbf{A}$ ,  $\mathbf{b}$ ,  $\mathbf{c}$ , and  $d$  are constants,  $\mathbf{X}$  is the state variable,  $u$  is the input,  $y$  is the output, and  $z$  is the  $z$ -transform operator. Although the structure can obtain a very significant op-amp number reduction, it still has some

disadvantages. The major disadvantage is mentioned below. The number of capacitors and switches used in this SC circuit is mainly proportional to the number of nonzero coefficients in the  $N \times N$  matrix  $\mathbf{A}$ . However, in order to obtain low capacitor ratio, low sensitivity, and wide dynamic range, the matrix  $\mathbf{A}$  must be chosen so that the number of nonzero elements in  $\mathbf{A}$  is as many as possible. Therefore, the components in the realized SC circuit become numerous and the layout routing becomes complicated. This may offset the chip area reduction gained from the reduced op-amp count.

In this paper, a new design method to implement arbitrary high-order filter functions is proposed. In the proposed method, the multiplexed SC differentiators and integrators are used as the building blocks. As the order of the filter transfer function increases, the number of op-amps used in the SC filter is fixed and the number of clock phases increases. The resulting circuit architecture is flexible and the number of capacitors and switches used in the circuit is only proportional to the order of filter function. Therefore, the entire circuit is not very complex and the efficient layout can be achieved easily.

The concept of the proposed design method is to transform the transfer function of the high-order filter into a cascade of second-order transfer functions and use a multiplexing SC circuit to compute the outputs of these second-order transfer functions sequentially and realize the desired high-order transfer functions. Therefore, due to the efficient use of the multiplexing technique, fewer components can be used to implement high-order filters. The discrete-time theory of this design method is described in Section II. According to this methodology, four basic functions are defined. The SC circuits to implement these functions are also presented in Section II. By using these basic building blocks, the high-order filters can be implemented. In Sections III and IV, a general high-order low-pass filter and design examples have been used to demonstrate how to use the basic functions to implement high-order filters, respectively. The experimental results to verify the performance of the proposed new structures are described in Section V. Finally, the conclusion is given.

## II. DESIGN METHODOLOGY

### A. Discrete-Time Theory

The  $z$ -domain transfer function of an arbitrary  $M$ th-order discrete-time linear system can be described as

$$H(z) = \frac{Y(z)}{U(z)} = \frac{\sum_{j=0}^M \beta_j z^{-j}}{1 + \sum_{i=1}^M \alpha_i z^{-i}} \quad (1)$$

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where  $\alpha_i$  and  $\beta_j$  are constant coefficients,  $U(z)$  is the  $z$ -transform of the input sequence  $u[m]$ ,  $Y(z)$  is the  $z$ -transform of the output sequence  $y[m]$ , and  $m$  is an integer. Applying the mathematical technique, the above equation can be transformed into the product of  $N$  second-order transfer functions (biquads) where  $N = \lfloor (M + 1)/2 \rfloor$  is the largest integer of  $(M + 1)/2$ . This is given by

$$H(z) = \prod_{i=1}^N \frac{D_i + E_i z^{-1} + F_i z^{-2}}{1 + B_i z^{-1} + C_i z^{-2}} \quad (2)$$

where  $B_i$ ,  $C_i$ ,  $D_i$ ,  $E_i$  and  $F_i$  are constant coefficients. Therefore, this linear system can be considered as a cascade of  $N$  biquads, shown in Fig. 1(a). Assume that  $\mathbf{P}_0(z) = U(z)$  represents the  $z$ -transform of the input sequence of the first biquad in the linear system.  $\mathbf{P}_N(z) = Y(z)$  represents the  $z$ -transform of the output sequence of the  $N$ th biquad in the linear system.  $\mathbf{P}_i(z)$ ,  $1 \leq i \leq N - 1$ , represents the  $z$ -transform of the output sequence in the  $i$ -th biquad which is also the input sequence in the  $(i + 1)$ th biquad under the multiplexing operation. Actually,  $\mathbf{P}_0(z)$  is the system input,  $\mathbf{P}_N(z)$  is the system output, and  $\mathbf{P}_i(z)$  is the intermediate outputs of the system. By using  $\mathbf{P}_i(z)$ , (2) can be rewritten as

$$H(z) = \prod_{i=1}^N \frac{\mathbf{P}_i(z)}{\mathbf{P}_{i-1}(z)} \quad (3)$$

where

$$\frac{\mathbf{P}_i(z)}{\mathbf{P}_{i-1}(z)} = \frac{D_i + E_i z^{-1} + F_i z^{-2}}{1 + B_i z^{-1} + C_i z^{-2}}. \quad (4)$$

To implement (3) with less hardware, the multiplexing technique is applied to the computation of each of the biquad outputs sequentially. The block diagram of such a multiplexing system is shown in Fig. 1(b), and its output sequence is defined as

$$Q[n] \equiv P_i[m], \quad n = m(N + 1) + i, \quad 0 \leq i \leq N \quad (5)$$

where the sampling period  $T_x$  of  $Q[n]$  is  $1/(N + 1)$  times the sampling period  $T_t$  of  $P_i[m]$ , and  $P_i[m]$  is the inverse  $z$ -transform of  $\mathbf{P}_i(z)$ . The operation to compute the desired system output can be divided into two steps: 1) setting the initial condition and 2) computing each of the biquad outputs sequentially in every  $T_t$  period following the first step. Both steps are explained as follows.

*Initialization Step:* During the clock phase  $T$ , i.e.,  $n = m(N + 1)$ , the multiplexing system is initialized with the new system input values. At this time, the output of the multiplexing system is set as

$$Q[n] = P_0[m] = u[m].$$

Through the initialization step, the associated data stored in this system is updated.

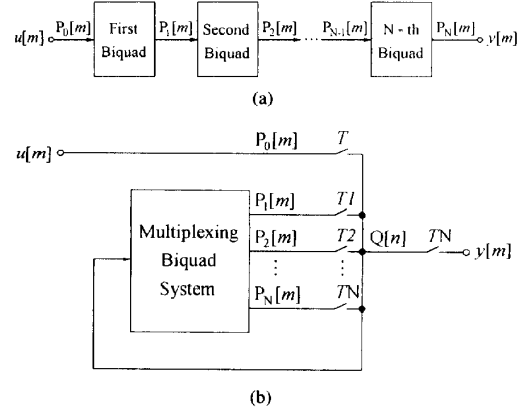


Fig. 1. (a) A cascade of  $N$  biquad systems to realize a high-order transfer function in (1). (b) A multiplexing system to compute the outputs of  $N$  biquads sequentially and realize the high-order transfer function.

*Computation Step:* During clock phases  $T1$  to  $TN$ , i.e.,  $n = m(N + 1) + i$  and  $1 \leq i \leq N$ , the multiplexing system produces the outputs of the  $N$  biquads. Applying the inverse  $z$ -transform to (4) and substituting  $P_i[m]$  by  $Q[n]$ , it can be transformed into

$$Q[n] = -B_i Q[n - N - 1] - C_i Q[n - 2N - 2] + D_i Q[n - 1] + E_i Q[n - N - 2] + F_i Q[n - 2N - 3]. \quad (6)$$

By using (6), the desired output can be calculated.

## B. Realization of Four Basic Functions

To develop the multiplexing system described above, the most important thing is to implement the multiplexing biquad system for the computation step. According to (6) and the general SC design method, four basic functions are defined to realize this system. These functions and their realization are described below. As to the initialization step, it can be implemented by adding some capacitor branches to the multiplexing biquad system circuit to set the required initial values.

*Slow Multiplexed Differentiator:* The relationship between the input sequence  $Q[n]$  and output sequence  $w_{D_i}[n]$  of the slow multiplexed differentiator is defined as

$$w_{D_i}[n] \equiv \begin{cases} 0, & n = m(N + 1) \\ h_{D_i}^i D_t \{Q[n]\}, & n = m(N + 1) + i, 1 \leq i \leq N \end{cases} \quad (7)$$

where

$$D_t \{Q[n]\} \equiv Q[n] - Q[n - N - 1] = P_i[m] - P_i[m - 1] \text{ and } h_{D_i}^i \leq 0.$$

The above equation is similar to the form of the backward-Euler differentiation, except that the delay of the subtrahend is  $N + 1$ . Thus it is called the slow multiplexed differentiator. Its coefficient is time-varying and periodic with the period  $T_t$ . Therefore, to implement this function, the multiplexing technique can be applied to an ordinary SC differentiator to

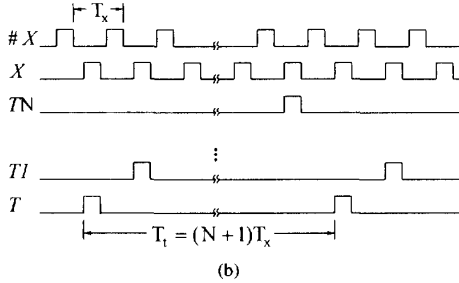
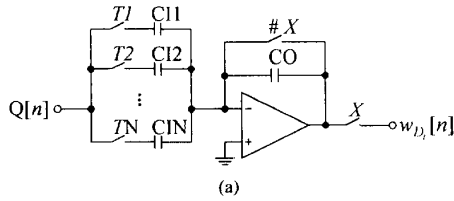


Fig. 2. (a) The circuit of slow multiplexed differentiator. (b) The associated clock waveforms.

produce the desired output. This results in the reduction of the components used. The designed SC slow multiplexed differentiator circuit and the associated clock waveforms are shown in Fig. 2 where the core structure of the SC differentiator proposed in [9], [10] has been used. The capacitor values are related to the coefficients as follow:

$$\frac{CI_i}{CO} = -h_{D_i}^i, \quad 1 \leq i \leq N.$$

In this circuit, the capacitor array controlled by the clock phases  $T1, T2, \dots, TN$  is used to hold  $N$  points of the past input and each capacitor in the array is accessed in turn every  $T_t$ . Therefore, the difference between  $Q[n]$  and  $Q[n-N-1]$  can be easily obtained.  $\#X$  and  $X$  are non-overlapping clocks with the clock period  $T_x$  for  $Q[n]$ , whereas the clock  $T$  has a clock period  $T_t = (N+1)T_x$  for  $P_i[m]$ .

**Slow Multiplexed Integrator:** The relationship between the input sequence  $Q[n]$  and output sequence  $w_{I_t}[n]$  of the slow multiplexed integrator is defined as

$$w_{I_t}[n] \equiv \begin{cases} 0, & n = m(N+1) \\ h_{I_t}^i I_t\{Q[n]\}, & n = m(N+1) + i, 1 \leq i \leq N \end{cases} \quad (8)$$

where

$$I_t\{Q[n]\} \equiv \sum_{j=0}^m Q[j(N+1) + i] = \sum_{j=0}^m P_i[j] \text{ and } h_{I_t}^i \leq 0.$$

Similar to the slow multiplexed differentiator, the realization of this function can be obtained by modifying the SC backward-Euler integrator into the time-sharing structure. This circuit is shown in Fig. 3 where the integrator proposed in [8] is adopted as the core structure and the clock  $T$  is used to obtained zero output at  $n = m(N+1)$ . In this circuit, the past  $N$ -point results are stored in the capacitor array controlled by the clock phases  $T1, T2, \dots, TN$ . Thus it is called the slow multiplexed integrator. The operation clock waveforms are the same as

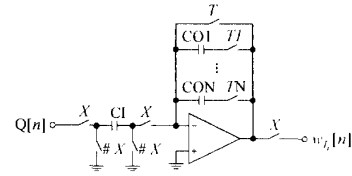


Fig. 3. Circuit of the slow multiplexed integrator.

those in Fig. 2. The capacitor values in the slow multiplexed integrator are related to the coefficients as follows:

$$\frac{CI_i}{CO_i} = -h_{I_t}^i, \quad 1 \leq i \leq N.$$

In this circuit, there is a serious disadvantage. When all the clock phases are off, the op-amp is under open-loop condition, and its output will be rapidly saturated to the level of power supply. Although it can be recovered in the next clock phase, this still degrades circuit performance. When using this circuit to implement (6), therefore, the architecture of overall SC circuits must be carefully designed to avoid this problem.

**Fast Multiplexed Differentiator:** The relationship between the input sequence  $Q[n]$  and the output sequence  $w_{D_x}[n]$  of the fast multiplexed differentiator is defined as

$$w_{D_x}[n] \equiv \begin{cases} 0, & n = m(N+1) \\ h_{D_x}^i D_x\{Q[n]\}, & n = m(N+1) + i, 1 \leq i \leq N \end{cases} \quad (9)$$

where

$$D_x\{Q[n]\} \equiv Q[n] - Q[n-1] \text{ and } h_{D_x}^i \leq 0.$$

This function is similar to the ordinary form of differentiation except the coefficient is time-varying and periodic with the period  $T_t$ . Therefore, a capacitor array is adopted as the output capacitor of the SC differentiator. By turning on the switches in the capacitor array, the effective output capacitor can be adjusted to the required value. The resultant circuit is shown in Fig. 4 where the capacitor ratios and the coefficients are related by

$$\frac{CI_i}{CO_i + CO} = -h_{D_x}^i, \quad 1 \leq i \leq N.$$

The capacitor  $CO$  is used to reduce the value of all  $CO_i$  and prevent the op-amp from entering the open-loop condition. The switch controlled by the clock phase  $T$  is to produce zero output when  $n = m(N+1)$ . The major difference between this differentiator and the slow multiplexing differentiator is the differentiation is performed for the two samples with one  $T_x$  delay rather than  $(N+1)T_x$  delay. Thus it is called the fast multiplexed differentiator.

**Fast Multiplexed Integrator:** The relationship between the input sequence  $Q[n]$  and the output sequence  $w_{I_x}[n]$  of the fast multiplexed integrator is defined as

$$w_{I_x}[n] \equiv \begin{cases} 0, & n = m(N+1) \\ I_x\{h_{I_x}^i Q[n]\}, & n = m(N+1) + i, 1 \leq i \leq N \end{cases} \quad (10)$$

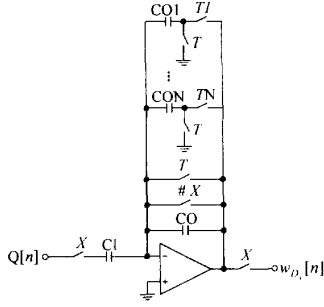


Fig. 4. Circuit of the fast multiplexed differentiator.

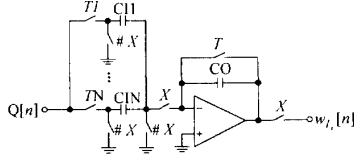


Fig. 5. Circuit of the fast multiplexed integrator.

where

$$I_x\{Q[n]\} \equiv \sum_{j=1}^i Q[m(N+1)+j] \quad \text{and} \quad h_{I_x}^i \leq 0.$$

Similar to the fast multiplexed differentiator, this function can be implemented by changing the input capacitor of the SC integrator into a capacitor array. Thus, the effective input capacitor value can be varied in different clock phases. Since the integration must restart with the new initial condition after  $N+1$  points, the switch controlled by the clock phase  $T$  is used to reset the stored charges on the capacitor. The circuit is shown in Fig. 5 where the capacitor ratios and the coefficient are related by

$$\frac{CI_i}{CO} = -h_{I_x}^i, \quad 1 \leq i \leq N.$$

Since the integrator in Fig. 5 performed the integration on the samples with one  $T_x$  delay rather than one  $T_t$  delay in the slow multiplexed integrator, it is called the fast multiplexed integrator.

### III. FILTER DESIGN PROCEDURE

In order to demonstrate how to apply the proposed new multiplexing design methodology described in Section II to the design of high-order filters, a general low-pass filter design procedure is described. First, the  $s$ -domain transfer function of a general low-pass filter is decomposed into the product of the

biquads as

$$H_N(s) = \frac{Y(s)}{U(s)} = \sum_{i=1}^N \frac{1 + b_i s + c_i s^2}{1 + d + (b_{i+1} + e_i)s + (c_{i+1} + f_i)s^2} \quad (11)$$

where  $b_i$ ,  $c_i$ ,  $d$ ,  $e_i$  and  $f_i$  are constant coefficients. Then (11) is transformed into the  $z$ -domain. Since all basic function circuits described in Section II are backward-Euler type, it is convenient to adopt the backward-Euler transformation

$$s = \frac{1 - z^{-1}}{T_t}$$

where  $T_t$  is the sampling period of input and output signals. Therefore, the  $z$ -domain transfer function can be expressed as (12) (see below.) Using (2)–(5) to define  $P_i[m]$  and  $Q[n]$ , the operation of the multiplexing biquad system in Fig. 1(b) can be described as

$$\begin{aligned} Q[n] = & Q[n-1] + b_i T_t^{-1} (Q[n-1] - Q[n-N-2]) \\ & + c_i T_t^{-2} ((Q[n-1] - Q[n-N-2]) \\ & - (Q[n-N-2] - Q[n-2N-3])) \\ & - dQ[n] - (b_{i+1} + e_i) T_t^{-1} (Q[n] - Q[n-N-1]) \\ & - (c_{i+1} + f_i) T_t^{-2} ((Q[n] - Q[n-N-1]) \\ & - (Q[n-N-1] - Q[n-2N-2])). \end{aligned} \quad (13)$$

According to (7), (9), and (10), it is straightforward to change (13) into

$$\begin{aligned} Q[n] = & I_x \{ D_x \{ -b_{i+1} T_t^{-1} D_t \{ Q[n] \} \} \\ & + D_x \{ -c_{i+1} T_t^{-2} D_t \{ D_t \{ Q[n] \} \} \} \\ & - dQ[n] - e_i T_t^{-1} D_t \{ Q[n] \} \\ & - f_i T_t^{-2} \{ D_t \{ Q[n] \} \} \}. \end{aligned} \quad (14)$$

Since the four basic linear operators in Section II have the following relations as

$$\begin{aligned} I_x \{ D_x \{ Q[n] \} \} &= Q[n] \\ D_t \{ h[n] Q[n] \} &= h[n] D_t \{ Q[n] \} \end{aligned}$$

if  $h[n]$  is a periodic sequence with the period  $T_t$ , (14) can be rewritten as

$$\begin{aligned} Q[n] = & -\alpha \beta D_t \{ \hat{b}_i Q[n] \} - I_x \{ \hat{e}_i \beta D_t \{ \hat{b}_i Q[n] \} \} \\ & - I_x \{ \hat{d} Q[n] \} - \gamma D_t \{ \hat{c}_i D_t \{ \hat{b}_i Q[n] \} \} \\ & - I_x \{ \hat{f}_i D_t \{ \hat{c}_i D_t \{ \hat{b}_i Q[n] \} \} \} \end{aligned} \quad (15)$$

where

$$\begin{aligned} b_i &= \alpha \beta \hat{b}_{i-1} T_t, & c_i &= \gamma \hat{b}_{i-1} \hat{c}_{i-1} T_t^2, \\ d &= \hat{d}, & e_i &= \beta \hat{b}_i \hat{e}_i T_t, & f_i &= \hat{b}_i \hat{c}_i \hat{f}_i T_t^2. \end{aligned}$$

$$H_N(z) = \frac{Y(z)}{U(z)} = \sum_{i=1}^N \frac{1 + b_i(1 - z^{-1})T_t^{-1} + c_i(1 - z^{-1})^2 T_t^{-2}}{1 + d + (b_{i+1} + e_i)(1 - z^{-1})T_t^{-1} + (c_{i+1} + f_i)(1 - z^{-1})^2 T_t^{-2}} \quad (12)$$

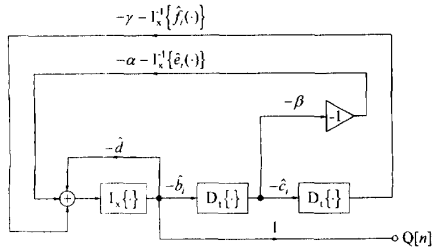


Fig. 6. The block diagram of (15).

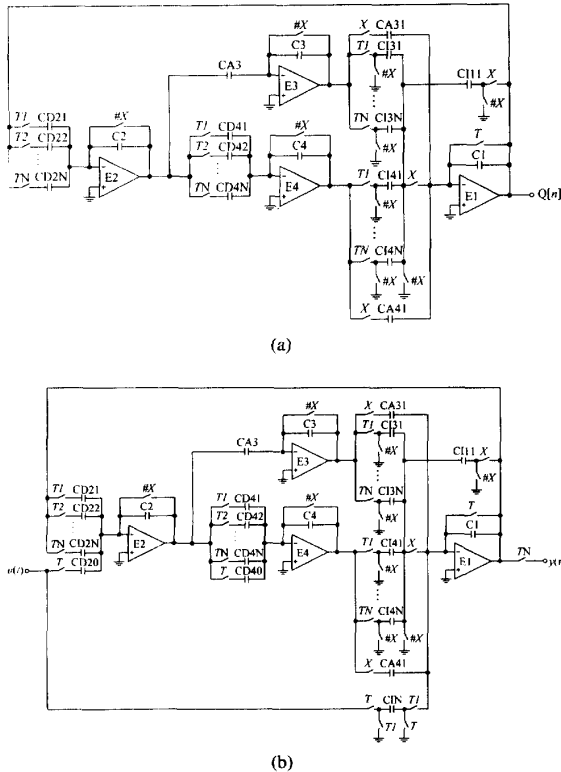


Fig. 7. (a) The circuit of the multiplexing biquad. (b) The entire circuit to realize (11).

The block diagram to represent the above equation is shown in Fig. 6. Assuming

$$\alpha, \beta, \gamma, \hat{d}, \hat{e}_i, \hat{f}_i \geq 0, \quad \hat{b}_i, \hat{c}_i > 0,$$

we have

$$b_i, c_i, d, e_i, f_i \geq 0.$$

From Fig. 6, it can be seen that the multiplexing biquad can be implemented by using the SC inverter [10], slow multiplexed differentiators, and fast multiplexed integrator. The resultant circuit is shown in Fig. 7(a).

As to the initialization step, its operation is to produce the initial conditions of the multiplexed biquad required in the clock phase  $T1$ . From the circuit of the multiplexed biquad, it can be observed that these initial conditions are the

voltages stored in the capacitors  $C1$ ,  $CA31$ , and  $CA41$ . For the capacitors  $CA31$  and  $CA41$ , their stored voltages must be set as following:

$$V(CA31) = \beta D_t \{ \hat{b}_0 Q[m(N+1)] \}$$

$$V(CA41) = D_t \{ \hat{c}_0 D_t \{ \hat{b}_0 Q[m(N+1)] \} \}.$$

As  $Q[m(N+1)] = u[m]$ , we can use the structure of the multiplexing biquad to compute these values by substituting  $u[m]$  for  $x[n]$  in the clock phase  $T$ . Therefore, the correct initial values can be stored in these capacitors. Since the resulting voltage value in the capacitor  $C1$  is meaningless, the switch controlled by the clock phase  $T$  is used to reset this value and prevent it from disturbing other operations. As to the capacitor  $C1$ , the required initial voltage during the clock phase  $T1$  is  $u[m]$ . It is easy to perform this initialization step by adding a capacitor branch connected to the op-amp  $E1$ . The entire circuit of the multiplexing low-pass filter system is shown in Fig. 7(b) where the capacitor branches  $CD20$  and  $CD40$  are added to compute the initial values stored in  $CA31$  and  $CA41$  during the clock phase  $T$ , and the capacitor branch  $CIN$  is used to store  $u[m]$  during the clock phase  $T$  and send it to  $C1$  during the clock phase  $T1$ .

According to (14)–(15) and Fig. 6, the relationship between the capacitor ratios in Fig. 7(b) and the coefficients of (11) can be described as

$$1 = \frac{CIN}{C1} \tag{16}$$

$$b_{i+1} = T_t \frac{CD2i}{C2} \frac{CA3}{C3} \frac{CA31}{C1}, \quad 0 \leq i \leq N \tag{17}$$

$$c_{i+1} = T_t^2 \frac{CD2i}{C2} \frac{CD4i}{C4} \frac{CA41}{C1}, \quad 0 \leq i \leq N \tag{18}$$

$$d = \frac{CIN}{C1} \tag{19}$$

$$e_i = T_t \frac{CD2i}{C2} \frac{CA3}{C3} \frac{C13i}{C1}, \quad 1 \leq i \leq N \tag{20}$$

$$f_i = T_t^2 \frac{CD2i}{C2} \frac{CD4i}{C4} \frac{C14i}{C1}, \quad 1 \leq i \leq N. \tag{21}$$

As mentioned above, the circuit in Fig. 7(b) can be directly used to implement (11) when  $b_i, c_i, d, e_i$ , and  $f_i$  are all nonnegative. To implement (11) for different coefficients, this circuit needs some modification. For negative  $b_i$  and  $e_i$ , they can be realized by adding suitable capacitor branches between the output of op-amp  $E2$  and the input of op-amp  $E1$ . For the negative  $c_i$  and  $f_i$ , they can be realized by using the SC inverter  $E3$ . As to the negative  $d$ , it can be realized by using the SC inverter  $E3$ . Also, increasing the capacitor ratio  $CIN/C1$  has the same effect.

Although it is simple and straightforward to develop the multiplexing low-pass system by using the backward-Euler mapping to transform  $H_N(s)$  into  $H_N(z)$ , this transformation causes  $Q$ -value degradation in  $H_N(z)$ . Therefore, the sampling frequency must be much larger than the cut-off frequency of the low-pass system, and the pre-warping technique must be applied to minimize the approximating error. If this error is still not tolerable, the bilinear transformation can be used to realize the four basic functions and obtain  $H_N(z)$ . Similar design procedure can also be developed to design high-order filters.

The architecture of the circuit shown in Fig. 7(b) has a disadvantage in that the feedback paths to the op-amp  $E1$

are of global feedback. It is lack of local feedback. Although these global feedback paths are all negative, it is possible to make the SC circuit oscillate if the global feedback is large enough. This is due to the extra time delay of the global feedback path which is passing the op-amps  $E2$ ,  $E3$ , and  $E4$ . There are three compensation methods to eliminate this effect. The first one is to add redundant components to the circuit to increase the local negative feedback. The second method is to partially change the architecture of the circuit to increase the local negative feedback. The last one is to use fully-differential op-amps instead of single-ended-output op-amps to decrease the time delay. These methods have their own advantages and disadvantages. They can be used according to the application need and its requirement.

#### IV. DESIGN EXAMPLE

Consider the design of a low-pass filter which has a flat passband with 3 dB attenuation at 0.5 kHz and a passband gain of unity. The stopband attenuation should be at least 70 dB for  $f > 1.5$  kHz. The sampling frequency is 16 kHz.

Since this filter has a flat passband, the Butterworth approximation is adopted to develop its transfer function. According to the computer program, the order of Butterworth filter must be larger than seven to satisfy the filter requirement. Hence, we choose  $M = 8$  and use the backward-Euler mapping to transform this transfer function into  $z$ -domain. Since this mapping will result in  $Q$ -value degradation at the center of the filter passband, the  $Q$ -value and the 3 dB frequency must be adjusted to minimize this effect. Therefore, the  $z$ -domain transfer function can be obtained as

$$H(z) = \frac{1}{1 + 1.2280(1 - z^{-1}) + 19.613(1 - z^{-1})^2} \times \frac{1}{1 + 4.4209(1 - z^{-1}) + 19.613(1 - z^{-1})^2} \times \frac{1}{1 + 6.8646(1 - z^{-1}) + 19.613(1 - z^{-1})^2} \times \frac{1}{1 + 8.1872(1 - z^{-1}) + 19.613(1 - z^{-1})^2}.$$

Using the circuit in Fig. 7(b) to implement this transfer function, the capacitor values can be easily calculated by (16)–(21). These values are

$$\begin{aligned} CD20 &= 0, & CD21 &= 1.2280, & CD22 &= 4.4209, \\ CD23 &= 6.8646, & CD24 &= 8.1872, \\ CD40 &= 0, & CD41 &= 6.6672, & CD42 &= 1.8519, \\ CD43 &= 1.1927, & CD44 &= 1, \\ CI41 &= CI42 = CI43 = CI44 = 2.3956, \\ CI11 &= CA31 = CA41 = 0, \end{aligned}$$

and other capacitors are unit capacitors. The SWITCAP [11] simulation result and the ideal frequency response of the

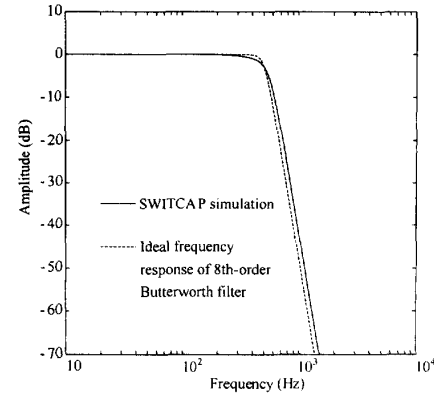


Fig. 8. SWITCAP simulation results and ideal calculation results of the 8th-order low-pass filter example.

8th-order Butterworth low-pass filter are shown in Fig. 8. Although there is some difference in the transition region, it still meets the filter specification.

#### V. EXPERIMENT RESULTS

To verify the proposed design method, an 8th-order low-pass filter is designed and fabricated in 1.2  $\mu\text{m}$  CMOS double-poly double-metal process. The circuit to implement this filter is shown in Fig. 9, and its  $z$ -domain transfer function can be expressed as

$$H(z) = \frac{(1 + CA31(1 - z^{-1}) + 4(1 - z^{-1})^2)^3}{(1 + (4 + CA31 - CI21)(1 - z^{-1}) + 12(1 - z^{-1})^2)^4}.$$

The chip photomicrograph is shown in Fig. 10. The op-amps in the circuit of Fig. 9 are of the simple two-stage type. The sampling period of the input signal is 1.6E-4 second and the capacitor values are

$$CD11 = CD12 = CD13 = CD14 = 4 \text{ pF}, \quad CI41 = 8 \text{ pF}, \\ CIN = C1 = CA3 = C3 = 1 \text{ pF}.$$

The capacitor values of CA31 and CI21 can be tuned from 1 pF to 4 pF and used to control the decay speed in the transition region and the  $Q$ -value, respectively. To demonstrate the capability of the compensation scheme in eliminating the circuit instability caused by the global feedback, the capacitor values of CD21, ..., CD24, CD41, ..., CD44, C2, and C4 are set to 4 pF to increase the time-delay of the global feedback. The second compensation method mentioned in Section III is applied to the filter circuit. Basically, the function of the capacitor array CD11, ..., CD14 is the same as that of the capacitor array CI31, ..., CI3N in Fig. 7(b). However, in the transient step, this capacitor array can increase the local feedback. Therefore, this circuit is more stable. The measured frequency response with different values of CA31 is shown in Fig. 11. It can be seen that the decay speed in the transition region increases as CA31 decreases. This result agrees with the responses from the theoretical calculation and the SWITCAP simulation.

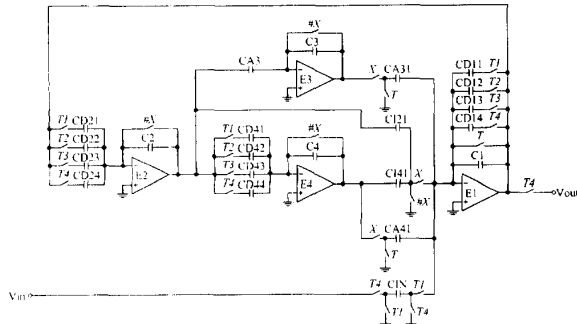


Fig. 9. The experimental low-pass filter with the compensation circuit.

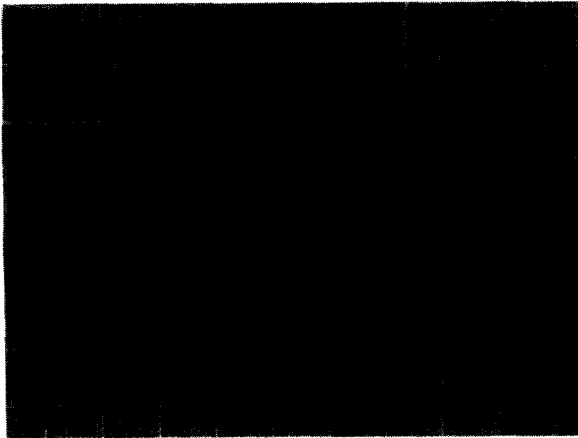


Fig. 10. Chip photomicrograph of the fabricated low-pass filter in Fig. 9.

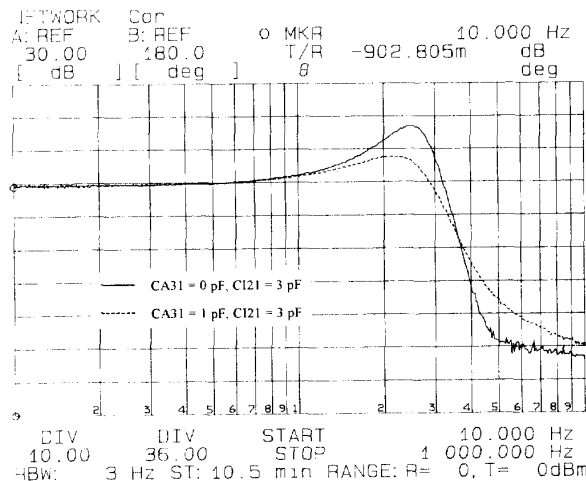


Fig. 11. The measured frequency response of the fabricated low-pass filter in Fig. 9 with different values of CA31.

The measured results with different values of CI21 are also shown in Fig. 12. The  $Q$  value of the filter increases as CI21 increases. This is also consistent with the theoretical calculation and SWITCAP simulation results.

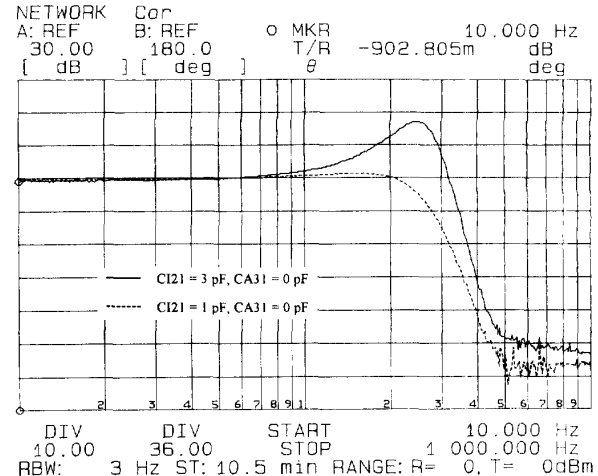


Fig. 12. The measured frequency response of the fabricated low-pass filter in Fig. 9 with different values of CI21.

## VI. CONCLUSION

Based upon the multiplexing technique which uses a SC biquad in the time-sharing way, a new design method for high-order SC filters is proposed and analyzed. By using the new design method, the realized SC high-order filters have less op-amps, switches, and capacitors, and thus smaller chip area, as compared to those realized by using the conventional method. As the filter order increases, only a few switches and capacitors, as well as extra clock phases, are required, but the number of op-amps remains the same. Thus the proposed design method is useful in those applications where power dissipation and chip area are critical issues while many clock phases are available.

Further work on applying the design method to high-order bandpass SC filter design and other special SC filter design and applications will be addressed in the near future.

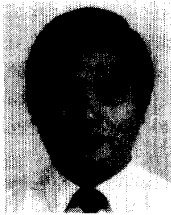
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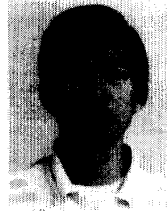


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