Passivation-Induced Subthreshold Kink Effect of Ultrathin-Oxide Low-Temperature Polycrystalline Silicon Thin Film Transistors

Mon-Chin Tsai, Ta-Chuan Liao, I-Che Lee, and Huang-Chung Cheng, *Member, IEEE*

***Abstract*—Polycrystalline silicon thin-film transistors (poly-Si TFTs) with an ultrathin electron cyclotron resonance plasma-oxidized gate oxide have been fabricated. These ultrathin gate oxide poly-Si TFTs demonstrate better gate controllability and short-channel effect suppression, as compared with conventional thick-gate oxide poly-Si TFTs. A subthreshold kink effect has been observed in these ultrathin gate oxide poly-Si TFTs after NH_3 plasma treatment for the first time. The ultrathin oxide will limit the diffusion of plasma radicals, resulting in plasma radical pileup along the channel width, causing this subthreshold kink effect. The kink effect will be less significant in devices with a narrow channel width as the current flow associated with the corners of the device will dominate over the flat-plate region.**

***Index Terms*—Electron cyclotron resonance (ECR) oxide, plasma passivation, subthreshold kink effect, thin-film transistor (TFT).**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) on transparent substrates are finding applications as pixel-switching elements of flat-panel liquid crystal displays [1], [2], applications as vertically stackable components of 3-D integrations [3], [4], and further system-on-panel (SOP) applications [5]. For the application in 3-D and SOP, a lower processing temperature and a thinner gate oxide are desired. The lower processing temperature can widen the system integration process window. The thinner gate oxide will allow scaling down of device dimensions and short-channel effect (SCE) suppression. Recently, a thin electron cyclotron resonance (ECR) plasma-oxidized gate oxide has been published as a low-temperature high-quality oxide solution to enhance gate controllability [6], [7]. In contrast to the conventional chemical vapor deposition (CVD) method of oxide deposition on a substrate, the ECR oxide methodology provides high-energy oxygen ions reacting with atomic silicon to form a silicon dioxide film on the silicon surface. Thus, this oxide growth can be processed at a lower temperature, rather than the conventional high-temperature thermal oxide growth. On the other hand, the grain boundaries and intragranular defects inside the poly-Si active layer also exert a profound influence on the device performance. Thus, both grain enlargement technologies [8], [9], as well as the defect passivation treatment [10], [11], have increasingly become important.

In this letter, ultrathin 5-nm ECR plasma-oxidized gate oxide poly-Si TFTs under 260 °C have been studied for the first time. The NH_3 plasma treatment is also applied to passivate the poly-TFTs defect states. A subthreshold kink phenomenon has been measured in these ECR poly-Si TFTs with the plasma treatment. This kind of kink effect becomes less significant with decreasing device channel width. The electrical characterization, the plasma radical diffusion path, and the device model for ultrathin oxide poly-Si TFTs are studied in this letter.

II. Experimental Procedure

Six-in-diameter (100) oriented silicon wafers were used as the substrate. A 600-nm-thick thermal oxide was grown on the silicon substrate in a stream oxygen ambient. Amorphous silicon (α-Si) films of 100 nm thick were then deposited on the oxide layer using a low-pressure CVD system at 550 °C. This α-Si film was treated with solid-phase crystallization under 600 °C for 24 h to accomplish a grain size around 0.2 μm. After defining the device active region, a 5-nm-thick ECR gate oxide was reacted in O_2: 10 sccm and Ar: 5 sccm mixed plasma reaction chamber for 60 min. The reaction chamber pressure was 50 mtorr; the substrate temperature was 260 °C with microwave power under 600 W. The conventional transistor process (including gate patterning), self-aligned phosphorous source/drain (S/D) ion implantation, and a 300-nm-thick passivation oxide layer were processed as follows: The S/D doping activation was performed at 600 °C in the N_2 ambient for 10 h. After contact opening and electrode metallization, a 1-h NH_3 plasma treatment in a parallel-plate plasma reactor at 300 °C with a power density of 0.7 W/cm^2 was carried out for defect reduction [12]. Different dimension poly-Si TFTs with a channel width from 10 to 0.2 μm and a gate length from 10 to 2 μm were designed to analyze the passivation effects. Device characterizations of these poly-Si TFTs with and without the NH_3 plasma treatment were also carried out.

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M.-C. Tsai is with the Department of Electronic Engineering, National Kaohsiung University of Applied Sciences, Kaohsiung 807, Taiwan (e-mail: marstsai@hotmail.com).

T.-C. Liao is with Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan (e-mail: tcliao.ee92g@nctu.edu.tw).

I.-C. Lee and H.-C. Cheng are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: iclee.ee95g@nctu.edu.tw; hccheng536@mail.nctu.edu.tw).

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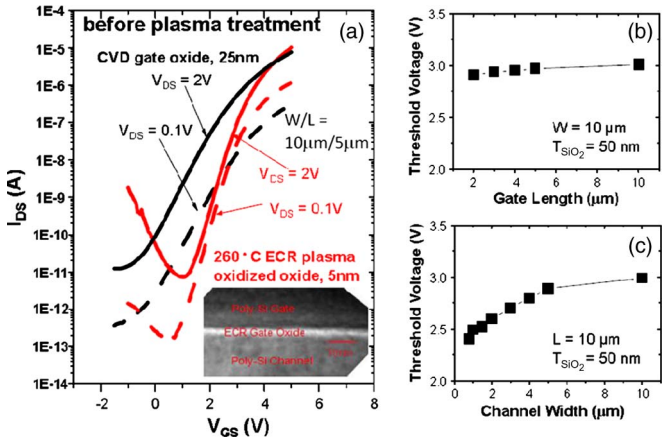

Fig. 1. (a) Transfer characteristics of poly-Si TFTs with the ECR and CVD oxide before the plasma treatment. (Inset) Cross-sectional TEM picture of the ECR oxide/poly-Si interface. (b) Threshold voltage variation of ECR oxide poly-Si TFTs exhibits the short-channel effect. (c) Threshold voltage variation of ECR oxide poly-Si TFTs exhibits the narrow-width effect.

III. Results and Discussion

The transfer characteristics of poly-Si TFTs with the ECR and CVD gate oxides are exhibited in Fig. 1(a). It is found that the ECR oxide poly-Si TFTs demonstrate a superior subthreshold swing performance than the CVD oxide ones. The inset shows the cross-sectional transmission electron microscopy (TEM) picture of the 5-nm-thick ECR oxide/poly-Si interface. Fig. 1(b) shows the threshold voltage variation for the TFTs of different gate lengths. The ultrathin gate oxide can improve the poly-Si TFT's gate controllability; this results in a superior swing performance and SCE suppression, compared with conventional CVD gate oxide poly-Si TFTs. The threshold voltage variation for the TFTs of different channel widths is also shown in Fig. 1(c). The threshold voltage decreases from 3 to 2.4 V for channel widths from 10 μm down to 0.8 μm. It implies that the gate control is further increased with decreasing of the channel width due to corner portion domination.

The transfer curves of these poly-Si TFTs with the NH_3 plasma treatment are also measured, as shown in Fig. 2. In contrast to the nonpassivated devices shown in Fig. 1, a subthreshold kink phenomenon has been measured in these poly-Si TFTs. The kink effect for a channel width of 10 μm is obvious in Fig. 2(a). However, this kink effect becomes insignificant when the channel width decreases to 5 μm, as shown in Fig. 2(b). Once the channel width keeps decreasing, the kink characteristic becomes invisible for the devices with a channel width of 0.8 μm, as shown in Fig. 2(c).

To explain this threshold voltage decrease with channel width and the subthreshold kink phenomenon for the NH_3 plasma-passivated devices, an effective poly-Si TFT model has been proposed. For the transistor in the width direction, the equivalent channel width is composited of a flat plate and corner edge portions. The fringe effect in the corner direction can provide a higher electric field than in the flat direction. This kind of transistor kink effect has been reported in shallow trench isolation devices before [13]. We can thus divide the equivalent transistor into flat and corner segments. Normally, the flat transistor dominates transistor characterization. The

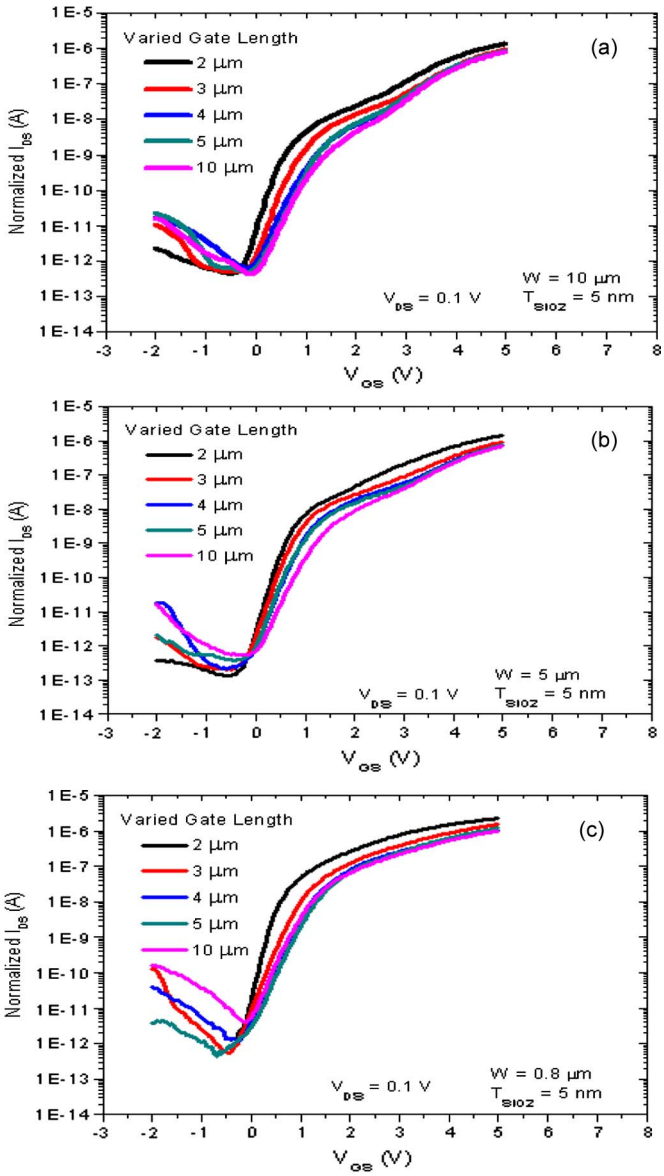

Fig. 2. Normalized transfer characteristics of ECR poly-Si TFTs with the NH_3 plasma treatment under different channel widths. (a) $W = 10$ μm. (b) $W = 5$ μm. (c) $W = 0.8$ μm.

corner transistor plays a limited role and is generally named as the parasitic transistor.

It is known that the NH_3 plasma treatment can passivate the poly-Si/oxide dangling bonds [14], thus improving transistor drivability and reducing the threshold voltage. It is also reported that the gate oxide is the major diffusion path for plasma radicals to passivate the poly-Si/oxide interface states [15]. For poly-Si TFTs with a thick gate oxide, the gate oxide provides a wide diffusion path for plasma radicals to sufficiently passivate the poly-Si/oxide interface. This is why no such subthreshold kink effect is observed in thick-gated poly-Si TFTs. However, once the oxide thickness is reduced, the diffusion of the plasma radicals will be limited, causing the plasma radicals to pile up at the transistor corner edge along the width direction. Thus, the threshold voltage drop in the corner edge will become more significant than that in the flat plate region. For Poly-Si TFTs operating at lower gate voltages, channel conduction starts

at the corner. The corner device works like a low-threshold-voltage transistor. As the gate voltage continues to increase, the flat device will be turned on. The flat device works like a high-threshold-voltage transistor. Once the drain current of the high-threshold-voltage transistor is higher than that of the low-threshold-voltage, the kink effect in the subthreshold region will thus be observed. By comparing the normalized transfer characteristics between Fig. 2(a) and (b), it can be found that the weighting of the corner transistor has been increased with reduced channel width. Once the channel width keeps decreasing, the corner transistor will gradually dominate the transistor characterization; the contribution of the flat transistor in the drain current will eventually become invisible, as shown in Fig. 2(c).

IV. Conclusion

In summary, low-temperature (260 °C) ultrathin ECR gate oxide poly-Si TFTs have been fabricated. The ultrathin gate poly-Si TFTs demonstrate good gate controllability in superior subthreshold swing performance and SCE suppression. A subthreshold kink effect has been measured for these ultrathin poly-Si TFTs after the NH_3 plasma treatment. This is due to the ultrathin gate oxide limiting plasma radical diffusion and results in the plasma radical pileup along the channel width. The reduced threshold voltage reduction in the corner transistor with respect to the flat transistor will appear as a visible subthreshold kink characteristic. Once the channel width keeps decreasing, the corner devices will gradually dominate the poly-Si TFTs characterization. This subthreshold kink phenomenon will thus be reduced in narrow width configuration.

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