A Cost-Effective Preamble-Assisted Engine With Skew Calibrator for Frequency-Dependent I/Q Imbalance in 4 × 4 MIMO-OFDM Modem

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***Abstract*—Variations in I/Q gains, phases, and filters of the RF frontend, namely frequency-dependent I/Q imbalance (FDI), are an important factor in OFDM-based wireless access. To enable the proper function of a 4 × 4 MIMO-OFDM receiver this work proposes a low-complexity preamble-assisted solution using only one complex divider and one complex multiplier to handle significant FDI distortions. An all-digital multiphase and multi-rate clock generator (MPRCG) was built to support fast dynamic frequency scaling for FDI estimation and compensation and for efficient implementation. Based on the proposed MPRCG, a skew calibration was also realized to tune I/Q timing coherently via multiphase A/D clocking. Performance evaluation showed that the proposed approach incurs an SNR loss of 1.5 dB to maintain a packet-error rate of less than 10% under a 1 dB gain error, 15° phase error and worse filter mismatch. Thus, this solution not only provides adequate performance, but also makes FDI estimation and compensation more cost-effective.**

***Index Terms*—Clock generator, dynamic frequency scaling, frequency-dependent I/Q imbalance, I/Q mismatch, MIMO-OFDM.**

I. Introduction

MULTIPLE-INPUT multiple-output orthogonal frequency division multiplexing (MIMO-OFDM) is widely used in next-generation communication systems to overcome frequency-selective fading [1]–[3]. However, RF distortions result in serious degradation in performance for most OFDM-based systems. Mismatches in gain, phase, and filter between in-phase (I) and quadrature-phase (Q), known as frequency-dependent I/Q imbalance (FDI), cause not only time-domain signal skew but also frequency-domain gain and phase imbalance. As a result, it becomes difficult for an OFDM direct-conversion receiver to recover data. The goal of this study is to mitigate analog front-end imperfections such as FDI distortion via digital signal processing.

A huge number of schemes have been proposed for such impairment compensation (e.g., [4]–[20]). Some studies [4]–[9] utilized specific formats in SISO-OFDM systems. A post-FFT least-squares equalization [4] costed 40 training symbols to achieve <1-dB SNR loss. Based on signal correlation property, a time-domain least-squares method [5] ensured low computational complexity. With loopback signal path, an adaptive pre-distortion scheme [6] required 1000 independent trials to reach at least 50-dB image rejection ratio (IRR). By using trigonometric least mean square algorithm, a CORDIC based adaptive FIR filter [7] worked properly within 20 iterations. In order to perform over 70-dB IRR, a pilot-based self-calibration approach [8] averaged 100 estimation results in the TX and the RX, respectively. And a nonlinear least squares scheme [9] would estimate both CFO and FDI within 1-dB SNR loss. In MIMO-OFDM systems, the joint compensation of CFO, TX FDI and RX FDI [10], whose SNR loss was less than 1 dB, was also performed by the user-defined preamble. Because IEEE WLAN standards define the short, long preambles (training fields) and coded datum, the I/Q imbalance can be solved efficiently. For example, a low-complexity time-domain algorithm [11] was used and implemented in an IEEE 802.11a receiver (SISO OFDM). And a few solutions were derived for IEEE 802.11n systems (MIMO OFDM): (1) a linear optimal solution and an RLS-based adaptive filter [12]; (2) an input-output relation governing Alamouti-coded OFDM systems [13]; and (3) a cross-validation estimation via the property of long preambles [14]. Recently, the blind algorithms have been made for general SISO-OFDM systems, e.g., a self-calibrating image rejection scheme [15] with an IRR > 70 dB, a CSAD method [16] for both CFO and FDI, an adaptive Wiener filter [17] for FDI cancellation, one time-domain and one frequency-domain FDI estimations [18] via the second-order statistics, a joint estimation and compensation [19] of CFO and FDI under timing uncertainty, and a circularity-based FDI compensation [20] being independent of carrier synchronization. Although several approaches [15], [17]–[19] work properly, they require at least 4000 trials to converge, and cost over 10 k multiplications and 20 k additions.

This study proposes a relatively low-complexity preamble-assisted algorithm, which has a cost-effective implementation and is able to remove FDI distortions in a 4 × 4 MIMO-OFDM receiver. Only four short and four long preambles are needed to estimate FDI distortions over frequency domains. Through skew calibration, the filter mismatch can be reduced to enhance frequency-domain compensation. Our implementation consists of a preamble-assisted engine, and an all-digital multiphase and multi-rate clock generator (MPRCG), as shown in Fig. 1. The proposed MPRCG not only eliminates timing skew via multiphase A/D clocking, but also supports fast dynamic frequency scaling (DFS) to minimize the number of complex dividers and complex multipliers in the

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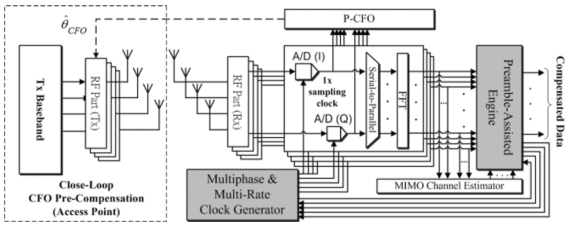


Fig. 1. Block diagram of a preamble-assisted engine with skew calibration for frequency-dependent I/Q imbalance.

preamble-assisted engine. As a result, the proposed mechanism is cost-effective and is well-suited to the next-generation wireless LAN proposed in the IEEE 802.11 TGac [22] group, as it uses only one complex divider and one complex multiplier.

The rest of this paper is organized as follows. Section II addresses system assumptions and mathematical notations. Section III presents the proposed preamble-assisted I/Q compensator. The hardware implementation is described in Section IV. Section V discusses the performance evaluation. Conclusions are presented in Section VI. Finally a divider-free arc-tangent and a table of abbreviations are presented in Appendix.

II. System Assumptions

A. System Description

This MIMO-OFDM system is set up for point-to-point transmission, e.g., an infrastructure mode, as shown in Fig. 1. A close-loop pre-compensation scheme is applied to account for CFO. A pseudo-CFO (P-CFO) [23] method, which rotates three training symbols by adding an extra frequency offset into the received sequence, is used to obtain an accurate CFO value ($\hat{\theta}_{\mathrm{CFO}}$) under I/Q mismatch. Having found this value, the transmitter can adjust its carrier to pre-compensate for the CFO distortion. Each MIMO-OFDM symbol has $\mathrm{N_{FFT}}$ sub-carriers where $\mathrm{N_{data}}$ sub-carriers are data and pilots. The other sub-carriers are nulls. The packets are assumed to contain common preambles and MIMO preambles, where the common preambles are similar to the preambles in SISO-OFDM systems. Both common preambles and MIMO preambles can be of two types: 1) time-domain short preambles, such as the common short preamble (CSP) and the MIMO short preamble (MSP); and 2) frequency-domain long preambles, such as the common long preamble (CLP) and the MIMO long preamble (MLP). The term $s_{\mathrm{CSP}}^{(i_{\mathrm{TX}},n_{\mathrm{Symbol}})}(\mathbf{t})$ denotes the nth CSP symbol in the ith transmitter antenna and its valid length is $(N_{\mathrm{FFT}})/(m)$, where $0 < m \leq N_{\mathrm{FFT}}$. The term $L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},n_{\mathrm{Symbol}})}(k)$ represents the nth MLP symbol in the ith transmitter antenna and k represents the kth fraction (sub-carrier). The number of MLPs is equal to the number of transmitter antennas, and their length is equal to $\mathrm{N_{data}}$. The detail descriptions of mathematical notations are provided in Table I.

B. FDI Models

Fig. 2 shows the block diagram of a typical FDI model [9], [14], [18]. The received RF signal with a central frequency w_c is expressed as

$$x_{\mathrm{RF}}^{(j_{\mathrm{RX}})}(t) = 2\mathrm{Re}\left\{z_{BB}^{(j_{\mathrm{RX}})}(t)e^{jw_c t}\right\} = z_{BB}^{(j_{\mathrm{RX}})}(t)e^{jw_c t} + z_{BB}^{(j_{\mathrm{RX}})*}(t)e^{-jw_c t} \quad (1)$$

TABLE I
Table of Mathematical Notations

Symbol	Explanation
$\alpha^{(j_{RX})}(k)$	The parameters of the FDI distortions in the j^{th} receiver antenna
$\beta^{(j_{RX})}(k)$	The parameters of the FDI distortions in the j^{th} receiver antenna
$\theta^{(j_{RX})}$	Phase error in the j^{th} receiver antenna
$C^{(i_{TX})}(k)$	The parameters of cross-ratio imparity in the i^{th} transmitter antenna
$D^{(j_{RX})}(k)$	The ratio of $\beta^{(j_{RX})}(k)$ to $\alpha^{(j_{RX})*}(-k)$
$g^{(j_{RX})}$	Amplitude mismatch in the j^{th} receiver antenna
$G^{(j_{RX})}(k)$	The channel gain after division-free compensation in the j^{th} receiver antenna
$\mathscr{H}^{(i_{TX},j_{RX})}(k)$	The ideal estimated CFR between the i^{th} transmitter antenna and the j^{th} receiver antenna
$\hat{\mathscr{H}}^{(i_{TX},j_{RX})}(k)$	The estimated CFR between the i^{th} transmitter antenna and the j^{th} receiver antenna
$H_{LPF_I}^{(j_{RX})}(k)$	The frequency responses of I-path low-pass filters in the j^{th} receiver antenna
$H_{LPF_Q}^{(j_{RX})}(k)$	The frequency responses of Q-path low-pass filters in the j^{th} receiver antenna
$L_{IdealPattern}^{(i_{TX})}(k)$	The ideal pattern in the i^{th} transmitter antenna
$L_{MLP}^{(i_{TX},n_{Symbol})}(k)$	The n^{th} MIMO long preamble (MLP) symbol in the i^{th} transmitter antenna
$L_{VLP}^{(i_{TX})}(k)$	The virtual long preamble (VLP) in the i^{th} transmitter antenna
N_{FFT}	Number of sub-carriers per OFDM symbol
N_{data}	Number of data and pilot sub-carriers per OFDM symbol
$r^{(j_{RX})}(t)$	The down-converted signal in the j^{th} receiver antenna
$R_{VLP}^{(j_{RX})}(k)$	The received virtual long preamble in the j^{th} receiver antenna
$s_{CSP}^{(i_{TX},n_{Symbol})}(t)$	The n^{th} common short preamble (CSP) symbol in the i^{th} transmitter antenna
$\Delta\hat{S}^{(j_{RX})}$	The estimated residual I/Q skew information in the j^{th} receiver antenna
$\hat{S}^{(j_{RX})}$	The estimated I/Q skew information in the j^{th} receiver antenna
$u_{LO}^{(j_{RX})}(t)$	The local oscillator signal in the j^{th} receiver antenna
w_c	The central frequency of RF
$x_{RF}^{(j_{RX})}(t)$	The received RF signal in the j^{th} receiver antenna
$z_{BB}^{(j_{RX})}(t)$	The received baseband signal in the j^{th} receiver antenna

where $z_{BB}^{(j_{\mathrm{RX}})}(t)$ is the received baseband signal, $*$ denotes the complex conjugate, and j is the index of the receiver antenna. The received RF signal $x_{\mathrm{RF}}^{(j_{\mathrm{RX}})}(t)$ is direct down-converted by a local oscillator signal $u_{\mathrm{LO}}^{(j_{\mathrm{RX}})}(t)$ with mismatched I branches and Q branches. The amplitude mismatch and phase error are $g^{(j_{\mathrm{RX}})} = (1+\varepsilon^{(j_{\mathrm{RX}})})$ and $\theta^{(j_{\mathrm{RX}})}$, respectively; ideally, $\varepsilon^{(j_{\mathrm{RX}})} = 0$ and $\theta^{(j_{\mathrm{RX}})} = 0$. The local oscillator signal $u_{\mathrm{LO}}^{(j_{\mathrm{RX}})}(t)$ of an imbalanced quadrature demodulator is then given by

$$u_{\mathrm{LO}}^{(j_{\mathrm{RX}})}(t) = \cos(w_c t) - jg^{(j_{\mathrm{RX}})}\sin\left(w_c t + \theta^{(j_{\mathrm{RX}})}\right) \quad (2)$$

The down-converted signal $r^{(j_{\mathrm{RX}})}(t) = r_I^{(j_{\mathrm{RX}})}(t) + r_Q^{(j_{\mathrm{RX}})}(t)$ is as shown in (3), where LPF_I and LPF_Q are the low-pass filters for the I and Q branches, respectively. The frequency responses of LPF_I and LPF_Q are given by $H_{\mathrm{LPF}_I}^{(j_{\mathrm{RX}})}(k)$ and $H_{\mathrm{LPF}_Q}^{(j_{\mathrm{RX}})}(k)$, respectively The non-coherent LPF_I and LPF_Q result in timing skews that are caused by the inconsistent main pulses of two

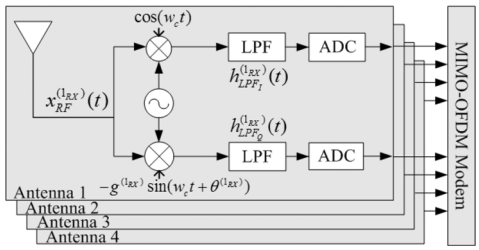


Fig. 2. Model of frequency-dependent I/Q imbalances in MIMO-OFDM systems.

LPFs, which are plotted in Fig. 3(a) and (b). From (3), the frequency-domain I- and Q-path signals after low-pass filtering are given by (3)–(4), shown at the bottom of the page. Thus, the received down-converted signal $R^{(j_{\mathrm{RX}})}(k)$ is

$$\begin{aligned} R^{(j_{\mathrm{RX}})}(k) &= R_I^{(j_{\mathrm{RX}})}(k) + jR_Q^{(j_{\mathrm{RX}})}(k) \\ &= \alpha^{(j_{\mathrm{RX}})}(k) Z_{BB}^{(j_{\mathrm{RX}})}(k) + \beta^{(j_{\mathrm{RX}})}(k) Z_{BB}^{(j_{\mathrm{RX}})*}(-k) \end{aligned} \tag{5}$$

where

$$\begin{aligned} \alpha^{(j_{\mathrm{RX}})}(k) &= \left[H_{LPF_I}^{(j_{\mathrm{RX}})}(k) + H_{LPF_Q}^{(j_{\mathrm{RX}})}(k) g^{(j_{\mathrm{RX}})} e^{-j\theta^{(j_{\mathrm{RX}})}} \right] \Big/ 2 \\ \beta^{(j_{\mathrm{RX}})}(k) &= \left[H_{LPF_I}^{(j_{\mathrm{RX}})}(k) - H_{LPF_Q}^{(j_{\mathrm{RX}})}(k) g^{(j_{\mathrm{RX}})} e^{j\theta^{(j_{\mathrm{RX}})}} \right] \Big/ 2 \end{aligned} \tag{6}$$

and $Z_{BB}^{(j_{\mathrm{RX}})}(k)$ is the received baseband signal in the jth receiver antenna, and $Z_{BB}^{(j_{\mathrm{RX}})*}(-k)$ is the image aliasing effect due to I/Q distortions where $-k = (N_{data} + 1 - k)$ is the mirror position (sub-carrier) of the OFDM symbols. For simplification without loss of generality, these two LPFs can be modeled by a finite impulse response (FIR) filter [9]. For example, the filter mismatch can be modeled by a worse case [9] of $h_{\mathrm{LPF}_I}^{(j_{\mathrm{RX}})}(t) = \delta(t) + 0.1\delta(t-1)$ and $h_{\mathrm{LPF}_Q}^{(j_{\mathrm{RX}})}(t) = 0.1\delta(t) + \delta(t-1)$, or as a minor case of $h_{\mathrm{LPF}_I}^{(j_{\mathrm{RX}})}(t) = \delta(t) + 0.1\delta(t-1)$ and $h_{\mathrm{LPF}_Q}^{(j_{\mathrm{RX}})}(t) = 0.8\delta(t) + 0.3\delta(t-1)$, as shown in Fig. 4(a) and (b). These also show that filter mismatch and its timing skew cause severe distortions. Due to the process, voltage and temperature effects of RF parts, FDI distortions are modeled as quasi-static, allowing distortions to be time-invariant over one group, composed of K packets ($K \in \mathbb{N}$), and change dependently from group to group.

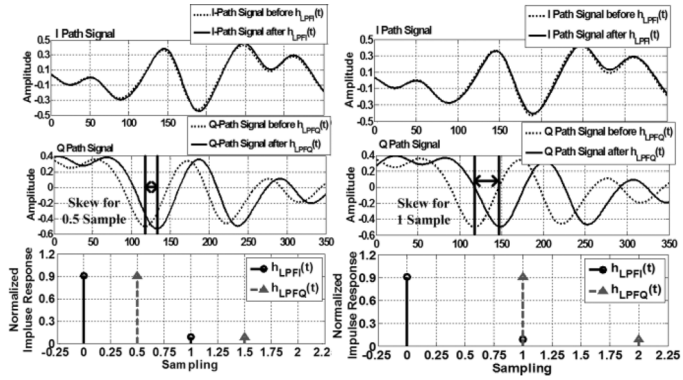


Fig. 3. Timing skews between the I and Q paths: (a) skewed by half a sample period and (b) skewed by one sample period.

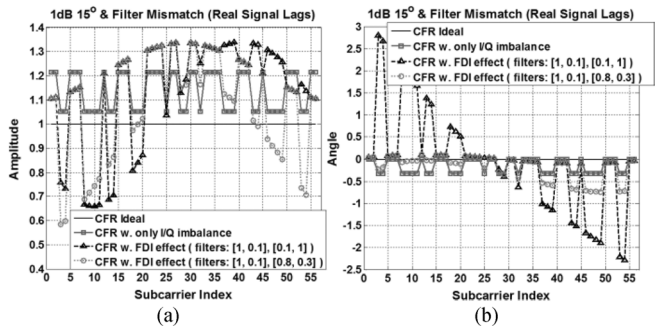


Fig. 4. Amplitude and angle of channel frequency response with 1 dB gain error, 15° phase error and timing skew: (a) amplitude and (b) angle.

C. Problem Statement

For a cost-effective design, preambles are useful to reduce computational complexity. If such preambles (e.g., the CLP and the MLP in the specifications) are not well-defined in packets, we can create a virtual one via the received preambles. Since the timing skew of filter mismatches cause I-path and Q-path signals inconsistency, as shown in Fig. 3(a) and (b), it should be eliminated first to reduce the residual I/Q-imbalance. Yet, it is difficult to remove that distortions by shifting or skewing I-path or Q-path buffers after analog-to-digital (A/D) conversion. Using multiphase A/D clocking to skew A/D sampling is simple and useful for making the main pulses of I-path and Q-path LPFs coherent. Besides, the number of complex dividers and complex multipliers must be minimized due to the high

$$\begin{aligned} r^{(j_{\mathrm{RX}})}(t) &= \mathrm{LPF}_I^{(j_{\mathrm{RX}})} \left\{ x_{\mathrm{RF}}^{(j_{\mathrm{RX}})}(t) \cos(w_c t) \right\} \\ &\quad - j\mathrm{LPF}_Q^{(j_{\mathrm{RX}})} \left\{ g^{(j_{\mathrm{RX}})} x_{\mathrm{RF}}^{(j_{\mathrm{RX}})}(t) \sin(w_c t + \theta^{(j_{\mathrm{RX}})}) \right\} \\ &= \mathrm{LPF}_I^{(j_{\mathrm{RX}})} \left\{ \frac{1}{2} \left[z_{BB}^{(j_{\mathrm{RX}})}(t) + z_{BB}^{(j_{\mathrm{RX}})*}(t) \right] + \frac{1}{2} \left[z_{BB}^{(j_{\mathrm{RX}})}(t) e^{2jw_c t} + z_{BB}^{(j_{\mathrm{RX}})*}(t) e^{-2jw_c t} \right] \right\} \\ &\quad + j\mathrm{LPF}_Q^{(j_{\mathrm{RX}})} \left\{ \begin{array}{l} \frac{g^{(j_{\mathrm{RX}})}}{2j} \left[z_{BB}^{(j_{\mathrm{RX}})}(t) e^{-j\theta^{(j_{\mathrm{RX}})}} - z_{BB}^{(j_{\mathrm{RX}})*}(t) e^{j\theta^{(j_{\mathrm{RX}})}} \right] \\ -\frac{g^{(j_{\mathrm{RX}})}}{2j} \left[z_{BB}^{(j_{\mathrm{RX}})}(t) e^{j(2w_c t + \theta^{(j_{\mathrm{RX}})})} - z_{BB}^{(j_{\mathrm{RX}})*}(t) e^{-j(2w_c t + \theta^{(j_{\mathrm{RX}})})} \right] \end{array} \right\} \end{aligned} \tag{3}$$

$$\begin{aligned} R_I^{(j_{\mathrm{RX}})}(k) &= \frac{H_{LPF_I}^{(j_{\mathrm{RX}})}(k) \left[Z_{BB}^{(j_{\mathrm{RX}})}(k) + Z_{BB}^{(j_{\mathrm{RX}})*}(-k) \right]}{2} \\ R_Q^{(j_{\mathrm{RX}})}(k) &= \frac{g^{(j_{\mathrm{RX}})} H_{LPF_Q}^{(j_{\mathrm{RX}})}(k) \left[Z_{BB}^{(j_{\mathrm{RX}})}(k) e^{-j\theta^{(j_{\mathrm{RX}})}} - Z_{BB}^{(j_{\mathrm{RX}})*}(-k) e^{j\theta^{(j_{\mathrm{RX}})}} \right]}{2j}. \end{aligned} \tag{4}$$

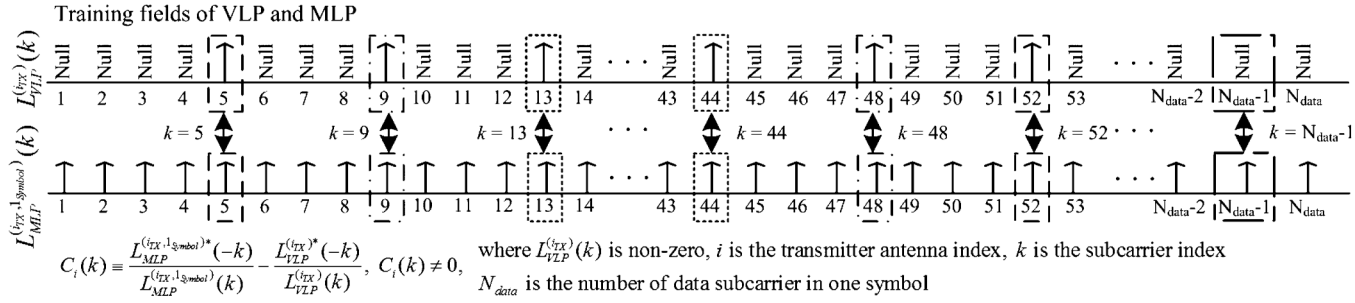


Fig. 5. The cross-ratio imparity of $L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)$ and $L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k)$.

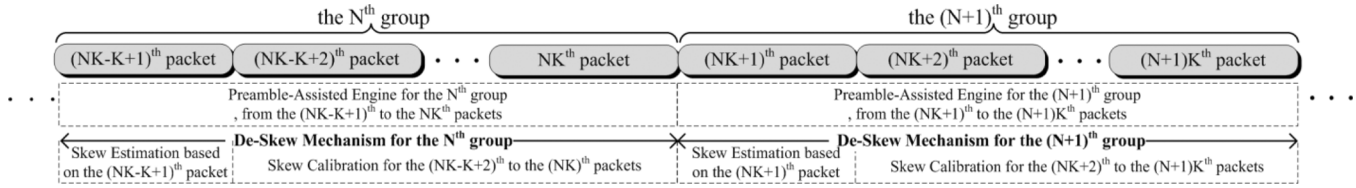


Fig. 6. Steps of the proposed mechanism.

cost of these two components in VLSI design. And multi-rate clocking should be utilized because the computational effort required for FDI estimation and compensation ([16], [17] and [18]) is not the same. Although phase-locked loops (PLL) and delay-locked loops (DLL) are popular, most exhibit unexpected phase transients, known as the hang-up phenomenon [24]–[26]. It is also key to derive an all-digital multiphase and multi-rate mechanism without PLLs, DLLs and analog circuits requiring.

III. Preamble-Assisted Compensation

A. Basic Concept

Due to the image aliasing effect caused by I/Q distortions shown as (5), a cross-ratio imparity (CRI), $C^{(i_{\mathrm{TX}})}(k) \neq 0$, is defined to serve the extraction of I/Q imbalance where $C^{(i_{\mathrm{TX}})}(k)$ is the difference between the ratio of (n_1)th symbol of preamble $(L^{(i_{\mathrm{TX}},n_1\ \mathrm{Symbol})}(k))$ to its conjugate mirror part, and the ratio of (n_2)th symbol of preamble $(L^{(i_{\mathrm{TX}},n_2\mathrm{Symbol})}(k))$ to its conjugate mirror part, where $n_1 \neq n_2$ and $n_1, n_2 \in \mathbb{N}$:

$$C^{(i_{\mathrm{TX}})}(k) \equiv \frac{L^{(i_{\mathrm{TX}},n_{1\mathrm{Symbol}})^*}(-k)}{L^{(i_{\mathrm{TX}},n_{1\mathrm{Symbol}})}(k)} - \frac{L^{(i_{\mathrm{TX}},n_2\ \mathrm{Symbol})^*}(-k)}{L^{(i_{\mathrm{TX}},n_2\ \mathrm{Symbol})}(k)} \tag{7}$$

where $L^{(i_{\mathrm{TX}},n_1\ \mathrm{Symbol})}(k)$ and $L^{(i_{\mathrm{TX}},n_2\ \mathrm{Symbol})}(k)$ are two different frequency-domain preambles in the ith transmitter antenna. According to heuristic results, at least one quarter of $L^{(i_{\mathrm{TX}},n_1\ \mathrm{Symbol})}(k)$ and $L^{(i_{\mathrm{TX}},n_2\ \mathrm{Symbol})}(k)$ should satisfy $C^{(i_{\mathrm{TX}})}(k) \neq 0$ and be distributed uniformly to ensure accurate FDI estimation. Therefore, we collect m time-domain CSPs and transfer them to the frequency domain via FFT to get a virtual long preamble (VLP), which is defined by

$$L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(\mathrm{k}) \equiv \left\{ s_{\mathrm{CSP}}^{(i_{\mathrm{TX}},n_{\mathrm{Symbol}})}(\mathrm{k}), s_{\mathrm{CSP}}^{(i_{\mathrm{TX}},n+1_{\mathrm{Symbol}})}(k), \ldots \right. \left. s_{\mathrm{CSP}}^{(i_{\mathrm{TX}},n+m-1_{\mathrm{Symbol}})}(\mathrm{k}) \right\} \times \overrightarrow{E}(k), \tag{8}$$

where

$$\overrightarrow{\mathrm{E}}(k) = \left[1\ e^{-j\frac{2\pi k}{N_{\mathrm{FFT}}}}\ e^{-j\frac{4\pi k}{N_{\mathrm{FFT}}}}\ e^{-j\frac{6\pi k}{N_{\mathrm{FFT}}}}\ e^{-j\frac{8\pi k}{N_{\mathrm{FFT}}}} \ldots e^{-j\frac{2\pi(N_{\mathrm{FFT}}-1)k}{N_{\mathrm{FFT}}}} \right]^T$$

where $\overrightarrow{E}(k)$ denotes the coefficient of the FFT, and $[\ldots]^{\mathrm{T}}$ signifies the transpose of the matrix. Then the $C^{(i_{\mathrm{TX}})}(k)$ from (7) can be rewritten as follows:

$$C^{(i_{\mathrm{TX}})}(k) \equiv \frac{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k)}{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)} - \frac{L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k)}{L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k)} \tag{9}$$

Fig. 5 shows plots of $L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)$ and $L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k)$, where $C^{(i_{\mathrm{TX}})}(k) \neq 0$ is distributed uniformly. To extract all the mismatches of gains, phases, and filters, a CRI, $C^{(i_{\mathrm{TX}})}(k) \neq 0$, is required, where $C^{(i_{\mathrm{TX}})}(k)$ is defined as $(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)) - (L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k))/(L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k))$ as (9). Since the multiphase A/D clocking is able to calibrate the skew of the two main pulses of I-path and Q-path LPFs to reduce filter mismatches, the proposed algorithm is divided into two parts: 1) CRI-based estimation to deal with FDI distortions via $C^{(i_{\mathrm{TX}})}(k) \neq 0$ over the frequency domain and 2) skew calibration to improve performance. However, most MIMO-OFDM systems do not support enough preambles for these two techniques to be applied to the same packet simultaneously. We can remove the skew of the two main pulses of the I-path and Q-path LPFs by using the skew information from the previously received packet. Thus, the SNR needed for the CRI-based estimation can be efficiently reduced. The steps of the proposed work are shown in Fig. 6. The first packet of every group estimates such skew information. Skew calibration, residual IQ-imbalance estimation and compensation are then active from the second packet to the Kth packet per group.

B. CRI-Based Estimation

Since the $C^{(i_{\mathrm{TX}})}(k)$ can be developed to satisfy $C^{(i_{\mathrm{TX}})}(k) \neq 0$ as shown in Fig. 5, we can estimate FDI distortions over the frequency domain. The channel frequency response (CFR) between the ith transmitter antenna and the jth receiver antenna $(H^{(i_{\mathrm{TX}},j_{\mathrm{RX}})}(k))$ can be estimated by multiplying the received $L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},n_{\mathrm{Symbol}})}(k)$ and the inverse matrix of ideal $L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},n_{\mathrm{Symbol}})}(k)$. Accounting for FDI distortions, the estimated

CFR ($\hat{H}^{(i_{\mathrm{TX}},j_{\mathrm{RX}})}(k)$) is a function of $\alpha^{(j_{\mathrm{RX}})}(k)$, $\beta^{(j_{\mathrm{RX}})}(k)$ and the ratio of $L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},n_{\mathrm{Symbol}})}(k)$ and its conjugate mirror

$$\hat{H}^{(i_{\mathrm{TX}},J_{\mathrm{RX}})}(k) = \alpha^{(J_{RX})}(k)H^{(i_{\mathrm{TX}},J_{\mathrm{RX}})}(k) + \beta^{(J_{RX})}(k)H^{(i_{\mathrm{TX}},J_{\mathrm{RX}})^*}(-k)\frac{L_{\mathrm{MLP}}^{(i_{TX},l_{\mathrm{Symbol}})^*}(-k)}{L_{\mathrm{MLP}}^{(i_{TX},l_{\mathrm{Symbol}})^*}(k)} \quad (10)$$

where $\alpha^{(j_{\mathrm{RX}})}(k)$ and $\beta^{(j_{\mathrm{RX}})}(k)$ are the parameters of the FDI distortions in the jth receiver antenna, and $H^{(i_{\mathrm{TX}},j_{\mathrm{RX}})}(k)$ is the ideal estimated CFR of frequency-selective fading in each path, where $1 \le \mathrm{i} \le 4, 1 \le \mathrm{j} \le 4$. The received virtual long preamble in the 1st receiver antenna ($R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k)$) is equal to the summation of $L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k)$, $i = 1-4$. According to the FDI model in (5), the received virtual long preamble $R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k)$ becomes

$$R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k) = \alpha^{(1_{\mathrm{RX}})}(k)\left[\sum_{i=1}^{4} L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k)\right] + \beta^{(1_{\mathrm{RX}})}(k)\left[\sum_{i=1}^{4} L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k) \times H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)\right]. \quad (11)$$

Based on (9), $(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)) - C^{(i_{\mathrm{TX}})}(k)$ can replace $(L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k))/(L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k))$ in (11), which becomes (12), shown at the bottom of the page. After replacing $\alpha^{(1_{\mathrm{RX}})}(k)H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k) + \beta^{(1_{\mathrm{RX}})}(k)H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k))$ with $\hat{H}^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k)$ from (10), $R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k)$ can be reduced as follows:

$$R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k) = \sum_{i=1}^{4} L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times \hat{H}^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k) - \beta^{(1_{\mathrm{RX}})}(k)\left[\sum_{i=1}^{4} L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k) \times C_i(k)\right] \quad (13)$$

In order to eliminate the unknown quantity $H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)$ in (13), we use (9) and (11) again. First, we replace index k with $-k$ and by taking the conjugate of (9) shown as in (14), $(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k)) - C^{(i_{\mathrm{TX}})*}(-k)$ is equal to $(L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k))/(L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k))$.

$$C^{(i_{\mathrm{TX}})*}(-k) \equiv \frac{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)}{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k)} - \frac{L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k)}{L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k)} \quad (14)$$

Replacing $(L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k))/(L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k))$ with $(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k)) - C^{(i_{\mathrm{TX}})*}(-k)$ in (11), we get (15), shown at the bottom of the page. The $\hat{H}^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k)$ from (10) can substitute for $\alpha^{(1_{\mathrm{RX}})}(k)H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k) + \beta^{(1_{\mathrm{RX}})}(k)H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k))$ in (15). Thus, (15) becomes

$$R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k) = \sum_{i=1}^{4} L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k) \times \frac{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)}{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k)} \times \hat{H}^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k) - \alpha^{(1_{\mathrm{RX}})}(k)\left[\sum_{i=1}^{4} L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k) \times H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k) \times C^{(i_{\mathrm{TX}})*}(-k)\right]. \quad (16)$$

To remove the unknown values $H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k)$ in (16) and $H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)$ in (13), we replace index k with $-k$ and take the conjugate of (16), which can be expressed as

$$R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})^*}(-k) = \sum_{i=1}^{4} L_{\mathrm{IdealPattern}}^{(i_{\mathrm{TX}})}(k) \times \hat{H}^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k) - \alpha^{(1_{\mathrm{RX}})*}(-k)\left[\sum_{i=1}^{4} L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k) \times C^{(i_{\mathrm{TX}})}(k)\right] \quad (17)$$

where $L_{\mathrm{IdealPattern}}^{(i_{\mathrm{TX}})}(k) = L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times (L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k))$. Since $L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k)L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)$ are known, $L_{\mathrm{IdealPattern}}^{(i_{\mathrm{TX}})}(k)$ can be defined as $L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times (L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k))$. The $H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)$ in (13) and (17) is canceled by division. The ratio of $\beta^{(1_{\mathrm{RX}})}(k)$ to $\alpha^{(1_{\mathrm{RX}})*}(-k)$ is defined by the $D^{(1_{\mathrm{RX}})}(k)$ in (18), at the bottom of the next page, where $L_{\mathrm{IdealPattern}}^{(i_{\mathrm{TX}})}(k) = L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times (L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k))/(L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k))$.

However, this representation of $D^{(1_{\mathrm{RX}})}(k)$ is insufficient due to the limited number of samples of the received preambles with $C^{(1_{\mathrm{TX}})}(k) \neq 0$. For example, only one-quarter of the sub-carriers (12 sub-carriers) are available to measure the $D^{(1_{\mathrm{RX}})}(k)$in 802.11n [21]. The remaining ratios must be determined by linear interpolation with moving-average smoothing in the frequency domains. The FDI compensation is then determined by

$$Z_{BB}^{(1_{\mathrm{RX}})}(k) = \frac{\alpha^{(1_{\mathrm{RX}})*}(-k)R^{(1_{\mathrm{RX}})}(k) - \beta^{(1_{\mathrm{RX}})}(k)R^{(1_{\mathrm{RX}})*}(-k)}{\alpha^{(1_{\mathrm{RX}})}(k)\alpha^{(1_{\mathrm{RX}})*}(-k) - \beta^{(1_{\mathrm{RX}})}(k)\beta^{(1_{\mathrm{RX}})*}(-k)} \quad (19)$$

$$R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k) = \sum_{i=1}^{4}\left\{L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times \left[\begin{array}{l}\alpha^{(1_{\mathrm{RX}})}(k)H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k) \\ +\beta^{(1_{\mathrm{RX}})}(k)H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)\left(\frac{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k)}{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)} - C^{(i_{\mathrm{TX}})}(k)\right)\end{array}\right]\right\} \quad (12)$$

$$R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k) = \sum_{i=1}^{4}\left\{L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})^*}(-k) \times \left[\begin{array}{l}\alpha^{(1_{\mathrm{RX}})}(k)H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k)\left(\frac{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})}(k)}{L_{\mathrm{MLP}}^{(i_{\mathrm{TX}},1_{\mathrm{Symbol}})^*}(-k)} - C^{(i_{\mathrm{TX}})*}(-k)\right) \\ +\beta^{(1_{\mathrm{RX}})}(k)H^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)\end{array}\right]\right\} \quad (15)$$

To reduce hardware complexity and decrease latency, a division-free compensation is found as follows:

$$G^{(1_{\mathrm{RX}})}(k)Z_{BB}^{(1_{\mathrm{RX}})}(k) = R^{(1_{\mathrm{RX}})}(k) - D^{(1_{\mathrm{RX}})}(k)R^{(1_{\mathrm{RX}})*}(-k), \quad (20)$$

where $G^{(1_{\mathrm{RX}})}(k) = \alpha^{(1_{\mathrm{RX}})}(k)(1 - D^{(1_{\mathrm{RX}})}(k)D^{(1_{\mathrm{RX}})*}(-k))$ and $Z_{BB}^{(1_{\mathrm{RX}})}(k)$ is the desired data. Because $G^{(1_{\mathrm{RX}})}(k)$ is just a part of the equivalent linear channel, $G^{(1_{\mathrm{RX}})}(k)$ and the radio channel can be equalized together. $Z_{BB}^{(1_{\mathrm{RX}})}(k)$ is then determined after equalization. In addition, this division-free compensation only requires one multiplication and one subtraction operations per subcarrier.

C. Skew Calibration

In order to improve IRR and reduce the required SNR, a skew calibration is proposed to reduce the timing mismatch of the two main pulses of LPFs via multiphase A/D clocking. The estimated $D^{(1_{\mathrm{RX}})}(k)$ in (18) varies with frequency due to the mismatch in the filters, gains, and phases, as shown in Fig. 7. The normalized I/Q skew is from -1 ideal sampling to $+1$ ideal sampling in the TGnD channel (8 taps and 50 ns RMS delay spread) [27] and FDI distortions with a 1 dB gain error and a 15° phase error [9], [14]. The I/Q skew is negative when the Q-path signal leads the I-path signal, and positive when the Q-path signal lags the I-path signal. From Figs. 7(a) and 8(a), it is also clear that the variance in amplitude increases as skew increases. Fig. 8(a) also shows that the variance is almost zero if the absolute value of I/Q skew is less than 0.25. The absolute value of residual I/Q skew ($|\Delta\hat{S}^{(1_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}|$) of the Nth group is acquired via the $(N\mathrm{K} - \mathrm{K} + 1)$th packet ($D^{(1_{\mathrm{RX}})}(k)|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}}$, where $N, K \in \mathbb{N}$) given in

$$\left|\Delta\hat{S}^{(1_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}\right| = \mathrm{Decision}\left[\frac{1}{12}\sum_{k=1}^{12}\left(D^{(1_{\mathrm{RX}})}(k)|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}} - M_{D1}|_{(NK-K+1)^{\mathrm{th}}packet}\right)^2\right] \quad (21)$$

where

$$\mathrm{Decision}(x) = \begin{cases} 0, & \text{where } 0 \le x \le B_0 \\ 0.25, & \text{where } B_0 < x \le B_1 \\ 0.5, & \text{where } B_1 < x \le B_2 \\ 0.75, & \text{where } B_2 < x \le B_3 \\ 1, & \text{where } B_3 < x \end{cases},$$

$\Delta\hat{S}^{(1_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}$ is the estimated residual I/Q skew of the 1st receiver antenna in the Nth group, and M_{D1} is the mean of $D^{(1_{\mathrm{RX}})}(k)$, $k = 1 - 12$; the function $\mathrm{Decision}(x)$ is used to determine $|\Delta\hat{S}^{(1_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}|$ based on the heuristic thresholds ($\mathrm{B}_0 - \mathrm{B}_3$). Fig. 7(b) shows the phase of the 12 estimates

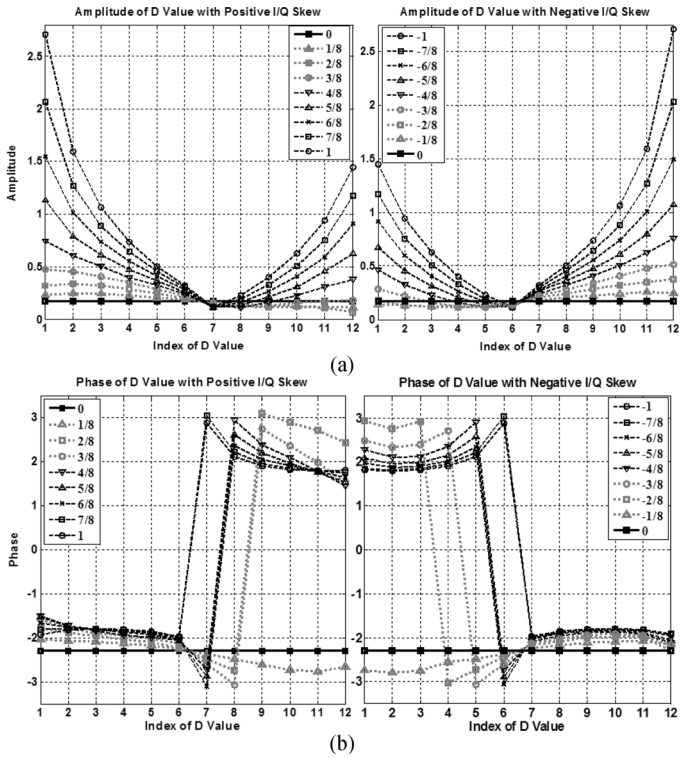


Fig. 7. Amplitude and phase of D value with the TGnD channel, 1 dB gain error, and 15° phase error: (a) amplitude and (b) phase.

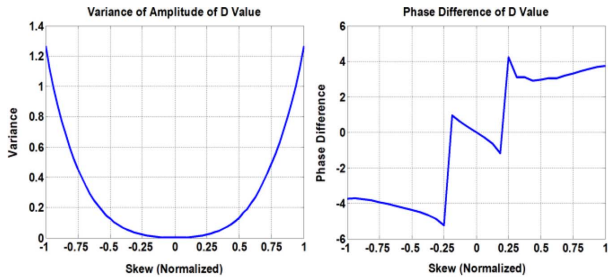
for $D^{(1_{\mathrm{RX}})}(k)|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}}$ and Fig. 8(b) shows the phase difference between $D^{(1_{\mathrm{RX}})}(12)|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}}$ and $D^{(1_{\mathrm{RX}})}(1)|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}}$. From these figures, we know that the sign of residual I/Q skew is the same as the sign of $(\angle D^{(1_{\mathrm{RX}})}(12)|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}} - \angle D^{(1_{\mathrm{RX}})}(1)|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}})$ when its absolute value is greater than or equal to 0.25. Since we only need the absolute value of residual I/Q skew to be greater than or equal to 0.25 in (21), the sign of the estimated residual I/Q skew $\Delta\hat{S}^{(1_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}$ is

$$\mathrm{sign}\left(\Delta\hat{S}^{(1_{\mathrm{RX}})}\Big|_{N^{\mathrm{th}}\mathrm{group}}\right) = \mathrm{sign}\left(\angle D^{(1_{\mathrm{RX}})}(12)\Big|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}} - \angle D^{(1_{\mathrm{RX}})}(1)\Big|_{(NK-K+1)^{\mathrm{th}}\mathrm{packet}}\right). \quad (22)$$

From (21) and (22), the estimate of residual I/Q skew $\Delta\hat{S}^{(1_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}$ can be determined. The skew information $\hat{S}^{(1_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}$ of the Nth group is obtained from

$$\hat{S}^{(1_{\mathrm{RX}})}\Big|_{N^{\mathrm{th}}\mathrm{group}} = \hat{S}^{(1_{\mathrm{RX}})}\Big|_{(N-1)^{\mathrm{th}}\mathrm{group}} + \Delta\hat{S}^{(1_{\mathrm{RX}})}\Big|_{N^{\mathrm{th}}\mathrm{group}}, \quad (23)$$

$$D^{(1_{\mathrm{RX}})}(k) = \frac{\beta^{(1_{\mathrm{RX}})}(k)}{\alpha^{(1_{\mathrm{RX}})*}(-k)} = \frac{R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})}(k) - \sum_{i=1}^{4} L_{\mathrm{VLP}}^{(i_{\mathrm{TX}})}(k) \times \hat{H}^{(i_{\mathrm{TX}},1_{\mathrm{RX}})}(k)}{R_{\mathrm{VLP}}^{(1_{\mathrm{RX}})^*}(-k) - \sum_{i=1}^{4} L_{\mathrm{IdealPattern}}^{(i_{\mathrm{TX}})}(k) \times \hat{H}^{(i_{\mathrm{TX}},1_{\mathrm{RX}})*}(-k)} \quad (18)$$



(a) (b)

Fig. 8. Characteristics of D values: (a) variances of amplitude and (b) phase difference between $D^{(1_{\mathrm{RX}})}$ (12) and $D^{(1_{\mathrm{RX}})}$ (1).

where $\hat{S}^{(1_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}$ is the skew information of the Nth group. For the jth receiver antenna, the same steps are applied to eliminate FDI distortions. Only 4 CSPs and 4 MLPs are required for the proposed solution.

IV. Hardware Implementation

The proposed hardware implementation is a 4×4 MIMO-OFDM receiver that meets the IEEE 802.11n draft requirements [21]. Two main components are described: 1) a preamble-assisted engine and 2) a multiphase and multi-rate clock generator. Their architecture is described in detail.

A. Preamble-Assisted Engine

The key to developing low-complexity implementations is to use only one complex multiplier and one complex divider shared among four antennas in RX. Fig. 9 shows the VLSI architecture of the proposed solution. This preamble-assisted engine performs three major functions: 1) estimation of the skew period, 2) estimation of residual FDI distortion and 3) compensation for the residual FDI. As complex dividers and complex multipliers account for most of the gate count in the implementation, a high-speed inner clock is needed to reduce the quantity of these two components by implementing a shared architecture. Since the computational effort involved in FDI estimation and compensation is different ([16], [17] and [18]), this high-speed inner clock needs to quickly switch between different clock rates for estimation and compensation for high power efficiency. Furthermore, both the ROM bank and the RAM bank are required to store data for each receiver antenna. The details of operation are as follows.

First, the estimated CFRs and received preambles become complex conjugates through the D-type latch. The ideal preambles (frequency domain $L^{(i_{\mathrm{TX}})}_{\mathrm{IdealPattern}}(k)$ and $L^{(i_{\mathrm{TX}})}_{\mathrm{VLP}}(k)$) are pre-stored in a ROM bank. The numerator and denominator of the $D^{(j_{\mathrm{RX}})}(k)$, which are obtained using (18), are stored in a RAM bank. Thus, by using a complex divider, the $D^{(j_{\mathrm{RX}})}(k)$ can be determined for the skew period estimation. As only 12 sub-carriers are able to calculate the $D^{(j_{\mathrm{RX}})}(k)$ directly using the received preambles in 802.11n [21], the other 44 sub-carriers must be determined using the linear interpolator. Instead of a divider, this linear interpolator only needs shift registers because $L^{(i_{\mathrm{TX}})}_{\mathrm{VLP}}(k)$ has non-zero values in the positions $\pm 5, \pm 9, \pm 13, \pm 17, \pm 21$ and ± 25 (shown in Fig. 5). Then a moving average process is exploited to smooth the whole $D^{(j_{\mathrm{RX}})}(k)$ which is for FDI compensation. The cost of this division-free compensation is just one multiplication and one subtraction per subcarrier based on (20).

According to (21) and (22), the absolute value of estimated skew is determined by the variance of $12D^{(j_{\mathrm{RX}})}(k)$ and the sign of estimated skew is decided by the phase of $D^{(j_{\mathrm{RX}})}(k)$ using the divider-free arc-tangent unit, shown in Appendix A. In Fig. 9, $B_0 - \mathrm{B}_3$ are the statistical results used as the boundary to determine the absolute value.

Once the timing skew of Nth group ($\hat{S}^{(j_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}$) is calculated, the multiphase A/D clocking will skew the A/D sampling to make main pulses of the I/Q signals coherent from the $(N\mathrm{K} - \mathrm{K} + 2)$th to the $(N\mathrm{K})$th packets.

To reduce complexity, only one complex divider and one complex multiplier are employed in the proposed engine. To perform FDI estimation based on (18), we need 8 multiplications, 1 division and 8 additions/subtractions to calculate each $D^{(j_{\mathrm{RX}})}(k)(12D^{(j_{\mathrm{RX}})}(k)$ involves 108 multiplications/divisions and 96 additions/subtractions and). In addition, another 14 multiplications/divisions and 36 additions/subtractions are needed to determine the skew estimate $\hat{S}^{(j_{\mathrm{RX}})}|_{N^{\mathrm{th}}\mathrm{group}}$. Using linear interpolation and moving averages, the total number of multiplications/divisions and additions/subtractions required are 176 and 294, respectively. The process flows of the complex multiplier and the complex divider are shown in Fig. 10. A $6\times$ clock is required to share one complex multiplier and one complex divider for FDI and skew estimations because there are 80 sub-carriers ($64 + 1/4$ cyclic prefix) per OFDM symbol. Thus, 480 (80×6) cycles are available to process ratio calculation, skew estimation, linear interpolation and the moving average. For FDI compensation, a $4\times$ clock is adequate for the complex multiplier because only one multiplication and one subtraction are needed per sub-carrier (based on (20)). Since division operations are not required for compensation, the unused complex divider should be gated to reduce power dissipation. Therefore, the required clock rates of the proposed engine are $6\times, 4\times$ and 0. DFS is implemented to improve the power efficiency and minimize the area (memory) requirements of the shared architecture. However, PLL-based DFS does not provide a $6\times$-to-$4\times$ fast DFS because the switch time of the FDI estimation and compensation is critical. An all-digital multi-rate mechanism is derived to make it easy to integrate DFS in a 4×4 MIMO-OFDM modem.

B. Multiphase and Multi-Rate Clock Generator

1) Four-Phase Clocking: In order to reduce filter mismatches via multiphase A/D clocking, a four-phase clock is needed to calibrate the timing skew of two main pulses of LPFs according to (21) and (22). While the phase interpolator [28] without PLL and DLL is a useful scheme for generating multiphase clocks, the analog delay elements are difficult to implement for wideband operations. Fig. 11 shows the all-digital architecture of the proposed MPRCG. The clock A2 has a phase delay of 180° in relation to clock A1. The clock OUT0 has a phase delay of θ° in relation to clock A1, set using a programmable all-digital delay line. Clock A3 has a phase delay of $2\theta^\circ$. The interpolator will create clock OUT90, which has half the phase delay of clock A2 in relation to clock A3. Therefore, the phase delay between clocks OUT0 and OUT90 is almost 90°. From OUT0 and OUT90, four clock with phase delays of $\theta^\circ + 0^\circ, \theta^\circ + 90^\circ, \theta^\circ + 180^\circ$ and $\theta^\circ + 270^\circ$ can be generated. The proposed four-phase clock generator utilizes a

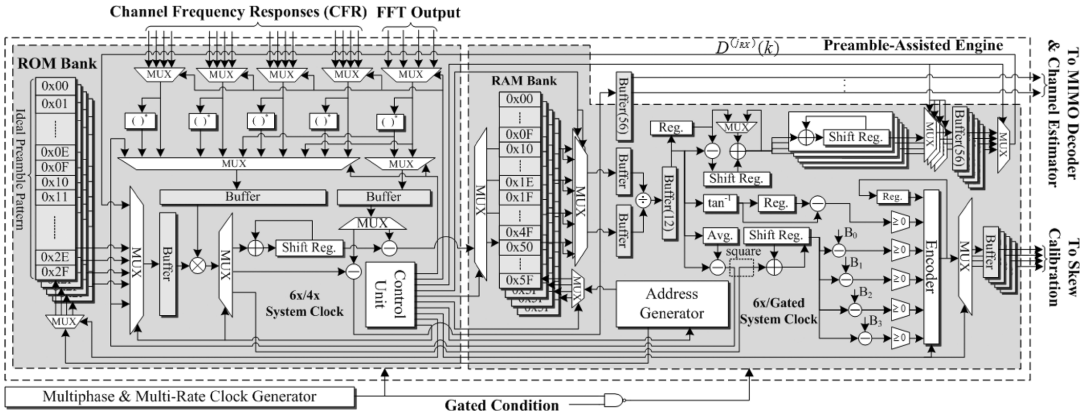


Fig. 9. The architecture of the preamble-assisted engine for a 4 × 4 MIMO-OFDM modem.

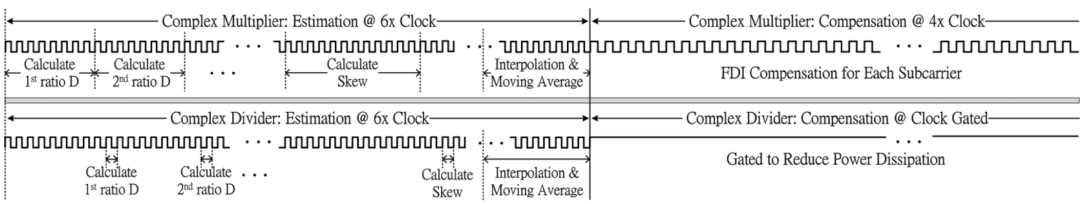


Fig. 10. The process flows of the complex multiplier and the complex divider.

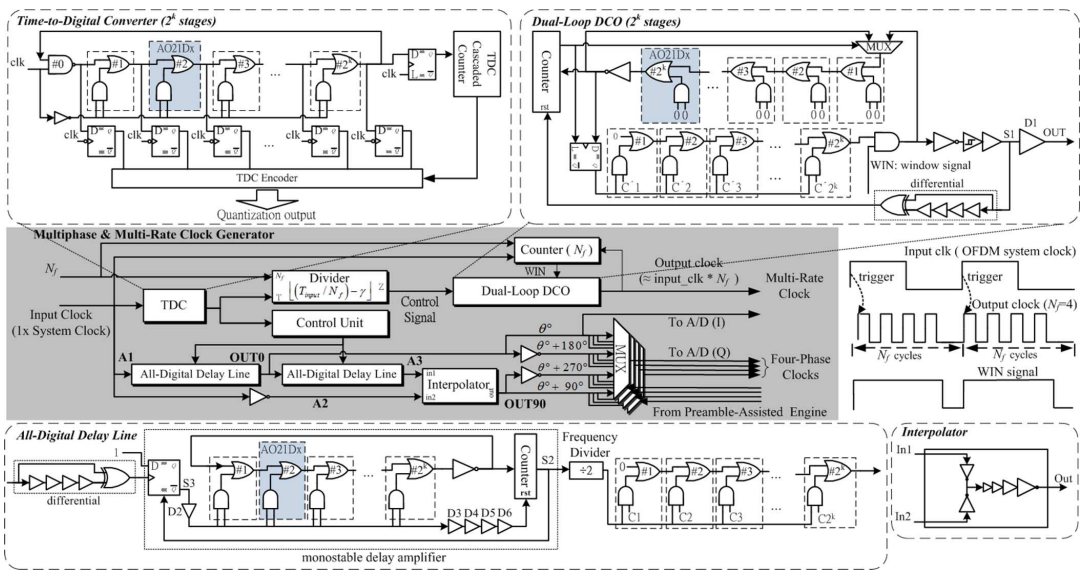


Fig. 11. Architecture of the all-digital multiphase and multi-rate clock generator.

time-to-digit converter (TDC) to calculate the cycle period of the input clock, programmable all-digital delay lines to set an appropriate delay, and the interpolator to generate a half-phase delay between two input clocks and a control unit to control the programmable all-digital delay lines. To reduce timing mismatches and provide good controllability, the delay chain applied in the TDC is also utilized in two all-digital delay lines and a dual-loop digitally controlled oscillator (DCO). To achieve good phase interpolator performance, the phase delay between clocks A1 and A3 is set as 150°–180°. The details of operation are as follows.

First, a TDC that includes a delay chain and a cascaded counter is employed to measure the period of the input clock. When it operates, the delay chain starts at the positive edge of the half-input clock and the D-type flip-flops record the delays to digitize the input period at the falling edge of the

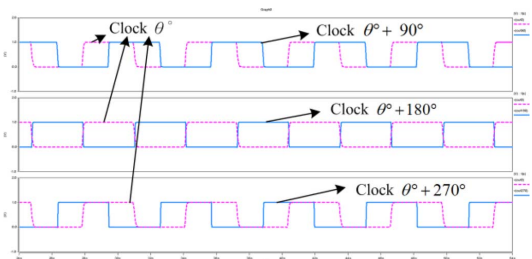


Fig. 12. Post-layout simulation of the four-phase clock generator at 80 MHz.

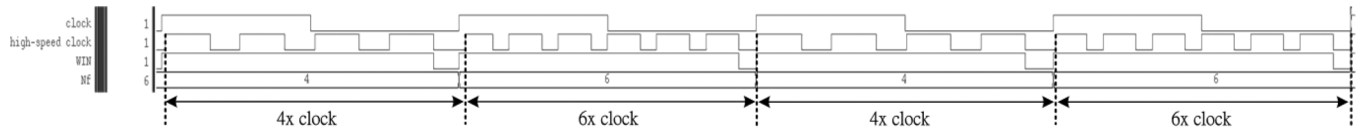


Fig. 13. Post-layout simulation of the multi-rate clock with a 20 MHz input clock for $N_f = 4$ and 6.

half-input clock. Then, the control unit processes the input period to control the programmable all-digital delay line, which can delay the input clock by θ°. Each programmable all-digital delay line is composed of four parts: a differential circuit for creating pulses on each edge of the input clock, a pulse-trigger monostable delay amplifier for delaying the input signal for n-round inner loops, a divide-by-2 divider for re-generating the output clock, and an individual delay chain used to enhance the resolution. Since each AO21Dx cell provides a few picoseconds of resolution in the monostable delay amplifier, a counter is employed to count the number of rounds of the inner loop to reduce the hardware cost and maintain flexibility. When the counter ends its count, signal S2 is set high to clear the D-type flip-flop. Next, signal S3 from the $\bar{Q}$ port of the D-type flip-flop will become high to stop the inner loop and reset the counter to zero. The delay cell D2 increases the driving capability of the signal S3. The delay cells D3–D6 delay the reset signal S3 to prevent a glitch in signal S2. On reset, the counter will set signal S2 to low to stop the reset signal S3. Thus, the counter causes signal S2 to become a pulse signal. Next, a divide-by-2 divider scales the output frequency by half, making it the same as the input clock. Finally, the individual delay chain improves the resolution according to the control signal C0–C2^k. To balance hardware cost and circuit delay, the value of k is 5 (resulting in a 32-stage TDC, delay amplifier, and individual delay chain). Fig. 12 shows a post-layout simulation of four-phase clock generation in an in-house 65 nm 1P6M digital CMOS process. The power dissipation is 289 μW at 160 MHz with a 1.0 V supply voltage.

2) Multi-Rate Clocking: To efficiently utilize the single complex multiplier and single complex divider for the dissimilar operations of estimation and compensation, a fast-switch multi-rate clock ($\geq 4\times$ clock rate) is provided by an all-digital MPRCG, which is built without any analog and all-digital PLL, as shown in Fig. 11. The proposed multi-rate clock generator consists of a time-to-digital converter (TDC) that is shared with the four-phase clock generator and calculates the input cycle period, a divider that calculates $1/\mathrm{N_f}$ multiplied by the input clock period, a dual-loop DCO for wideband transmission, and a counter that enables or disables the output of the dual-loop DCO. After TDC, a programmable divider calculates the clock period of an $\mathrm{N_f} \times \mathrm{high-speed\ clock}$ ($1/\mathrm{N_f}$ times the input clock period). Since $\mathrm{N_f}$ is either 4 or 6 in our implementation, this divider is implemented using shifters, an adder, and a subtractor. The subtractor is used to calculate the approximate clock period of an $\mathrm{N_f} \times \mathrm{high-speed\ clock}$ as follows:

$$T_{\mathrm{output}} = \lfloor (T_{\mathrm{input}}/N_f) - \gamma \rfloor \tag{24}$$

where T_{input} is the period of the input clock, N_f is the frequency multiplication factor, T_{output} is the clock period of the $N_f\times$ high-speed clock and γ is a tolerance factor representing mismatches of circuits and layouts ($\gamma = 0.5 - 2$ for an in-house 65 nm CMOS digital process). If N_f is equal to 4, only a shifter is needed. If N_f is 6, the $1/6\times$ calculation can be implemented by $(1/8) + (1)/(32)$ ($(1/6) \simeq (1/8) + (1)/(32)$). Thus, only shifters and an adder are needed.

After the divider, a dual-loop DCO begins to generate an $N_f\times$ high-speed clock, and the counter maintains the "window" signals [29] (Fig. 11), which allow the dual-loop DCO to generate N_f clocks at each rising edge of the input clock and to disable the dual-loop DCO after N_f clocks. The dual-loop DCO consists of two parts: 1) an inner loop for extending bandwidth and 2) an individual delay chain for increasing resolution. In order to minimize gate count and provide flexibility, a counter is utilized to calculate the number of rounds in the inner loop (2^k stages for each round). Next, the individual delay chain (controlled by the signal C'0-C'2^k), is used to improve the resolution of the dual-loop DCO. Due to the inner loop and individual delay chain, the dual-loop DCO is able to output a fast-switch multi-rate clock at the positive edge of the window signal. The differential circuit is utilized to generate pulses on rising or falling edges of the signal S1 in order to reset the counter to zero. A Schmitt trigger buffer cascaded with two clock buffers is added at the output to reduce jitter and enhance the driving capability because this multi-rate clock must drive the proposed preamble-assisted engine. The clock buffer D1 before the output isolates the feedback clock and reduces loading effects.

Since it employs AO21Dx logic to control the clock feedback (a total of 2^k stages), the dual-loop DCO is not affected by large parallel loading and long reset latency, in contrast to tri-state feedback [30] and pass-transistor feedback. There are 32 stages ($k = 5$) in each delay chain and the counter counts every 2 rounds, like the TDC and the delay amplifier. Using the proposed all-digital MPRCG, an approximate high-speed clock can be created easily and synchronized at each rising edge of the reference clock without PLLs. The main cost of applying this MPRCG is a 10–15% additional timing margin in VLSI implementations. Fig. 13 shows the post-layout simulation of the $6\times$-to-$4\times$ clock and fast switching with a 20 MHz reference clock. According to (24), with $N_f = 4$ and $\gamma = 1$, the $4\times$ clock runs at 79.62 MHz and the frequency offset is 0.48% (compared to 80 MHz). The $6\times$ clock is at 122.25 MHz and the frequency offset is 1.88% (compared to 120 MHz), with $N_f = 6$ and $\gamma = 0.2$. Both of these results are well within the 15% timing margin.

C. Implementation and Discussion

All modules, including the preamble-assisted engine, the MPRCG, and the divider-free arc-tangent (Appendix A) were realized using hardware-description language and Design Analyzer (Synopsys). Our work was implemented by the Taiwan Semiconductor Manufacturing Company in-house 65 nm 1P6M GP CMOS technology. The hardware costs of the proposed solution can be divided into two components: the base part that is independent of the RX antenna numbers; and the MIMO part,

TABLE II
VLSI COMPLEXITY OF THE PREAMBLE-ASSISTED ENGINE

Implementation Modules	# of Gates	Ratio
Base Parts of Preamble-Assisted Engine		
Complex Divider	13.4k	29.32%
Complex Multiplier	6.1k	13.35%
Divider-Free Arc-tan Function	3.4k	7.44%
Complex Adder	2.7k	5.91%
Comparators	1k	2.19%
Encoder	1k	2.19%
MIMO Part of Preamble-Assisted Engine		
Mux. Function	9.8k	21.44%
Control Unit	1.8k	3.94%
Address Generator	1.2k	2.63%
D-Latch Conjugate	1.4k	3.06%
Multiphase and Multi-Rate Clock Generator		
Time-to-Digital Convertor	1154	2.52%
Control Unit	988	2.16%
All-Digital Delay Lines	968	2.12%
Dual-Loop DCO	495	1.08%
Divider, Divide by 4 or 6	116	0.25%
Counter	103	0.23%
Others	64	0.14%
Interpolator	16	0.04%
Total Gate Counts	45.7k	**100%**
Memory	**Size (bytes)**	**Ratio**
SRAM	1598	80.6%
ROM	384	19.4%
Total Memory	**1982**	**100%**

which is proportional to the RX antenna number; this data is summarized in Table II. The base part consists of six modules that cost 27.6 k gates (60.4%): 13.4 k gates for a complex divider, 6.1 k gates for a complex multiplier, 3.4 k gates for the proposed divider-free arc-tan, 2.7 k gates for 16 complex adders, 1 k gates for 5 comparators and 1 k gates for an encoder. The MIMO part includes 22 multiplexers, a control unit, an address generator and D-latch conjugates, and occupies 14.2 k gates (31.07%). The MPRCG with 32 stages in each delay chain ($k = 5$) is composed of a TDC (1154 gates), a control unit (988 gates), two programmable delay lines (968 gates), a dual-loop DCO (495 gates), a divider that divides by 4 or 6 (116 gates), a counter (103 gates), an interpolator (16 gates) and other parts (64 gates). The output range of the proposed MPRCG is from 3.2 MHz to 7 GHz. The total gate count including both the preamble-assisted engine and the MPRCG is 45.7 k.

As multi-rate clocking uses the TDC shared with the four-phase clock generator, it only costs an additional 714 gates (including a divide-by-4-or-6 divider, a dual-loop DCO and a counter). With multi-rate clocking, the preamble-assisted engine only needs one complex divider (13.4 k gates) and one complex multiplier (6.1 k gates). Thus, the extra 714 gates help save on an additional gate count of 19.5 k (13.4 k + 6.1 k), making this architecture cost-effective. Since register buffers, RAM and ROM are necessary for sharing the proposed solution with four receiver antennas, 384 bytes of ROM and 1598 bytes of SRAM are required, which cost the equivalent of about 50k gates. Furthermore, to balance the wire loading of programmable all-digital delay lines in MPRCG shown in Fig. 11 the fixed layer must be enabled in the ASIC layout to guarantee inter-connection. The MPRCG must also be placed close to the power lines and power PADs to have adequate current in order to stabilize the power bounce and reduce clock jitter.

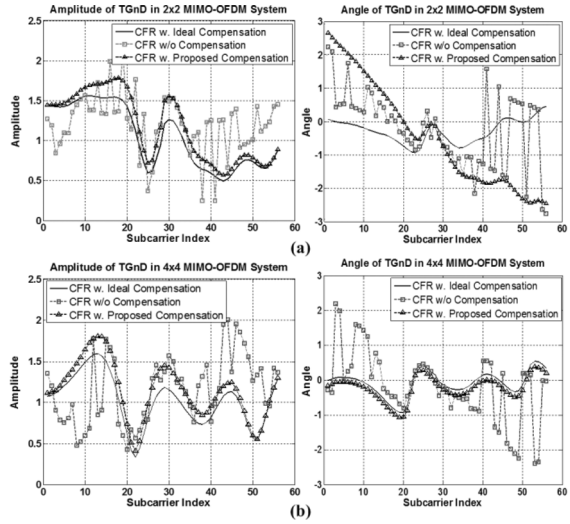


Fig. 14. Amplitude and phase of estimated CFR $\hat{H}^{(1_{\mathrm{TX}},1_{\mathrm{RX}})}(k)$ with a FDI of 1 dB gain error, 15° phase error and a worse filter mismatch with skew for a 1 sample period in TGnD channel: (a) 2 × 2 MIMO OFDM and (b) 4 × 4 MIMO OFDM.

V. PERFORMANCE EVALUATION

A. Simulation and Measurement

This solution was ported to IEEE 802.11n [21], supported 1) 2 × 2 MIMO OFDM and 2) 4 × 4 MIMO OFDM, with a bandwidth of 20 MHz ($\mathrm{N_{FFT}} = 64, \mathrm{N_{data}} = 56$ and $m = 4$), 64-QAM modulation, 2/3-coding rate, 4 × 4 space-time block code [31] and a data length of 1024 bytes. In addition, $L^{(i_{\mathrm{TX}})}_{\mathrm{IdealPattern}}(k)$ and $L^{(i_{\mathrm{TX}})}_{\mathrm{VLP}}(k)$ satisfy the condition $C^{(i_{\mathrm{TX}})}(k) \neq 0$ in twelve positions ($k = \pm4, \pm8, \pm12, \pm16, \pm20$ and ±24). A frequency-selective fading model [27] was used to evaluate the proposed approach. The two types of channel conditions considered are TGnD (RMS: 50 ns, 8 taps) and TGnE (RMS: 100 ns, 15 taps) [27]. In each antenna, the settings of the frequency-dependent I/Q imbalances are 1 dB gain error, 15° phase error and a worse filter mismatch with a different skew period [9], [14] (the LPFs of the I-path and the Q-path are modeled as $h^{(J_{\mathrm{RX}})}_{\mathrm{LPF_I}}(t) = \delta(t) + 0.1\delta(t-1)$ and $h^{(J_{\mathrm{RX}})}_{\mathrm{LPF}_Q}(t) = 0.1\delta(t) + \delta(t-1)$, and the skew period including a 1, 1/2, 1/4 and 1/8 sample period). The packet-error rate (PER) is the performance index and the required PER is 10%. Fig. 14 shows the amplitude and phase of estimated CFR ($\hat{H}^{(1_{\mathrm{TX}},1_{\mathrm{RX}})}(k)$) with frequency-dependent I/Q imbalances in the TGnD, where the high-frequency distortions are removed and the CFRs are comparable to those of frequency-selective fading after compensation. Although there are gain and phase differences between compensated CFR and ideal CFR, shown as $G^{(1_{\mathrm{RX}})}(k)$ in (20), they will not degrade the performance due to $G^{(1_{\mathrm{RX}})}(k)$ being as a part of CFRs in the equalizer. Fig. 15 plots the error rate of the skew period detection. It shows that the skew-detection error rate approaches zero when SNR is greater than 10, which means the proposed skew detector

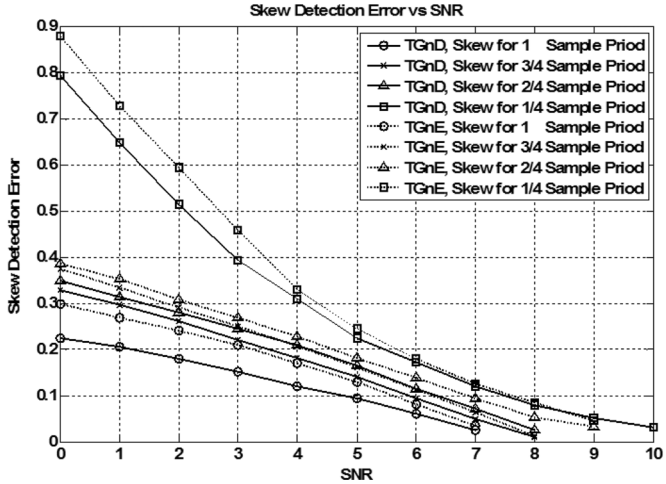


Fig. 15. The error rate of the (normalized) skew detection.

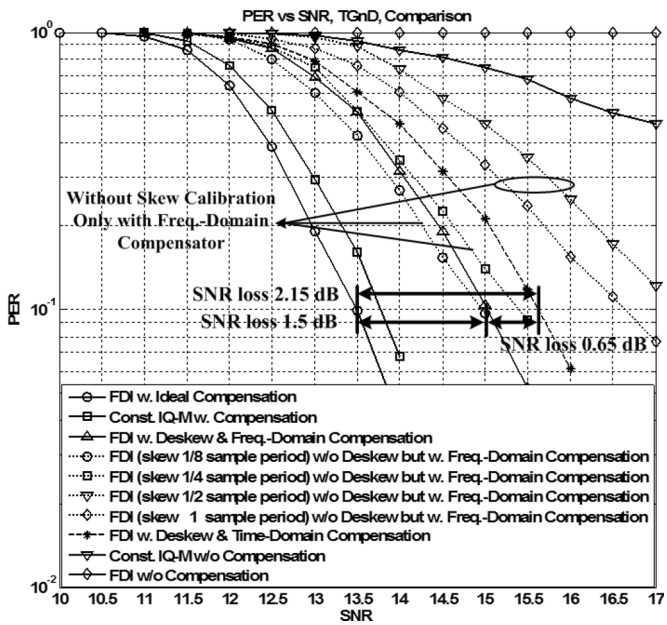


Fig. 16. PER versus SNR, with a worse filter mismatch, 1 dB gain error, 15° phase error and TGnD fading channel.

functions as required. In Fig. 16, the conditions of frequency-selective fading are TGnD [27]. The FDI condition is 1 dB gain error, 15° phase error and a worse filter mismatch [9], [14] with skew periods of 1, 1/2, 1/4 and 1/8 of the sample period. Fig. 16 shows the following scenarios: "FDI w. Ideal Compensation" refers to a system with perfect compensation; "FDI w/o Compensation" means that the compensation scheme is not applied to the system; and "FDI (skew 1/8 sample period) w/o Deskew but w. Freq.-Domain Compensation" indicates that the skew period of the FDI condition is 1/8 of the sample period and the time-domain skew calibration scheme is not used, only the frequency-domain I/Q compensator is applied; "FDI w. Deskew & Time-Domain Compensation" means that after the time-domain skew calibration scheme, a typical time-domain I/Q compensator is used instead of the proposed frequency-domain compensator; and "FDI w. Deskew & Freq.-Domain Compensation" means that after the time-domain skew calibration scheme, the frequency-domain I/Q compensator in (20) is applied. Since a

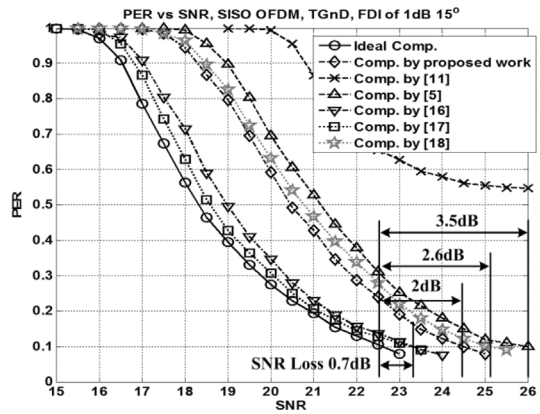


Fig. 17. PER versus SNR in SISO-OFDM Platform with TGnD and a worse FDI of 1 dB 15° [5], [11], [16]–[18].

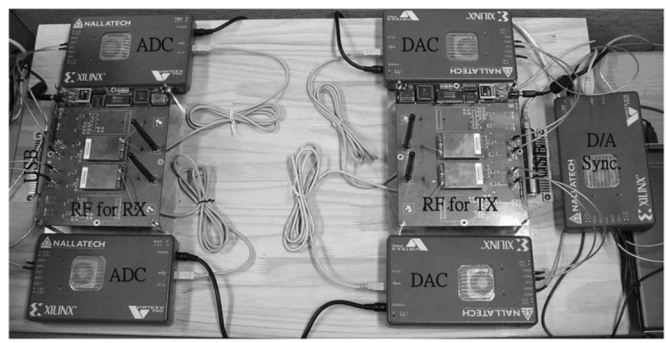


Fig. 18. SDR platform for a 2×2 MIMO-OFDM system.

1/8 skew of filter mismatches is not critical, we only consider skews of 1, 1/2 and 1/4 sample periods in the design. With both skew calibration and frequency-domain compensation, this work proposes a 1.5 dB SNR loss to ensure a $\mathrm{PER} \leq 10\%$ and a $\geq$47 dB IRR per antenna. If FDI distortions are the same in every packet, then a $>$70 dB IRR can also be achieved through more packets. For a robust comparison, the proposed design and other researches [5], [11], [16]–[18] were all ported to a SISO-OFDM platform in the TGnD channel (RMS: 50 ns, 8 taps) and the worse FDI of 1 dB gain error and 15° phase error. Those SNR losses are: 1) 3.5 dB [5]; 2) 0.7 dB [16], [17]; 3) 2.6 dB [18]; and 4) 2 dB (this work), as shown in Fig. 17.

For algorithmic verification, a 2×2 software-defined radio (SDR) was constructed, as shown in Fig. 18. The field-programmable gate array (FPGA) chips (Xilinx Virtex-II) with on-board 14-bit digital-to-analog (D/A) and analog-to-digital (A/D) converters serve as the interface between the in-house RF modules and the software. The packets are generated using MATLAB and then transmitted to RF front-ends through 14-bit D/A convertors. In order to make MIMO transmissions coherent, an additional D/A module acts as a hardware trigger controlling all D/As coherently at TX. After down-converting the RF signals into baseband at the receiver, analog signals are fed into four 14-bit A/Ds for quantization. The proposed algorithm then processes the quantized signals using software (MATLAB). In this platform, we used MATLAB to generate skewed I-path and Q-path signals in TX for creating filter mismatch. The gain and phase errors were $\sim$0.9 dB and $\sim 10°$, respectively. We employed an $8\times$ system clock to simulate

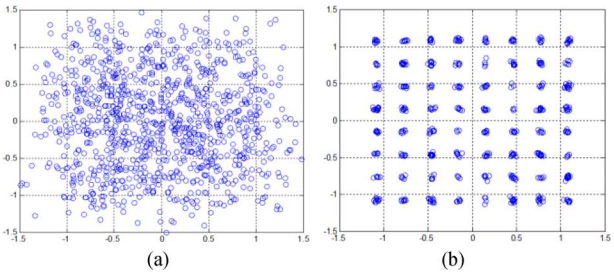


Fig. 19. Measured 64-QAM constellations in the 1st receiver antenna with 0.9 dB gain error, 10° phase error, a normalized skew period of ~ 0.4 and 50.9 dB IRR: (a) without compensation and (b) with compensation.

MPRCG in the FPGA because the FPGA cannot realize our delay chain. Carrier synchronization and channel estimation [32] have also been included. The measured 64-QAM constellations in the first receiver antenna at RX are plotted in Fig. 19. The measured IRR is 50.9 dB, which is better than the 47 dB in MATLAB because the channel fading in the SDR platform is much simpler than in the TGnD channel. The measured EVMs with and without compensation were -1.698 dB and -23.064 dB, respectively. Both simulations and measurements suggest that the proposed 2×2 MIMO-OFDM receiver overcomes the problems of frequency-dependent I/Q imbalances, and is suitable for a 4×4 MIMO-OFDM receiver.

B. Complexity Discussion

Table III summarizes the comparison of design features in the TGnD channel (RMS: 50 ns, 8 taps) and the worse FDI of 1 dB gain error and 15° phase error, e.g., system specification, converged cycles, computational efforts, SNR losses and gate counts. By using time-domain least-squares method for FDI cancellation via known preamble [5], a total of 208 multiplications/divisions and 191 additions/subtractions are required in a 64 pt FFT-based OFDM system with perfect CFR. A FII is estimated via long preambles [11] requiring around 258 multiplications/divisions and 252 additions/subtractions in an OFDM system with 64 subcarriers. Taking the compensation into consideration, the total numbers of multiplications/divisions and additions/subtractions required are 578 and 380. Besides, two filter-based methods result in low SNR losses, but they require additional computational complexity: 1) a CSAD [16] with $3\times$ upsampling where the length of the de-correlating adaptive filters is 3 costs about 1848 multiplications/divisions and 1176 additions/subtractions; 2) a Wiener-based solution [17] using multiplications and matrix inverses requires over 20 k multiplications/divisions and 30 k additions/subtractions for estimation and compensation. With a single-tap matrix filter inversion, a blind-based FDI compensation [18] needs 30 000 symbols, 13 440 k multiplications/divisions and 9600 k additions/subtractions. The proposed CRI-based estimation and skew calibration require 176 multiplications/divisions and 294 additions/subtractions, including interpolation and the moving average. According to (20), 56 multiplications/divisions and 56 additions/subtractions are needed to compensate for an OFDM symbol with 56 data subcarriers. In total, each OFDM symbol requires 232 multiplications and 350 additions/subtractions to remove FDI distortions over the frequency domain. Compared with these solutions, the proposed method needs only 4 short preambles and 4 long preambles and requires the lowest computational effort.

For a fair comparison of VLSI implementations, we focus on total gate counts instead of area as the chip area is affected by technology, cell library, design rules, utilization, floorplan, routing scheme, and power width. The MIMO parts of multiplexers, D-latches, controller and address generator (in Table II) is reduced to cost 4.6 k gates and 618 bytes of SRAM are utilized to buffer one OFDM symbol after IEEE 802.11a (SISO-OFDM) porting with 14-bit precision. For such a SISO-OFDM system, a $2\times$ gated clock is sufficient and easy to implement via differential circuits (11 gates)—the proposed multiphase and multi-rate clock generator (MPRCG) is not required. The total gate counts and memory then become $32.2\text{k}\ (=\ 27.6\text{k} + 4.6\text{k})$ and 714 bytes (96 bytes of ROM included). It occupies 1170 flip-flops and 1968 LUTs as implemented by a Virtex-II FPGA. Two solutions for IEEE 802.11a systems are: an I/Q imbalance compensator [11] costing 59.8 k gates in UMC 0.18 um 1P6M digital CMOS technology, and an I/Q imbalance corrector (14-bit precision) [16] implemented by a Virtex-IV FPGA with 2267 flip-flops and 2510 LUTs (51.2 k gates shown using XFLOW of Xilinx tools). In comparison, the proposed solution is not only cost-effective, but also ensures that a 4×4 MIMO-OFDM receiver functions properly under FDI distortions.

VI. Conclusion

This study presents a cost-effective preamble-assisted algorithm and its implementation for frequency-dependent I/Q imbalance to deal with mismatches of filters, gains, and phases in a 4×4 MIMO-OFDM receiver. With the proposed skew calibrator and a CRI-based estimator, only 4 short preambles and 4 long preambles are needed to achieve over 47 dB IRR. Simulations and measurements also indicate that the proposed scheme can reduce FDI distortions with 1 dB gain errors, 15° phase errors and a worse filter mismatches [9], [14] to maintain $\text{PER} \leq 10\%$ in frequency-selective fading. In VLSI implementations, our all-digital MPRCG ensures coherence of I/Q timing via multiphase A/D clocking and supports fast DFS to minimize the hardware cost, requiring just one complex multiplier and one complex divider in the design. In addition, this work is compatible with new specifications proposed by the IEEE 802.11ac [22] study group. Therefore, system performance can be improved using the proposed solution to relax the analog frontend specification, and thus, enable high levels of integration.

Appendix

A. Divider-Free Arc-Tangent

An arc-tangent function is required to determine the sign of the skew period in (22). Due to the high nonlinearity of arc-tan characteristics, it is not straightforward to realize this function. A divider-free arc-tan solution based on logarithms was built, as shown in Fig. 20. It consists of two lookup tables (LUT), a

TABLE III
COMPARISON OF THE DESIGNED FEATURES IN THE TGnD CHANNEL AND THE WORSE FDI OF 1-dB GAIN ERROR AND 15° PHASE ERROR

	Ref. [5]	Ref. [11]	Ref. [16]	Ref. [17]	Ref. [18]	**Proposed Work**
System Specification	SISO-OFDM	SISO-OFDM + 64QAM	SISO-OFDM + 64QAM	SISO-OFDM + 64QAM	SISO-OFDM + 64QAM	**MIMO-OFDM + 64 QAM (4×4 system)**
Method	Time-Domain Least-Square Approach	Time-Domain Compensated Scheme	CSAD Filter	Wiener Filter	Adaptive Filter	**CRI-based Estimation & Skew Calibration**
Required Format	Known Preambles	Long Preambles	None	None	None	**Short + Long Preambles**
Converged Cycles (# of Symbols)	1	1	3	N/A	30000	**4 Short + 4 Long**
SNR Loss	3.5 dB	N/A	0.7 dB	0.7 dB	2.6 dB	**1.5 dB 2 dB (*1)**
# of Multiplication/Division	208	578	1848	>20*k*	13440*k*	**232**
# of Additions/Subtraction	191	380	1176	>30*k*	9600*k*	**350**
Gate Counts	N/A	59.8k	51.2k	N/A	N/A	**32.2k (*2) 45.7k (*3)**

Note 1: (*1) means the SNR loss in SISO-OFDM platform with a worse FDI of 1 dB, 15° in the TGnD channel.
Note 2: (*2) means the total gates in the proposed SISO-OFDM receiver.
Note 3: (*3) means the total gates in the proposed 4×4 MIMO-OFDM receiver.

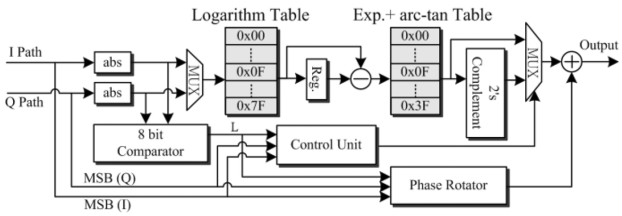


Fig. 20. Architecture of divider-free arc-tan.

subtractor to calculate the difference, a comparator to compare |I| and |Q|, and a phase rotator to rotate the result into the correct phase. The first LUT is used to convert the input number into a logarithmic form. The exponential table and arc-tan table together make up the second LUT to transfer the difference into $\theta°$. To minimize the size of the LUTs, the I-Q plane is divided into eight sections based on the sign of I and Q and on whether |I| is less than or greater than |Q|. The phase rotator will rotate by $\theta°$ to the correct phase, depending on the section. The phase region of the divider-free arc-tan is given by (25), shown at the bottom of the page. In Fig. 20, the comparison result L (L = 1 when $|I| > |Q|$ and L = 0 when $|I| \leq |Q|$) and the MSBs of the I/Q signals (MSB(I) and MSB(Q)) are used to decide whether the 2's complement of the phase is required, and also to determine the appropriate output region.

B. Table of Abbreviations

Abbreviation	Full name
CFO	Carrier frequency offset
CFR	Channel frequency response
CLP	Common long preamble
CRI	Cross-ratio imparity
CSP	Common short preamble
DCO	Digitally controlled oscillator
DFS	Dynamic frequency scaling
DLL	Delay-locked loops
FDI	Frequency-dependent I/Q imbalance
FII	Frequency-independent I/Q imbalance
IRR	Image rejection ratio
LPF	Low-pass filter
LUT	Lookup tables
MIMO-OFDM	Multiple-input multiple-output orthogonal frequency division multiplexing
MLP	MIMO long preamble
MPRCG	Multiphase and multi-rate clock generator
MSP	MIMO short preamble
PER	Packet-error rate
PLL	Phase-locked loops
TDC	Time-to-digit converter
VLP	Virtual long preamble

ACKNOWLEDGMENT

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$$\theta_i = \tan^{-1}\left(\frac{Q_i}{I_i}\right) = \begin{cases} \tan^{-1}\left(e^{\log|Q_i|-\log|I_i|}\right)+0°, & \text{where } |I_i|>|Q_i| \& \{\text{sign}(I_i),\text{sign}(Q_i)\}=\{+,+\} \\ -\tan^{-1}\left(e^{\log|I_i|-\log|Q_i|}\right)+90°, & \text{where } |I_i|<|Q_i| \& \{\text{sign}(I_i),\text{sign}(Q_i)\}=\{+,+\} \\ \tan^{-1}\left(e^{\log|Q_i|-\log|I_i|}\right)+180°, & \text{where } |I_i|>|Q_i| \& \{\text{sign}(I_i),\text{sign}(Q_i)\}=\{-,-\} \\ -\tan^{-1}\left(e^{\log|I_i|-\log|Q_i|}\right)+270°, & \text{where } |I_i|<|Q_i| \& \{\text{sign}(I_i),\text{sign}(Q_i)\}=\{-,-\} \\ -\tan^{-1}\left(e^{\log|Q_i|-\log|I_i|}\right)+360°, & \text{where } |I_i|>|Q_i| \& \{\text{sign}(I_i),\text{sign}(Q_i)\}=\{+,-\} \\ \tan^{-1}\left(e^{\log|I_i|-\log|Q_i|}\right)+270°, & \text{where} |I_i|<|Q_i| \& \{\text{sign}(I_i),\text{sign}(Q_i)\}=\{+,-\} \\ -\tan^{-1}\left(e^{\log|Q_i|-\log|I_i|}\right)+180°, & \text{where } |I_i|>|Q_i| \& \{\text{sign}(I_i),\text{sign}(Q_i)\}=\{-,+\} \\ \tan^{-1}\left(e^{\log|I_i|-\log|Q_i|}\right)+90°, & \text{where} |I_i|<|Q_i| \& \{\text{sign}(I_i),\text{sign}(Q_i)\}=\{-,+\} \end{cases} \quad (25)$$

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