Journal of ELECTRONIC MATERIALS, Vol. 42, No. 8, 2013
DOI: 10.1007/s11664-013-2616-x

Investigation of Characteristics of Al_2O_3/n-$In_xGa_{1-x}As$ (x = 0.53, 0.7, and 1) Metal–Oxide–Semiconductor Structures

HAI-DANG TRINH,[1,5] YUEH-CHIN LIN,[1] CHIEN-I KUO,[1] EDWARD YI CHANG,[1,2] HONG-QUAN NGUYEN,[1] YUEN-YEE WONG,[1] CHIH-CHIEH YU,[3] CHI-MING CHEN,[4] CHIA-YUAN CHANG,[4] JYUN-YI WU,[4] HAN-CHIN CHIU,[4] TERRENCE YU,[4] HUI-CHENG CHANG,[4] JOSEPH TSAI,[4] and DAVID HWANG[4]

1.—Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan. 2.—Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan. 3.—Instrument Technology Research Center, Hsinchu 30010, Taiwan. 4.—Taiwan Semiconductor Manufacturing Company Limited, Hsinchu Science Park, Hsinchu 30010, Taiwan. 5.—e-mail: trinhhaidang@gmail.com

The electrical properties of Al_2O_3/n-InGaAs metal–oxide–semiconductor capacitors (MOSCAPs) with In content of 0.53, 0.7, and 1 (InAs) have been investigated. Results show small capacitance–voltage (C–V) frequency dispersion in accumulation (1.70% to 1.85% per decade) for these MOSCAPs, mostly being assigned to border traps in Al_2O_3. With higher In content, shorter minority-carrier response time and smaller C–V hysteresis are observed. The reduction of C–V hysteresis might be related to the reduction of Ga-bearing oxides in Al_2O_3/InGaAs interfaces as indicated by x-ray photoelectron spectroscopy.

Key words: ALD Al_2O_3, surface treatment, InGaAs, InAs, MOSCAPs

INTRODUCTION

High-k/III–V structures have been extensively studied recently to realize complementary metal–oxide–semiconductor (MOS) technologies at the 16-nm node and beyond.[1] However, regardless of long-term efforts by the community, the high-k/III–V interface trap density (D_{it}) still remains a challenge. Passivation of high-k/III–V interfaces is always needed to reduce D_{it}. Recently, reports have indicated that the quality of high-k/III–V interfaces not only depends on the passivation method but is also influenced by the III–V compounds themselves.[2,3] Study of high-k/n-InGaAs structures with In content from 0 to 0.53 showed a significant reduction of capacitance–voltage (C–V) frequency dispersion at the accumulation region as the In content reaches 0.53.[3] Besides, some recent reports showed that the frequency dispersion in accumulation in high-k/$In_{0.53}Ga_{0.47}As$ MOS capacitors (MOSCAPs) is closely related to the traps inside the gate oxide, or so-called border traps.[4–6] Simulations have been done on $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs to study the effect of border traps on the frequency dispersion in the accumulation capacitance.[5,6] In this work, we intend to study the electrical properties of high-k/n-InGaAs structures in which the In content varies from 0.53 to 1. The purpose of the study is to investigate the electrical properties of atomic layer deposition (ALD) Al_2O_3/n-InGaAs MOSCAP structures related to border traps and interface traps, such as the frequency dispersion and hysteresis.

(Received December 13, 2012; accepted April 13, 2013; published online May 29, 2013)

EXPERIMENTAL PROCEDURES

InGaAs wafers with different In content used in the study were (a) 100 nm $In_{0.53}Ga_{0.47}As$, (b) 5 nm $In_{0.7}Ga_{0.3}As$/10 nm $In_{0.53}Ga_{0.47}$, and (c) 5 nm InAs/3 nm $In_{0.7}Ga_{0.3}As$/10 nm $In_{0.53}Ga_{0.47}As$ epilayer stacks grown on n^+-type InP substrates by molecular beam epitaxy and supplied by IQE Inc. The top layer in each structure was a nominal 2×10^{17} cm^{-3} Si-doped In(Ga)As material. Wafers

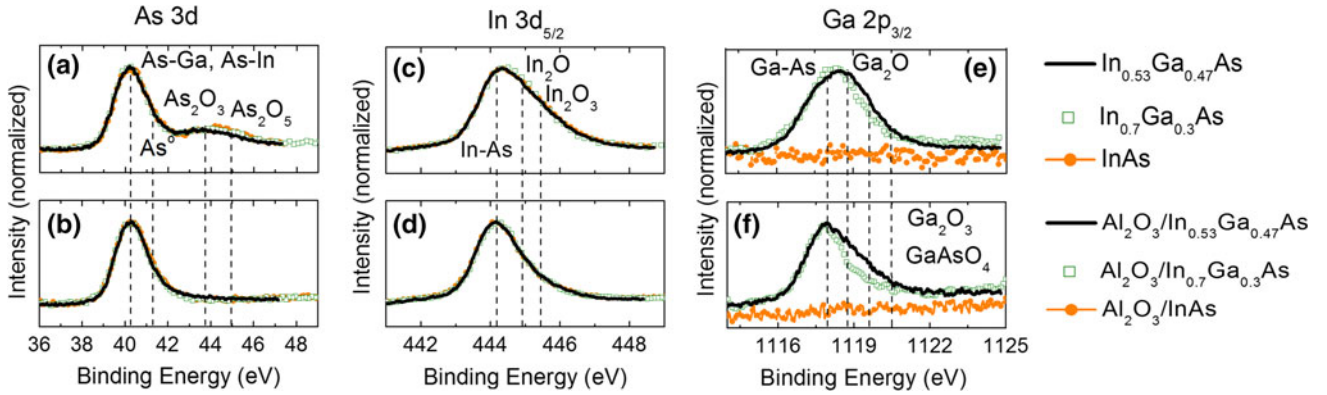

Fig. 1. As 3d, In $3d_{5/2}$, and Ga $2p_{3/2}$ XPS spectra of samples: bare native-oxide-covered (a) $In_{0.53}Ga_{0.47}As$, (b) $In_{0.7}Ga_{0.3}As$, and (c) InAs surfaces; and (d) $Al_2O_3/In_{0.53}Ga_{0.47}As$, (e) $Al_2O_3/In_{0.7}Ga_{0.3}As$, (f) and Al_2O_3/InAs interfaces after using HCl + TMA treatment followed by ALD of 1.5 nm Al_2O_3.

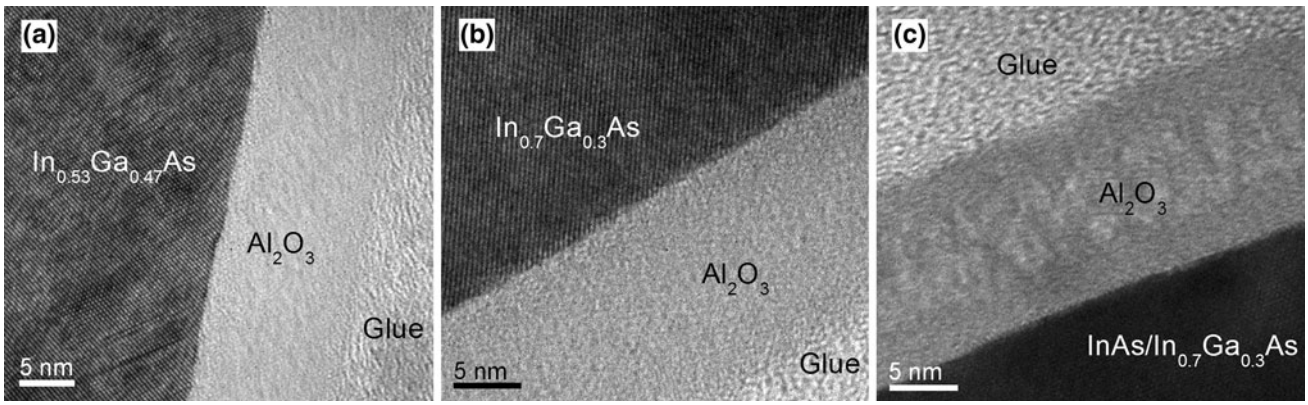

Fig. 2. HRTEM micrographs of MOSCAP structures: (a) $Al_2O_3/In_{0.53}Ga_{0.47}As$, (b) $Al_2O_3/In_{0.7}Ga_{0.3}As$, and (c) Al_2O_3/InAs.

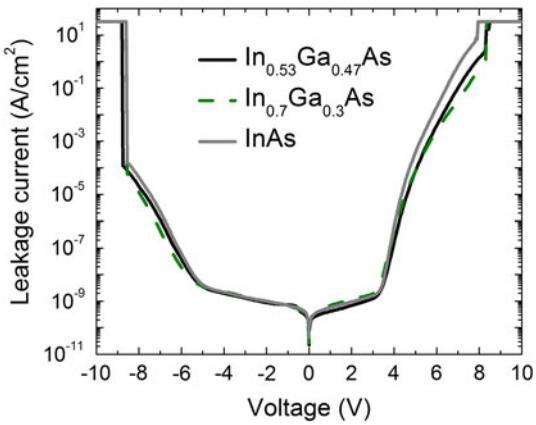

Fig. 3. *I–V* characteristics of MOSCAP structures.

were degreased by acetone and isopropanol before dipping in 4% HCl solution for 1 min to remove native oxides. They were then loaded into the ALD system for Al_2O_3 deposition. In the ALD chamber, *in situ* trimethylaluminum (TMA) clean was used by employing 10 TMA/N_2 pulses before the deposition of 120 cycles of Al_2O_3 at 300°C using TMA and H_2O as precursors. *In situ* TMA cleaning is effective for further removal of native oxides via ligand-exchange reactions between TMA and InGaAs native oxides.[7–10] Besides, HCl + TMA treatment was reported to give a good-quality Al_2O_3/n-InAs interface.[8,11] After oxide deposition, samples were post-deposition annealed (PDA) at 400°C in H_2/N_2 (1:1) gas for 10 min. Finally, Pt/Au gate metal and Au/Ge/Ni/Au back-side contact metal were deposited, followed by post-metal-deposition annealing (PMA) at 400°C in N_2 gas for 30 s. The MOSCAPs were characterized by multifrequency *C–V*, conductance–voltage (*G–V*), and current–voltage (*I–V*) measurements using an Agilent HP 4284A precision LCR meter and a Keithley 4200 semiconductor analyzer, respectively. The Al_2O_3/InGaAs, InAs interfaces were analyzed by x-ray photoelectron spectroscopy (XPS) measurements and high-resolution transmission electron microscopy (HRTEM).

RESULTS AND DISCUSSION

Figure 1 illustrates the As 3d, In $3d_{5/2}$, and Ga $2p_{3/2}$ XPS spectra of the native-oxide-covered

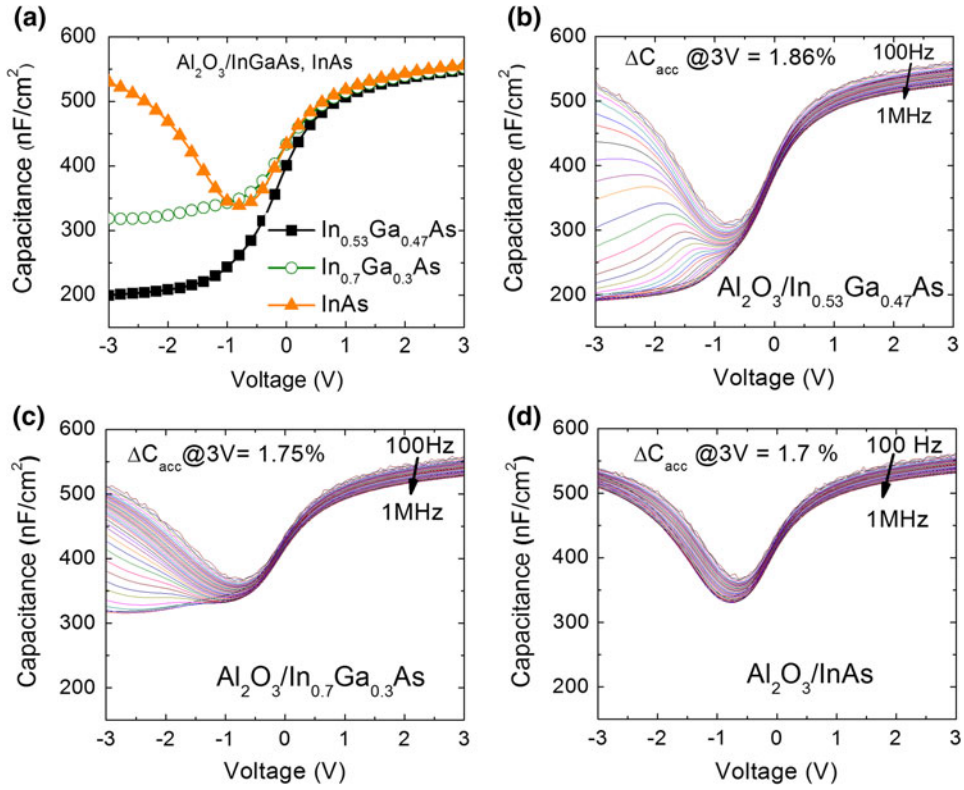

Fig. 4. (a) *C–V* response at 1 MHz of $Al_2O_3/In_xGa_{1-x}As$ MOSCAPs; (b–d) multifrequency *C–V* responses of $Al_2O_3/In_xGa_{1-x}As$ MOSCAPs.

$In_{0.53}Ga_{0.47}As$, $In_{0.7}Ga_{0.3}As$, and InAs surfaces (Fig. 1a, c, e) and $Al_2O_3/In_{0.53}Ga_{0.47}As$, $Al_2O_3/In_{0.7}Ga_{0.3}As$, and Al_2O_3/InAs interfaces after using HCl + TMA treatment following deposition of 1.5 nm Al_2O_3 (Fig. 1b, d, f). It can be seen that, after surface treatment and oxide deposition, As_2O_3 and As_2O_5 oxides reduced to below the detection level of XPS for all samples, as shown in Fig. 1b. In- and Ga-related oxides of these samples were also significantly reduced, as indicated in Fig. 1d, f. The As 3d and In $3d_{5/2}$ spectra after normalization show very similar profiles. On the other hand, the Ga $2p_{3/2}$ spectra show reduction of the intensity at the Ga-O sides with increase of the In content, especially for the samples after surface treatment and high-k deposition (Fig. 1c, f). This observation indicates that the relative ratios of Ga oxides to the bulk Ga-As decreased with increase of the In content. In addition, this reduction of Ga-related oxides is more significant for the high oxidation states, i.e., Ga_2O_3 and $GaAsO_4$, as shown in Fig. 1f.

Figure 2 shows HRTEM micrographs of the Al_2O_3/InGaAs and Al_2O_3/InAs/InGaAs structures. Normally, air-exposed Ga(In)As surfaces have native oxide layers with thickness above 2.0 nm to 3.0 nm.[12,13] Here, the samples show an abrupt transition from $In_{0.53}Ga_{0.47}As$, $In_{0.7}Ga_{0.3}As$, and InAs layers to Al_2O_3 without an interface oxide layer. The highly ordered lattice images at the interface and the smooth surface suggest that the structures exhibit good thermal stability after PDA at 400°C. The Al_2O_3 films are amorphous as shown in the figure, and the thickness of the oxide films estimated from TEM micrographs is about 12.0 nm. The current density–voltage (J–V) characteristics of the samples are presented in Fig. 3. All samples exhibit similar, low leakage currents with breakdown field of 7.2 MV/cm. This indicates that the ALD Al_2O_3 is a good-quality oxide layer.

The *C–V* responses of the MOSCAPs at frequency of 1 MHz are shown in Fig. 4a. When the In content increases, the *C–V* responses change from high-frequency to low-frequency *C–V* behavior. For the case of InAs, a strong inversion layer is observed at the high frequency of 1 MHz. This behavior was observed before[14] and is more obvious in this experiment. The variation of the *C–V* curves in the depletion/inversion regions can be explained by the increase of the intrinsic carrier concentration n_i in InGaAs with increase of the In content (from $\sim 6.3 \times 10^{12}$ cm^{-3} for $In_{0.53}Ga_{0.47}As$ to $\sim 10^{15} \times$ cm^{-3} for InAs[15]). This would result in a decrease of the minority-carrier response time τ_R (or an increase of the minority-carrier generation rate) according to the relationship $\tau_R = \tau_T/n_i$,[16] where τ_T is the carrier lifetime.

The multifrequency *C–V* responses of the MOSCAPs shown in Fig. 4b–d indicate that the frequency dispersion in the accumulation region is small and very similar (1.85%, 1.75%, and 1.70% per decade for x = 0.53, 0.7, and 1, respectively) for all the samples. This behavior seems to be different for

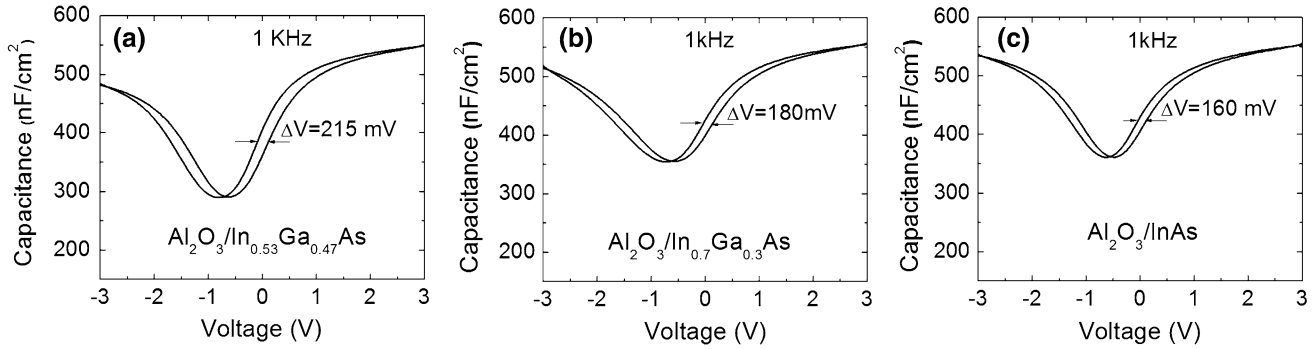

Fig. 5. Bidirectional *C–V* responses of $Al_2O_3/In_xGa_{1-x}As$ MOSCAP structures with different In contents at frequency of 1 kHz.

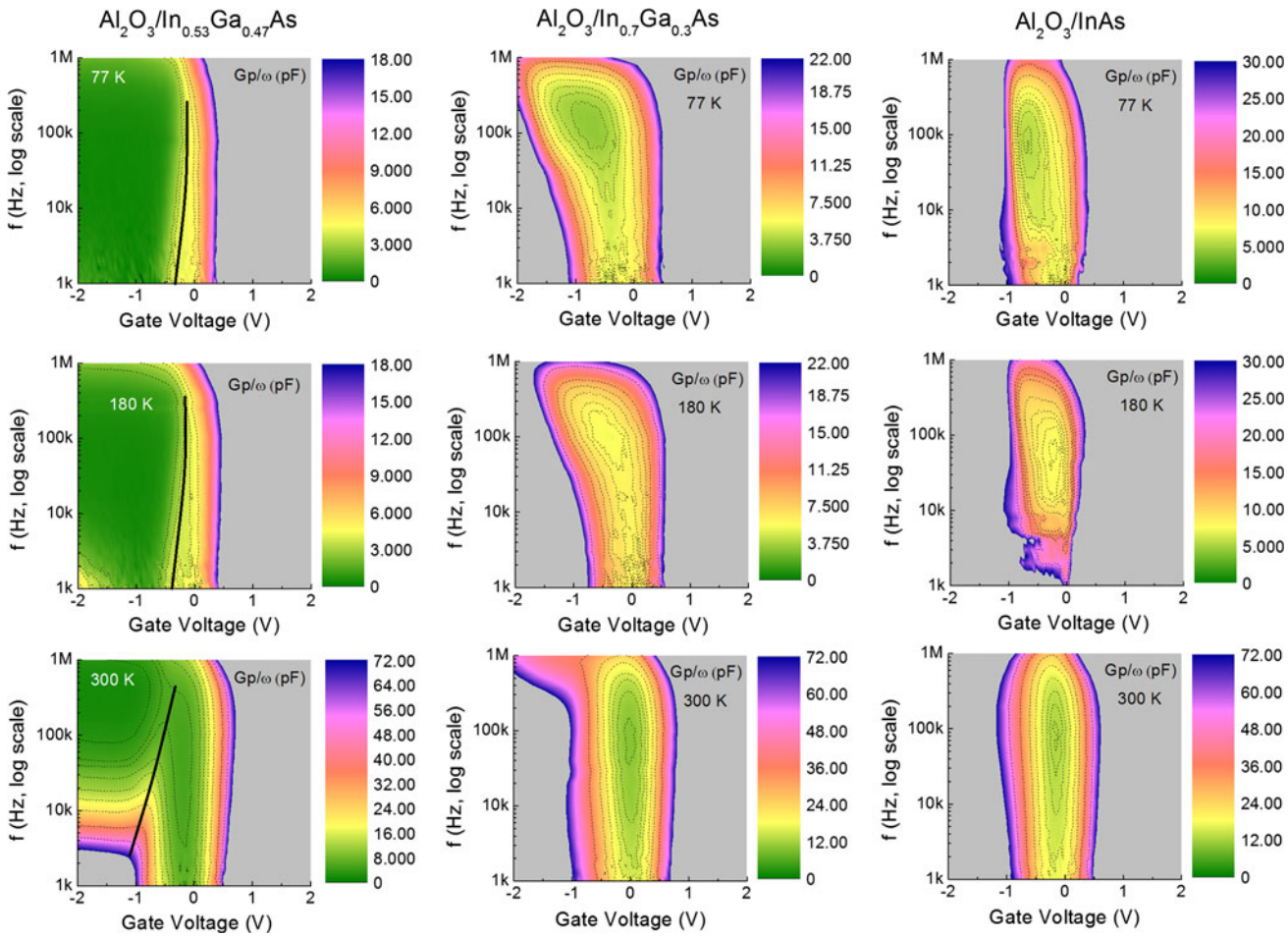

Fig. 6. Conductance contours $G_p/\omega(f, V)$ at different temperatures (77 K, 180 K, and 300 K) for $Al_2O_3/In_xGa_{1-x}As$ MOSCAP structures.

high-*k*/$In_xGa_{1-x}As$ structures with $x < 0.53$, for which the frequency dispersion is strongly dependent on the In content.[3] This result suggests that, for high-*k*/InGaAs with high In content, interface traps do not seem to contribute to the frequency dispersion in the accumulation regime. Study of Al_2O_3/*n*-InAs structures with various surface treatments also showed that the frequency dispersion in the accumulation regime is small, even for untreated samples with high D_{it} values.[8,11] In the equilibrium state, with doping concentration N_D of 2×10^{17} cm^{-3}, the Fermi level is located very close to the conduction-band edge (estimated about 0.0013 eV below E_C) for $In_{0.53}Ga_{0.47}As$ and ~0.022 eV above E_C for InAs.[15,17] Thus, in the accumulation region, due to the band bending, the Fermi level at Al_2O_3/InGaAs and Al_2O_3/InAs interfaces would be located within the conduction band. The interface states inside the conduction band have too short response time, thus, they can follow

the frequencies in the range of 1 kHz to 1 MHz used in typical measurements.[5,18] Thus, the contribution of traps to the frequency dispersion cannot be observed with traditional C–V measurements. In this context, the frequency dispersion is mostly due to the contribution of border traps which are located near the interface and inside the gate oxide. This kind of trap has a long response time and would interact with conductance-band electrons via tunneling.[4] In fact, the effects of border traps on Al_2O_3/InGaAs and Al_2O_3/InAs structures are very similar, as indicated by the very similar frequency dispersion values.

Bidirectional C–V responses show a reduction of hysteresis with increase of the In content (Fig. 5). In this experiment, the contribution of the gate oxide to the hysteresis is expected to be the same for all samples, because the thermal processes were performed at a relatively low temperature of 400°C to minimize the effect of channel material diffusion into the gate oxide. Therefore, the effect of interface traps on hysteresis will decrease with increasing In content. This result could be related to the reduction of Ga-related oxides with increase of the In content, especially Ga^{3+} oxides as discussed in the analyses of the XPS spectra. Such reduction of Ga oxides leading to the improvement of C–V characteristics has also been seen for $HfO_2/In_xGa_{1-x}As$ structures with x in the range from 0 to 0.53.[3,19] First-principles calculations showed that the large amount of Ga-O and As-As bonds at the high-k/Ga(In)As interfaces would cause a high interface state density.[20] Experimentally, it was also reported that reduction of Ga_2O_3 by using a Si interface passivation layer could result in a significant improvement of the electrical properties of Al_2O_3/GaAs MOS structures.[21] The other possible explanation for this phenomenon is a decrease of the InGaAs bandgap with increase of the In content, as proposed and explained by an empirical model.[2,22] According to this model, when the In content increases, the bandgap decreases, which would lead to a reduction of the total density of traps in the bandgap as well as their effect on the electrical behavior of high-k/InGaAs structures.

Temperature-dependent C–V and G–V measurements were performed at 77 K, 180 K, and 300 K for all samples. Based on the C–V and G–V data, the parallel conductance was determined and the conductance maps of G_p/ω were plotted to trace the movement of the Fermi level.[23] Figure 6a shows the conductance maps G_p/ω at different temperatures for the Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ structure. Except for weak inversion C–V responses at frequency below 4 kHz at room temperature, high-frequency curves are observed across the whole range of measured frequencies (1 kHz to 1 MHz) and temperatures (data not shown here). This confirms the accuracy of the extracted conductance values.[16] From the conductance map, the conductance peak maximum can shift with the gate bias (solid lines, Fig. 4a, conductance contours), indicating unpinning of the Fermi level in the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP. From the relationship between the trap response time and measured frequency,[24] these measurements enable us to extract the interface trap density, D_{it}, at different energy positions inside the bandgap.[16,23,25] In this case, D_{it} values from 10^{12} eV^{-1} cm^{-2} to 2.5×10^{11} eV^{-1} cm^{-2} located in the energy range from 0.4 eV to 0.70 eV above the $In_{0.53}Ga_{0.47}As$ valence-band minimum are obtained (here, a value of the capture cross-section of 10^{-14} cm^2 was taken to determine the locations of the traps).

Figure 6b and c show the conductance maps for the $Al_2O_3/In_{0.7}Ga_{0.3}As$ and $Al_2O_3/InAs$ structures, respectively. For these two structures, high-frequency C–V responses were not observed even when the temperature was decreased to 77 K (data not shown here). Since inversion layers always respond to the full range of measured frequencies and temperatures, their contribution to the conductance will affect the accuracy of the conductance method.[26] As can be seen in the figures, the conductance contours are closed due to the contribution of inversion carriers. Thus, the extracted value of D_{it} is an overestimate and the traces of the Fermi level could not be observed. To eliminate the contribution of the inversion layer from the extraction of the D_{it} value, application of the full conductance method is needed in future study.[26]

CONCLUSIONS

We studied material and electrical characteristics of ALD $Al_2O_3/In_xGa_{1-x}As$ structures with In content of 0.53, 0.7, and 1. XPS analysis shows a significant reduction of native oxides after HCl + TMA treatment, as supported by HRTEM imaging. Multifrequency C–V responses show low-frequency dispersion in the accumulation region. This frequency dispersion seems to be mostly due to border traps in the oxide rather than due to interface traps. The C–V hysteresis shows a reduction of the interface traps with increasing In content, which could be related to the reduction of Ga-related oxides. The conductance method showed a low interface trap density distribution at energy positions from 0.4 eV to 0.70 eV above the valence band of $In_{0.53}Ga_{0.47}As$. The conductance contours showed free movement of the Fermi level with the gate bias for the case of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ structure. However, for the cases of $Al_2O_3/In_{0.7}Ga_{0.3}As$ and $Al_2O_3/InAs$, traces of Fermi level movement were not observed due to the inversion layer contribution.

ACKNOWLEDGEMENTS

This work was supported by the NCTU-UCB I-RiCE Program and sponsored by the Taiwan

National Science Council under Grant No. NSC-102-2911-I-009-301.

REFERENCES

1. R. Chau, S. Datta, and Majumdar, *Dig. IEEE CSICS* 17 (2010).
2. P.D. Ye, *J. Vac. Sci. Technol. A* 26, 697 (2008).
3. É. O'Connor, S. Monaghan, R.D. Long, A. O'Mahony, I.M. Povey, K. Cherkaoui, M.E. Pemble, G. Brammertz, M. Heyns, S.B. Newcomb, V.V. Afanas'ev, and P.K. Hurley, *Appl. Phys. Lett.* 94, 102902 (2009).
4. E.J. Kim, L. Wang, P.M. Asbeck, K.C. Saraswat, and P.C. McIntyre, *Appl. Phys. Lett.* 96, 012906 (2010).
5. Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P.C. McIntyre, P.M. Asbeck, M.J.W. Rodwell, and Y. Taur, *IEEE Electron Device Lett.* 3, 485 (2011).
6. G. Brammertz, A. Alian, D.H.C. Lin, M. Meuris, M. Caymax, and W.E. Wang, *IEEE Trans. Electron Devices* 58, 3890 (2011).
7. H.D. Trinh, E.Y. Chang, P.W. Wu, Y.Y. Wong, C.T. Chang, Y.F. Hsieh, C.C. Yu, H.Q. Nguyen, Y.C. Lin, K.L. Lin, and M.K. Hudait, *Appl. Phys. Lett.* 97, 042903 (2010).
8. H.D. Trinh, E.Y. Chang, Y.Y. Wong, C.C. Yu, C.Y. Chang, Y.C. Lin, H.Q. Nguyen, and B.T. Tran, *Jpn. J. Appl. Phys.* 49, 111201 (2010).
9. C.L. Hinkle, A.M. Sonnet, E.M. Vogel, S. McDonnell, G.J. Hughes, M. Milojevic, B. Lee, F.S. Aguirre-Tostado, K.J. Choi, H.C. Kim, J. Kim, and R.M. Wallace, *Appl. Phys. Lett.* 92, 071901 (2008).
10. M. Milojevic, C.L. Hinkle, F.S. Aguirre-Tostado, H.C. Kim, E.M. Vogel, J. Kim, and R.M. Wallace, *Appl. Phys. Lett.* 93, 252905 (2008).
11. H.D. Trinh, G. Brammertz, E.Y. Chang, C.I. Kuo, C.Y. Lu, Y.C. Lin, H.Q. Nguyen, Y.Y. Wong, B.T. Tran, K. Kakushima, and H. Iwai, *IEEE Electron Device Lett.* 32, 752 (2011).
12. Y.C. Chang, M.L. Huang, K.Y. Lee, Y.J. Lee, T.D. Lin, M. Hong, J. Kwo, T.S. Lay, C.C. Liao, and K.Y. Cheng, *Appl. Phys. Lett.* 92, 072901 (2008).
13. M.M. Frank, G.D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y.J. Chabal, J. Grazul, and D.A. Muller, *Appl. Phys. Lett.* 86, 152904 (2005).
14. Y.C. Wu, E.Y. Chang, Y.C. Lin, C.C. Kei, M.K. Hudait, M. Radosavljevic, Y.Y. Wong, C.T. Chang, J.C. Huang, and S.H. Tang, *Solid-State Electron.* 54, 37 (2010).
15. Material parameters taken from the website: http://www.ioffe.ru/SVA/NSM/.
16. E.H. Nicollian and J.R. Brews, *MOS Physics and Technology* (New York: Wiley, 1982).
17. S.M. Sze and K.K. Ng, *Physics of Semiconductor Devices* (New York: Wiley, 2007).
18. W. Shockley and W.T. Read Jr, *Phys. Rev.* 87, 835 (1952).
19. C.L. Hinkle, E.M. Vogel, P.D. Ye, and R.M. Wallace, *Curr. Opin. Solid State Mater. Sci.* 15, 188 (2011).
20. W. Wang, C.L. Hinkle, E.M. Vogel, K. Cho, and R.M. Wallace, *Microelectron. Eng.* 88, 1061 (2011).
21. C.L. Hinkle, M. Milojevic, B. Brennan, A.M. Sonnet, F.S. Aguirre-Tostado, G.J. Hughes, E.M. Vogel, and R.M. Wallace, *Appl. Phys. Lett.* 94, 162101 (2009).
22. S. Oktyabrsky and P.D. Ye, eds., *Fundamentals of III-V Semiconductor MOSFETs* (New York: Springer, 2010).
23. G. Brammertz, H.-C. Lin, K. Martens, D. Mercier, S. Sioncke, A. Delabie, W.E. Wang, M. Caymax, M. Meuris, and M. Heyns, *Appl. Phys. Lett.* 93, 183504 (2008).
24. G. Brammertz, K. Martens, S. Sioncke, A. Delabie, M. Caymax, M. Meuris, and M. Heyns, *Appl. Phys. Lett.* 91, 133510 (2007).
25. G. Brammertz, H.C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W.E. Wang, M. Caymax, M. Meuris, and M. Heyns, *J. Electrochem. Soc.* 155, H945 (2008).
26. K. Martens, C.O. Chui, G. Brammertz, B.D. Jaeger, D. Kuzum, M. Meuris, M.M. Heyns, T. Krishnamohan, K. Saraswat, H.E. Maes, and G. Groeseneken, *IEEE Trans. Electron Devices* 55, 547 (2008).