InAs/$In_{1-x}Ga_xAs$ Composite Channel High Electron Mobility Transistors for High Speed Applications

Edward Yi Chang[1], Chien-I Kuo[1], Heng-Tung Hsu[2], Chia-Yuan Chang[1]

[1]*Department of Materials Science and Engineering, National Chiao-Tung University*
[1]edc@mail.nctu.edu.tw

[2]*Department of Communications Engineering, Yuan Ze University*

***Abstract*—80-nm InAs channel HEMTs with different lattice matched sub-channels, $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$, have been fabricated. The device with InAs/ $In_{0.7}Ga_{0.3}As$ composite channel exhibits high drain current density (1101 mA/mm), and high transconductance (1605 mS/mm) at drain bias V_{DS} = 0.8 V. The high current gain cutoff frequency (f_t) of 360 GHz and maximum oscillation frequency (f_{max}) of 380 GHz of the device with InAs/ $In_{0.7}Ga_{0.3}As$ were obtained at V_{DS} = 0.7 V in comparison to the InAs/$In_{0.53}Ga_{0.47}$ As channel HEMTs with f_t = 310 and f_{max} = 330 GHz. This is due to the high electron mobility and electron confinement in the InAs/ $In_{0.7}Ga_{0.3}As$ channel. In addition, a low gate delay time 0.84 psec was obtained at V_{DS} = 0.5 V. The excellent performance of the InAs channel HEMTs demonstrated in this study shows great potential for high speed and very low power logic applications with the optimal design of $In_{0.7}Ga_{0.3}As$/InAs/$In_{0.7}Ga_{0.3}As$ composite channel.**

I. INTRODUCTION

Low DC power consumption devices and circuits have always been desired for all kinds of communications systems especially the satellite communications. With the breakthrough in semiconductor hetero-structure technologies, planar III-V compound semiconductor field effect transistors (FETs) or high electron mobility teansistors (HEMTs) have been identified as one of the most attractive devices for such applications. Besides, in order to extend Moore's law well into the next decade, III-V based heterostructure devices is also a potential candidate FETs for low-power logic applications beyond Si CMOS technology in 22 nm node era [1-3].

The excellent RF-performance has been demonstrated by InAlAs/InGaAs HEMTs on InP substrate or GaAs substrate [4-6]. In fact, higher electron mobility and velocity can be realized by reducing of gate length (*Lg*) or increasing of the indium content in the InGaAs channel. Due to the high electron mobility (~ 20000 $cm^2/V \bullet s$), high drift velocity, reasonable energy band gap (0.36 eV), and large conduction band offset in InAs, InAs-channel HEMT is considered very promising for high speed and low power logic applications.

In this study, channel structures of HEMTs with different indium concentration as upper and lower lattice-matched sub-channels, including $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ are fabricated and evaluated for the RF and digital performances.

II. EXPERIMENT

The epitaxial structure of the InAs-channel with different $In_{1-x}Ga_xAs$ cladding layer as the sub-channel ($In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$) HEMTs were grown by molecular beam epitaxy (MBE) on InP substrate, respectively. These sub-channels were applied to minimize the interface roughness scattering and further enhance the electron confinement in the thin strained InAs layer and improve the electron transport properties [7]. In addition, both of these two types of devices used the InP etching stop layer to improve the selectivity of the wet chemical recess etch and provide semiconductor surface passivation on each side of the gate to reduce the trapping effect on the InAlAs surface [8]. With the use of the InP etching stop layer, the lateral recess length was easy to control. A high uniform threshold voltage (V_{th}) was achieved and RF performance was improved using the InP etch layer [9].

For the device fabrication, the active area of the device was isolated by wet etch. Source and drain Ohmic metal were formed with 240-nm-thick Au/Ge/Ni/Au and alloyed by rapid thermal annealing at 250 oC for 30 sec. As a result of the highly Si doped cap, a low Ohmic contact resistance (Rc) and an sheet resistance (Rsh) were obtained by using the transmission line model method. A tri-layer resist system of ZEP-520/PMGI/ZEP520 was used for the E-Beam lithography. The gate-recess was performed precisely by wet chemical etching using succinic acid-based solution because the side-recess spacing played an important role in balancing short-channel effect and frequency response [10]. The Ti/Pt/Au gate metal was formed by evaporation and lift off. The gate length of the T-shaped gate was 80 nm. Fig. 1 shows the cross-sectional scanning electron microscopy (SEM) image of the T-shaped gate resist profile. Finally, devices were passivated using a 100-nm-thick PECVD (plasma enhanced chemical vapor deposition) silicon nitride film.

III. RESULT AND DISSCUSSION

Fig. 2 (a) and 2 (b) shows the current-voltage characteristics of 2 × 50 μm devices of InAs/$In_{0.53}Ga_{0.47}As$ composite channel HEMTs. As observed from the figure, this device can be well pinched off with a threshold voltage of -0.8 V. The fabricated InAs MHEMT shows a drain current density of 834 mA/mm and transconductance, $g_{m,max}$ of 1450 mS/mm at V_{DS} = 0.8 V. On the other hand, the DC characteristics of the InAs/$In_{0.7}Ga_{0.3}As$ composite channel

HEMTs are shown in the Fig. 3 (a) and (b). The drain current density of 1101 mA/mm and $g_{m,max}$ of 1605 mS/mm are observed. The high transconductance was due to higher carrier concentration and superior electron transport properties in the InAs/$In_{0.7}Ga_{0.3}As$ channel. The result indicates that the InAs-channel HEMTs can be operated at low drain bias condition to reduce dc power dissipation and is suitable for low power applications.

The S-parameters of the 2 × 50 μm device were measured from 5 to 80 GHz using on-wafer probing system with HP8510XF network analyzer. A standard Load-Reflection-Reflection-Match (LRRM) calibration method was used to calibrate the measurement system. The parasitic effects (mainly capacitive) due to the probing pads have been carefully removed from the measured S-parameters using the same method as in [11] and the equivalent circuit model in [12]. Fig. 4 shows the frequency dependence of the current gain H_{21}, the power gain MAG/MSG, and the Mason's unilateral gain U of the InAs/$In_{0.53}Ga_{0.47}As$ device measured at V_{DS} = 0.7 V and V_{gs} = -0.4 V. The f_T and f_{max} are 310 and 330 GHz, respectively by extrapolating H_{21} and MAG/MSG by least square fitting with a -20 dB/dec slope. Comparison to the InAs/$In_{0.7}Ga_{0.3}As$ channel device, a very high current gain cut-off frequency f_T of 360 GHz and the maximum oscillation frequency f_{max} of 380 GHz were obtained and the results are shown in Fig. 5. The excellent RF performance of InAs/$In_{0.7}Ga_{0.3}As$ composite channel device is mainly caused by high transconductance.

To characterize such device for high-speed logic applications, the gate delay time (CV/I) or intrinsic speed was also evaluated. C is the total gate capacitance including gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) which extracted from the high frequency S-parameter. V is the applied drain voltage and equal to the power supply voltage (V_{CC}). I is the on-state current with the bias point. According to the definition in [13-14], the gate delay time of both devices were calculated to be 0.87 (InAs/$In_{0.53}Ga_{0.47}As$) and 0.84 (InAs/$In_{0.7}Ga_{0.3}As$) psec at the same drain voltage V_{DS} = 0.5 V, respectively. Fig. 6 shows the comparison of delay time for different types of devices (InAs HEMTs, advanced Si-MOSFETs and InSb HEMTs) as a function of gate length [2, 15]. In this plot, it can be seen that the 80 nm InAs HEMTs exhibits excellent intrinsic speed than the state-of-the-art Si NMOSFETs at the same gate length. It indicates the InAs is a material with great potential for low-voltage high-speed III-V-based logic circuit applications. Overall, the InAs/$In_{0.7}Ga_{0.3}As$ HEMTs exhibit very well intrinsic speed, DC and RF performances owing to the appropriate epi-structure design, and short gate length.

IV. Conclusions

In this study, high performance 80 nm InAs/$In_{1-x}Ga_xAs$ composite-channel HEMTs with different indium content sub-channel has been fabricated and characterized. The high current gain cutoff frequency (f_T) of 360 GHz and maximum oscillation frequency (f_{max}) of 380 GHz were obtained at V_{DS} = 0.7 V with a calculated low gate delay time (0.84 psec at V_{CC} = 0.5 V) due to the high electron mobility in the InAs/$In_{0.7}Ga_{0.3}As$ channel. Overall, the device with $In_{0.7}Ga_{0.3}As$ sub-channel displays better characteristics than with $In_{0.53}Ga_{0.47}As$ sub-channel because of the carrier confinement improvement and superior transport property. Finally, the device exhibits the sate-of-the-art performance and the device technology demonstrated is suitable for high-frequency milimeter wave and high-speed logic applications.

Acknowledgment

The authors would like to acknowledge the assistance and support from the National Science Council and the Ministry of Economic Affairs, Taiwan, R.O.C., under the contracts NSC 96-2752-E-009-001-PAE and 95-EC-17-A-05-S1-020. Part of this work was supported by the "Nanotechnology Support Project" of the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan.

References

[1] D. H. Kim, J. A. Alamo, J. H. Lee, and K. S. Seo, "Performance Evaluation of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs for beyond-CMOS logic applications," in *IEDM Tech. Dig.*, 2005, pp.767-770.

[2] R. Chau, S. Datta, and A, Majumdar, "Opportunities and Chanllenges of III-V Nanoelectronics for future high-speed,low-power logic applications," in *Proc. IEEE CSIC Dig.*, pp. 17-20, 2005.

[3] C. I. Kuo, H. T. Hsu, and E. Y. Chang, "InAs-Channel Based Quantum Well Transistor," Electrochemical and Solid-state Lett., 11 (7) pp. H193-H196 2008.

[4] Y. Yamashita, A. Endoh, K. Shinohra, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, "Pseudomorphic $In_{0.52}Al_{0.48}As$/ $In_{0.7}Ga_{0.3}As$ HEMTs with an ultrahigh f_t of 562 GHz," *IEEE Electron Device Lett.*, vol. 23, pp. 573-575, Oct. 2002.

[5] K. Shinohra, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiyamizu, "547 GHz f_t $In_{0.7}Ga_{0.3}As$/ $In_{0.52}Al_{0.48}As$ HEMTs With Reduced Source and Drain Resistance," *IEEE Electron Device Lett.*, vol. 25, pp. 241-243, May 2004.

[6] S. J. Yeon, M. Park, J. Choi, and K. Seo, "610 GHz InAlAs/$In_{0.75}GaAs$ Metamorphic HEMTs with an ultra-short 15-nm-gate," in *IEDM Tech. Dig.*, pp.613-616 2007.

[7] T. Akazaki, K. Arai, T. Enoki, and Y. Ishii, "Improved InAlAs/InGaAs HEMT Characteristics by Inserting an InAs Layer into the InGaAs Channel," *IEEE Electron Device Lett.*, vol. 13, pp. 325-327, June. 1992.

[8] G. Meneghesso, D. Buttari, E. Perin, C. Canali, and E. Zanoni, "Improvement of DC, low frequency and reliability properties of InAlAs–InGaAs InP-based HEMTs by means of an InP etch stop layer," in *IEDM Tech. Dig*., Dec. 1998, pp. 227–230.

[9] T. Suemitsu, H. Yokoyama, T. Ishii, T. Enoki, G. Meneghesso, and E. Zanoni, "30-nm two-step recess gate InP-based InAlAs/InGaAs HEMTs," *IEEE Trans. Electron Devices*, vol. 49, no. 10, pp. 1694–1700, Oct. 2002.

[10] T. Suemitsu, H. Yokoyama, Y. Umeda, T. Enoki, and Y. Ishii, "High-performance 0.1-μm gate enhancement-mode InAlAs/InGaAs HEMTs using two-step recessed gate technology," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1074-1080, Jun. 1999.

[11] Y. Yamashita, A. Endoh, K. Shinohara, M. Higashiwaki, K. Hikosaka, T. Mimura, S. Hiyamizu, and T. Matsui "Ultra-short 25nm Gate Lattice Match InAlAs/InGaAs HEMTs Within the Range of 400GHz Cut Off Frequency," *IEEE Electron Device Lett.*, vol. 22, pp. 367-369 August 2001

[12] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp.1151-1159, 1988

[13] R. Chau, S. Datta, M. Docyz, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, "Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications", *IEEE Trans. Nanotechnology*, Vol. 4, No. 2, pp. 153–158, 2005.

[14] J. Guo, A. Javey, H. Dai, and M. Lundstrom, "Performance analysis and design optimization of near ballistic carbon nano tube field effect transistors," in *IEDM Tech. Dig.*, 2004, pp.703-706.

[15] T. Ashley, A. R. Barnes, L. Buckle, S. Datta, A. B. Dean, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, R. Jefferies, T. Martin, K. J. Nash, T. J. Philips, W. H. A. Tang, and R. Chau, "InSb-based quantum well transistors for high speed, low power applications," in Proc. CS-Mantech Conf., Apr. 2005.

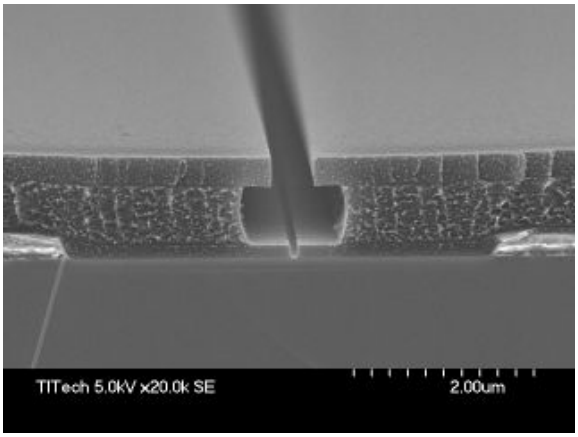

Fig. 1 Cross-sectional SEM image of the 80nm T-shaped gate resist profile.

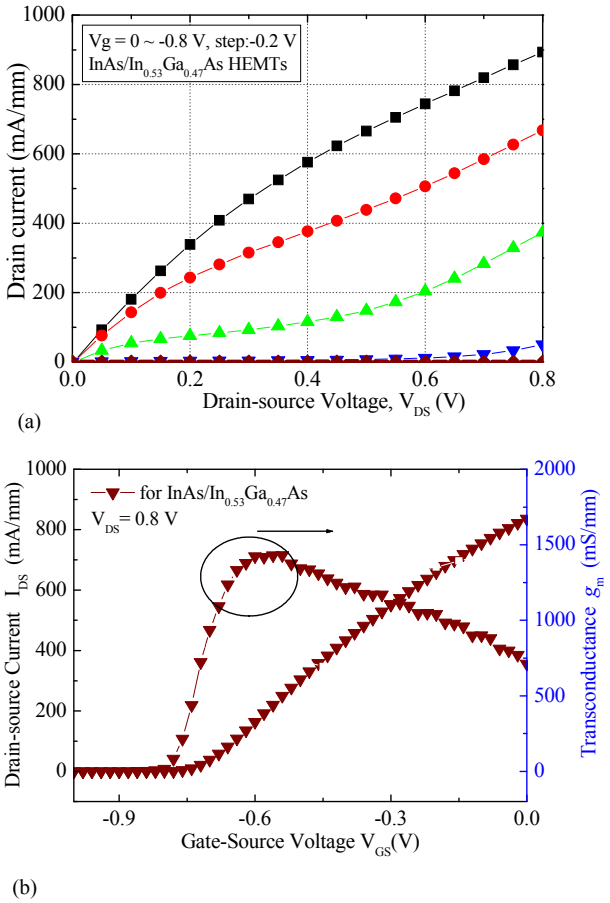

Fig. 2. Current-Voltage characteristics of the $InAs/In_{0.53}Ga_{0.47}As$ 0.08 × 100 μm^2 HEMTs. (a) Drain-source current versus drain-source voltage curves (b) Transconductance versus gate-source voltage curves.

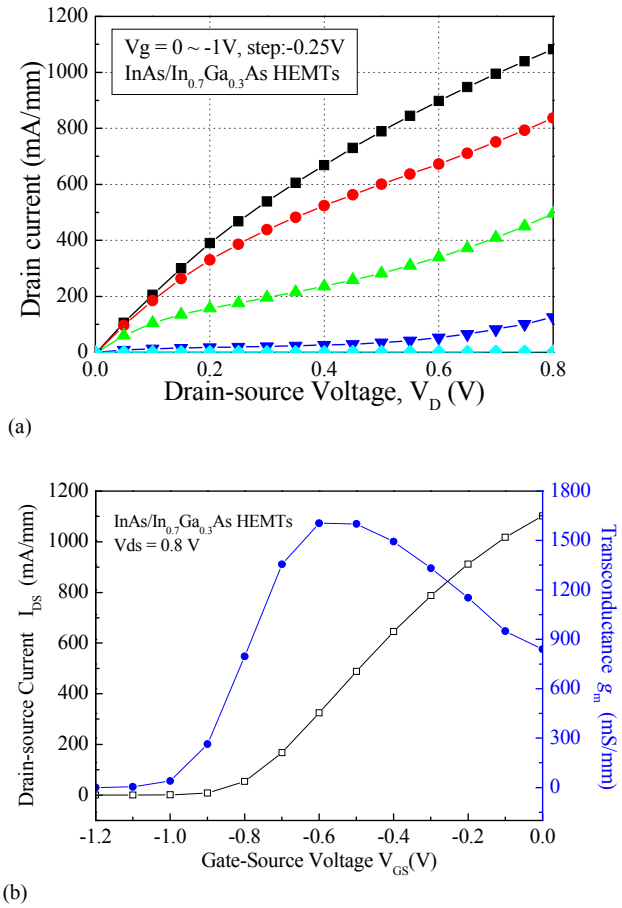

Fig. 3 Current-Voltage characteristics of $InAs/In_{0.7}Ga_{0.3}As$ 0.08 × 100 μm^2 HEMTs. (a) Drain-source current versus drain-source voltage curves (b) Transconductance versus gate-source voltage curves

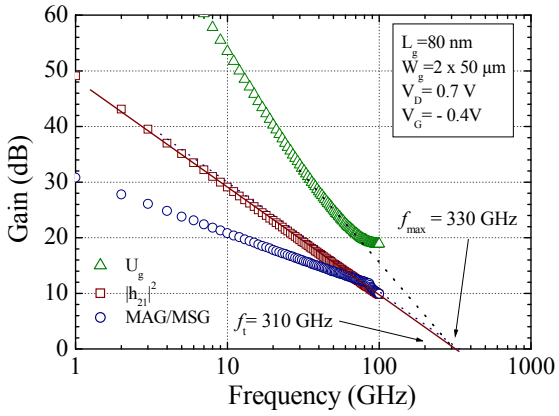

Fig. 4 Typical current gain $|h_{21}|$, MAG/MSG and U_g as a function of frequency of a 0.08 μm × 100 μm $InAs/In_{0.53}Ga_{0.47}As$ HEMT. The V_{DS} is 0.7 V, and the V_G is – 0.4 V.

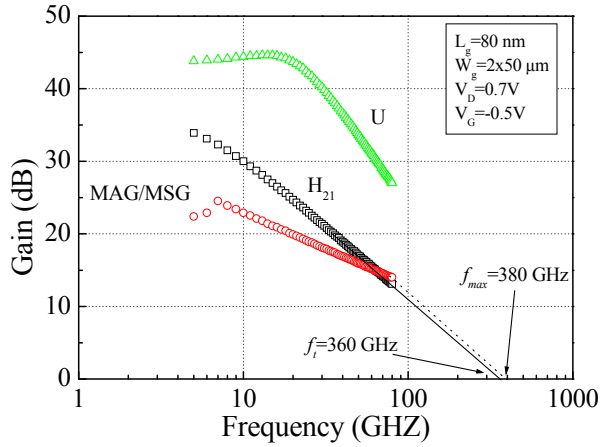

Fig. 5 Frequency dependence of the current gain H_{21}, the power gain MAG/MSG, and the unilateral gain U of the InAs/$In_{0.7}Ga_{0.3}As$ composite channel HEMTs. The frequency range was from 5 to 80 GHz, and the device was biased at V_{DS} = 0.7V and V_{gs} = -0.5V.

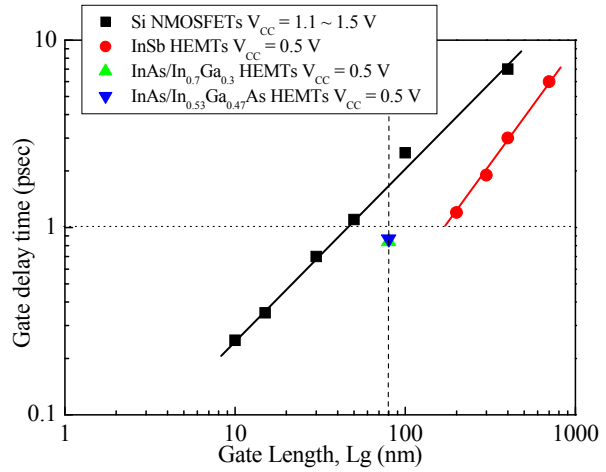

Fig. 6 Gate delay of InAs, InSb HEMTs and Si NMOSFETs as a function of gate length.