Impacts of NBTI/PBTI and Contact Resistance on Power-Gated SRAM With High-κ Metal-Gate Devices

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***Abstract*—The threshold voltage (V_{TH}) drifts induced by negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) weaken PFETs and high-k metal-gate NFETs, respectively. These long-term V_{TH} drifts degrade SRAM cell stability, margin, and performance, and may lead to functional failure over the life of usage. Meanwhile, the contact resistance of CMOS device increases sharply with technology scaling, especially in SRAM cells with minimum size and/or sub-ground rule devices. The contact resistance, together with NBTI/PBTI, cumulatively worsens the SRAM stability, and leads to severe SRAM performance degradation. Furthermore, most state-of-the-art SRAMs are designed with power-gating structures to reduce leakage currents in Standby or Sleep mode. The power switches could suffer NBTI or PBTI degradation and have large contact resistances. This paper presents a comprehensive analysis on the impacts of NBTI and PBTI on power-gated SRAM arrays with high-k metal-gate devices and the combined effects with the contact resistance on SRAM cell stability, margin, and performance. NBTI/PBTI tolerant sense amplifier structures are also discussed.**

***Index Terms*—Contact resistance, negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), power-gated SRAM, reliability.**

ACRONYM

SRAM	Static random access memory.
PBTI	Positive bias temperature instability.
NBTI	Negative bias temperature instability.
$\mathrm{R_{OV}}$	Overlap resistance.
$\mathrm{R_{EXT}}$	Extension resistance.
$\mathrm{R_{DP}}$	Deep resistance.
R_C	Silicon-contact diffusion resistance.

NOTATION

R_S	The sheet resistance per square of the underlying heavily doped silicon layer, in unit of $\Omega/\square$.
ρ_C	The specific contact resistivity between the metal and the diffusion layer in unit of ohm square centimeter.
l_t	The transfer length.
L_{silicide}	The length of a contacted silicide.

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I. INTRODUCTION

NBTI has long been a concern for scaled PFETs. The long-term V_{TH} drift caused by NBTI has been shown to degrade the stability and performance of SRAM, and may lead to functional failure over the life of usage. Recently, with the introduction of high-k metal-gate technology to contain the gate leakage current, and to enable scaling of MOSFET to 45 nm node and below, PBTI has emerged to be a major reliability concern for NFETs due to V_{TH} instability caused by charge trapping at the interface. These long term V_{TH} drifts degrade MOSFET current drive over time, and their effects become more significant with technology and voltage scaling (see Fig. 1) [1].

The transistor performance also degrades with the ever-increasing device contact resistances and series resistances of the channel/source/drain in scaled technologies. [2], [3]. Conventionally, the contact and series resistance are second-order effects on the device performance. However, with technology scaling, the contact area and the device width decrease, leading to increase in contact and series resistances. When the silicide length continuously shrinks and is smaller than the transfer length, the contact resistance increases sharply, severely degrading the stability and performance of circuits.

SRAMs in deep sub-100 nm technologies have poor margin and stability due to large leakage and process variation, fundamental limitation such as random dopant fluctuation (RDF), and microscopic effects such as line edge roughness (LER). The combined/cumulative effects of NBTI/PBTI and device contact and series resistance aggravate the already poor margin and stability of SRAMs. Furthermore, many state-of-the-arts SRAMs are designed with power-gating structures to reduce static power in Standby or Sleep mode [4]–[7]. The power-gating structures play vital roles to contain leakage current in Standby or Sleep mode, and to provide sufficient currents for SRAM arrays in Active mode. Unfortunately, power switches also suffer NBTI/PBTI stress and degradation, and become weaker over time. As such, it is crucial to understand the NBTI/PBTI degradation of the power-gating structures, in addition to the cell, and the resulting combined impacts on the power-gated SRAMs.

Previous works have shown that SRAM read static margin (RSNM) was degraded by NBTI effects, while write margin (WM) was improved [8]. RSNM and WM were both degraded

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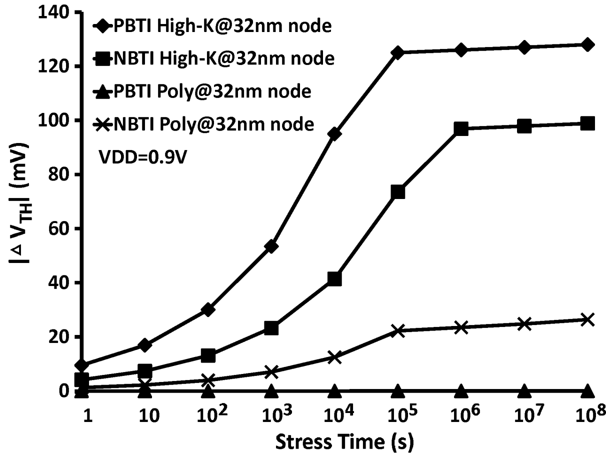


Fig. 1. V_{TH} drifts induced by NBTI and PBTI using reaction-diffusion framework calibrated with published data [1]. T_{INV} for high-k metal gate (nMOS = 7.5 Å; pMOS = 7.7 Å), T_{INV} for poly gate (nMOS = 16.5 Å; pMOS = 17.5 Å).

when PBTI and NBTI were considered together, and the degradations were more sensitive to PBTI [9]. SRAM V_{CCMIN} was also shown to degrade with time [10]. However, these papers only focused on analyzing SRAM cells in standard 6-T SRAM array structures. In this paper, we present a comprehensive analysis on the impacts of NBTI and PBTI on power-gated SRAM arrays. Two different types of power-gating structures, header and footer, are analyzed. The resulting impacts on the stability, margin, power, performance, virtual supply bounce, and wake-up time, etc., are discussed. The effects of contact and series resistances on the SRAM cell, and the combined impacts with NBTI/PBTI on SRAM are also investigated.

In the following section, we first describe the details of our simulation model in predictive technology model (PTM) high-k CMOS 32 nm technology in Section II. Section III shows NBTI/PBTI impacts on power-gated SRAM. The impacts of contact resistance on power-gated SRAM are analyzed in Section IV, and their combined effects with NBTI/PBTI are also studied. Section V compares SRAM sensing structures, including differential sensing amplifier and large signal sensing scheme, and shows that judicious choice of appropriate sense amplifier structure can mitigate NBTI and PBTI effects. The conclusions of the paper are given in Section VI.

II. Analysis Models

This section describes the NBTI/PBTI model and contact resistance model used in our analyses. The power-gated SRAM structure and its operation in this work are also introduced.

A. NBTI and PBTI Model

NBTI causes the threshold voltage (V_{TH}) of PFET to become more negative with time, leading to long term degradation of current drive. Under negative gate bias (stress phase), holes in inversion layer interact with and break Si-H bonds at interface. The H-species diffuse into the oxide, leaving interface traps at interface, thus causing increase in $|V_{TP}|$. When stress conditions are removed, H-species diffuses back to interface and passivates dangling Si-bonds, and passivation (or "recovery") occurs. Thus, the device lifetime under ac stress is longer than that predicted by dc stress measurements. The corresponding effect for NFET, namely PBTI, is in general quite small and can be neglected for oxide/poly-gate device. NFETs with high-κ gate, however, exhibit significant charge trapping and thus long-term V_{TH} shift as well. The V_{TH} drift of PFET (NFET) due to NBTI (PBTI) can be described by dc reaction-diffusion (RD) framework when the stress signal does not change (i.e., static stress) [8], [11], [12]. If the stress signal changes with time (i.e., alternating stress), the dc RD model can be multiplied by a prefactor to account for the signal (stress) probability, frequency, duty cycle of the stress signal, and the recovery mechanism, and the new formula is called ac RD model [8], [11], [12]. However, according to the results of [12] and [13], the impact of the signal frequency on V_{TH} drift is relatively insignificant. Thus, we neglect the effect of signal frequency, and analyze cases with various signal (stress) probabilities. In following analysis, the prefactor of the ac RD model is simplified as function of signal probability. The simplified ac RD model is

$$\Delta V_{TH}(t) \cong K_{AC} \times t^n \cong \alpha(S) \times K_{DC} \times t^n \quad (1)$$

where prefactor α is a function of signal probability (S), and K_{DC} is a technology—dependent constant. Notice also that NBTI/PBTI induced V_{TH} drift depends strongly on the V_{GS} bias and temperature, but barely on V_{DS} [11], [12]. Fig. 1 shows the V_{TH} drifts induced by NBTI and PBTI using reaction-diffusion framework and calibrated with published data [1]. The V_{TH} drifts are incorporated into PTM 32 nm and PTM high-k 32 nm device models.[1] Notice that in the model, T_{INV} of poly-gate PFET is 17.5 Å, while T_{INV} of high-k metal-gate PFET is only 7.7 Å. T_{INV} of high-k metal-gate device is almost 2.3 times smaller than T_{INV} of poly-gate device. These are consistent with the facts that the best (smallest) T_{INV} that can be achieved with SiON/poly-Si gate is around 17–18 Å, limited by gate tunneling leakage, and that state-of-the-art 32 nm high-k metal-gate devices have T_{INV} around 7.5–8.0 Å. As such, in our model, the V_{TH} drift of high-k gate-device is more serious than the SiON/poly-Si gate device.

B. Contact Resistance Model

As shown in Fig. 2(a), the source/drain (S/D) series resistance can be divided into overlap resistance (R_{OV}), extension resistance (R_{EXT}), deep resistance (R_{DP}), and silicon-contact diffusion resistance (R_C), where all resistance are in units of $\Omega/\square$. Conventionally, R_{OV}, R_{EXT}, and R_{DP} are included in the device model, but R_C is not. We model the R_C of a transistor as shown in Fig. 2(b). With technology scaling, the sum of R_{OV}, R_{EXT}, and R_{DP} decreases, but R_C increases. The formula for silicon-contact diffusion resistance is given by

$$R_C = \sqrt{R_S \rho_C} \coth\left(\frac{L_{\text{silicide}}}{l_t}\right) \quad (2)$$

where R_S is the sheet resistance per square of the underlying heavily doped silicon layer, in unit of $\Omega/\square$, ρ_C is the specific contact resistivity between the metal and the diffusion layer in unit of ohm square centimeter, and l_t is the transfer length,

[1][Online]. Available: http://www.eas.asu.edu/~ptm/

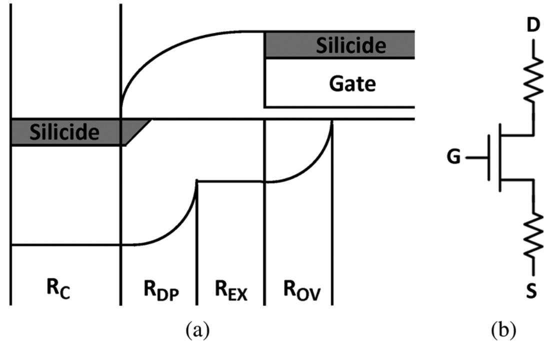


Fig. 2. (a) Series resistance components of S/D and (b) schematic of NMOS with S/D diffusion contact resistances.

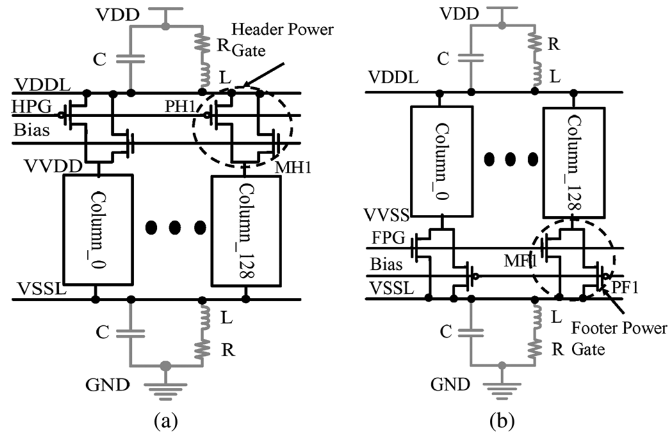


Fig. 3. Power-gated SRAM with (a) header and (b) footer.

which is defined as $l_t = (\rho_C/R_S)^{1/2}$ [3]. When L_{silicide} is larger than l_t, the contact resistance is only slightly dependent on the contact region. However, when L_{silicide} is smaller than l_t, the contact resistance increases sharply if L_{silicide} is further scaled down. According to [3], the contact resistance would be larger than the sum of R_{OV}, R_{EXT}, and R_{DP}, and increases sharply beyond 45 nm technology node. As diffusion contact resistance dominates the short channel device resistance, we focuses on its impacts on SRAM array in the following analysis.

C. Power-Gated SRAM Structures

SRAM power-gating structures can be divided into two basic types: a header power-gating structure and a footer structure. Fig. 3(a) shows a column-based header-gated SRAM structure. In this structure, PH1 is the header power switch used for leakage reduction, and MH1 is the clamping device to bias virtual supply (VVDD) for data retention in Standby or Sleep mode. Fig. 3(b) shows a column-based footer-gated SRAM structure. MF1 is the footer power switch, and PF1 is the clamping device to bias virtual ground (VVSS) for data retention in Standby or Sleep mode. Fig. 4 shows the standard 6T SRAM cells used in our analysis. The sub-array block size is 128 × 128 cells. Parasitic capacitance, inductance, and resistance of the package are included in our analysis. Each power-gated SRAM array is packed by a package model [14], and parasitic capacitance, inductance and resistance of the package model are 5.32 pF, 8.18 nH, and 0.217 Ω, respectively.

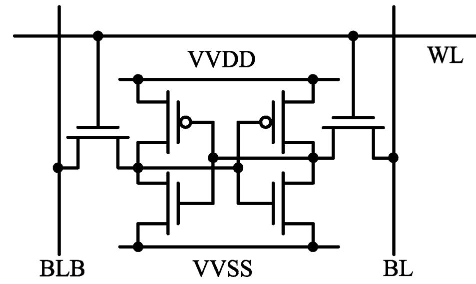


Fig. 4. 6-T SRAM cell.

TABLE I
SIGNAL (STRESS) PROBABILITY CASE SUMMARY

Case	Cell Signal Probability for Array Analysis	Case	*Individual Cell Signal Probability*
A	none	D	none
B	25% (75%)	E	25% (75%)
C	50% (50%)	F	50% (50%)
		G	75% (25%)

In power-gated SRAM arrays, the power switch should provide sufficient supply voltage and current for SRAM cells to maintain adequate margin and performance during Read and Write operations. As the power switch is constantly under NBTI or PBTI stress (V_{GS} stress) in Active mode, they have the highest probability of being stressed. Hence, we assume the worst case scenario that the power switch is always stressed. In contrast, the clamping device (diode) is shunted and shorted by the power switch and experiences no NBTI/PBTI stressing during Active mode. In Standby or Sleep Mode, the stressing voltage (V_{GS}) of the clamping device is about one V_{TH} (MOS diode voltage), thus the NBTI or PBTI effects on the clamping device is negligible.

The following sections present detail simulation results based on BSIM predictive high-k metal-gate model for 32 nm. The supply voltage of the SRAM arrays is 0.9 V. The contact area is assumed as $0.05 \times 0.05\ \mu\mathrm{m}^2$ based on scaling from UMC 65 nm CMOS process technology in accordance with scaling factor from ITRS Roadmap.[2] The ranges of values for sheet resistance and specific contact resistivity are based on scaling/extrapolation from UMC 65 nm CMOS process, published data, as well as ITRS projection [3].[2] The contact resistance at 32 nm node ranges from around 100 to 500 Ω.

Besides, The V_{TH} drift due to NBTI and PBTI are based on ac RD framework and calibrated with published data [1]. The prefactors of ac RD framework for different cases are from [8]. When the entire array under NBTI/PBTI stress is analyzed, all cells of the array are assumed to be stressed with three different signal probability cases (Cases A, B, and C in Table I): none, 25% (75%) and 50% (50%). On the other hand, when an individual cell is examined, four different signal probability (SP) cases (Cases D, E, F, and G in Table I) are considered: none, 25% (75%), 50% (50%), and 100% (0%).

[2][Online]. Available: http://www.itrs.net/

III. Impacts of NBTI and PBTI on Power-Gated SRAM

This section analyzes the impacts of NBTI and PBTI on power-gated SRAM. Long-term reliability degradations of header and footer structures are investigated, including RSNM, WM, and access performance. NBTI and PBTI effects on power-gated SRAM wake-up transition are also analyzed.

A. Active Mode Virtual Supply

When a header-gated SRAM is stressed, the VVDD drifts with time, and the stability of the array is impacted. VVDD is determined by the resistance of the power switch and the equivalent resistance of the SRAM array. Hence, the drift of VVDD is also affected by signal probabilities of SRAM cells. When only NBTI is present/considered, VVDD decreases with the stress time [see Fig. 5(a)] as V_{TH} and resistance of the PFET header increase due to NBTI, and the effect is more significant than the increase in the equivalent resistance of the SRAM array. On the other hand, if only PBTI is present/considered, VVDD increase [see Fig. 5(b)] with the stress time since there is no PBTI effect on the PFET header switch while the equivalent resistance of the SRAM array increases due to PBTI on cell NFETs. Similar behavior can be observed for a footer-gated SRAM. When only NBTI is present/considered, VVSS decreases [see Fig. 5(d)] since there is no NBTI effect on the NFET footer switch, while the equivalent resistance of the SRAM array increases due to NBTI on cell PFETs. In contrast, if only PBTI is present/considered, VVSS increases with time [see Fig. 5(e)]. This is because the equivalent resistance of the NFET footer increases due to PBTI, and the effect is more significant than the increase in the equivalent resistance of the SRAM array. Finally, when both NBTI and PBTI are present/considered, VVDD variation of a header-gated SRAM shows the combined effect of NBTI-only and PBTI-only cases [see Fig. 5(c)]. Similar observation for VVSS variation of a footer-gated SRAM when both NBTI and PBTI are present/considered can be seen in [see Fig. 5(f)]. These results imply that virtual supply drift due to the V_{TH} drift of header/footer power switch is only partially compensated by the V_{TH} drift of the SRAM cell array.

B. Read Operation

RSNM of a cell is defined as the voltage difference between the maximum SRAM Read disturb and the minimum trip point of the SRAM inverter pair during Read operation. Therefore, when PFET loading transistors are degraded by NBTI, trip points of the SRAM inverter pair reduce and RSNM becomes worse. Degradation of header (footer) power switch by NBTI (PBTI) increases the V_{TH} and "ON" resistance of the power switch, thus reducing the voltage across the array during Active mode to degrade the RSNM of a cell [see Fig. 6(a) and (d)]. On the other hand, the impact of PBTI degradation of the cell driving (pull-down) NFETs depends on the signal (stress) probability. When both NFET driving transistors are stressed and suffer PBTI induced V_{TH} drift, the RSNM tends to improve [see Fig. 6(b) and (e)]. The reason is as follows. Due to PBTI, both Read disturb and trip points of SRAM inverter pair increase. However, Read disturb is determined by the voltage divider formed by the NFET access transistor and the NFET driving transistor during Read operation. As the NFET driving transistor in the voltage divider is fully on, the PBTI effect of the Read disturb increase is smaller than the increase of inverter trip voltage where the NFET driving transistor is off. Thus, RSNM improves when V_{TH} of both NFET driving transistors increase. In contrast, if the signal (stress) probability is skewed [e.g. 100% (0%)], the Read disturb would dominates RSNM for the worst-case pattern, and RSNM decreases with the stress time [see Fig. 6(b) and (e)]. Furthermore, when both NBTI and PBTI are considered and the signal (stress) probability is not 100% or 0% (so both NFET driving transistors are stressed), the RSNM degradation induced by NBTI can be offset by RSNM improvement induced by PBTI of the driving NFETs [see Fig. 6(c) and (f)]. Fig. 7(a) and (b) show the relation between RSNM and signal (stress) probability when the stress time is 10^6 s. 10^6 s is chosen as the V_{TH} drifts induced by NBTI and PBTI saturate when the stress time is around 10^5 to 10^6 s [1]. The V_{TH} drift induced by PBTI saturates earlier than that induced by NBTI. These figures clearly indicate that while NBTI degrades RSNM in general, PBTI can improve RSNM when signal (stress) probability is between around 25% and 75%. RSNM under PBTI reaches the peak value when cell signal (stress) probability is around 50%. Both figures also indicate that the RSNM degradation induced by NBTI can be offset by RSNM improvement induced by PBTI when the cell signal (stress) probability is between around 25% and 75%. As such, SRAM cell array lifetime would be extended if the cell signal (stress) probability could be maintained around 50%.

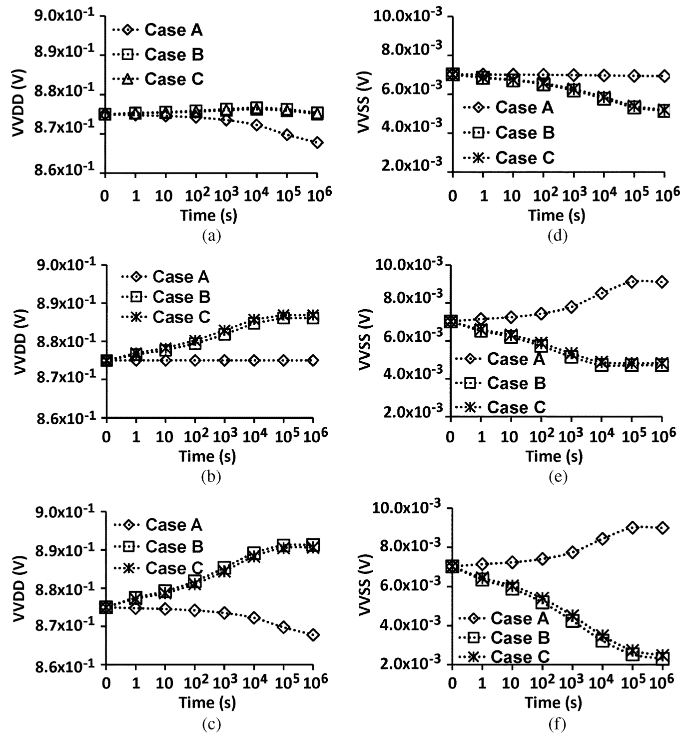


Fig. 5. Active mode VVDD of header structure impacted by (a) NBTI, (b) PBTI, and (c) NBTI&PBTI; active mode VVSS of footer structure impacted by (d) NBTI, (e) PBTI, and (f) NBTI&PBTI.

The Read delay is determined by the bitline discharging time by the access NFET and the driving NFET of the selected cell. Therefore, Read delays are relatively insensitive to the

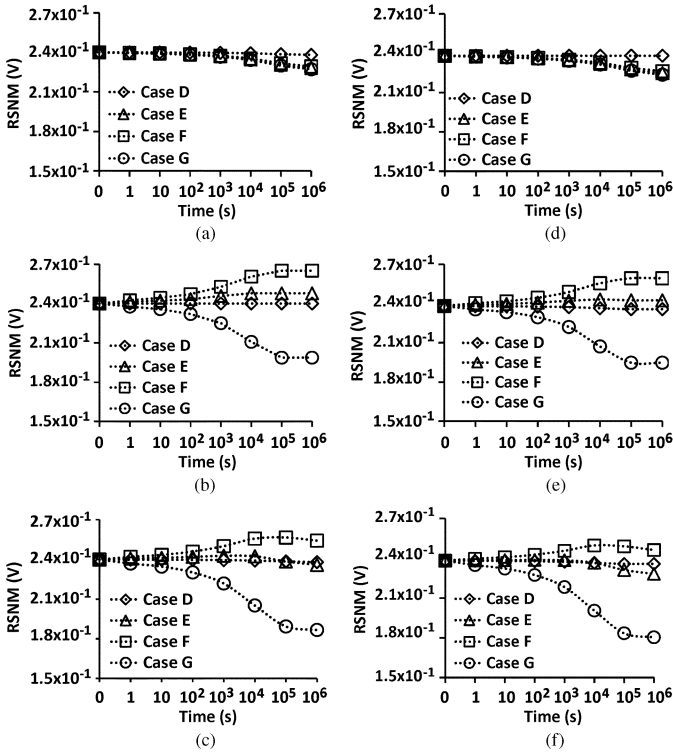


Fig. 6. RSNM of header structure impacted by (a) NBTI, (b) PBTI, and (c) NBTI&PBTI; RSNM of footer structure impacted by (d) NBTI, (e) PBTI, and (f) NBTI&PBTI.

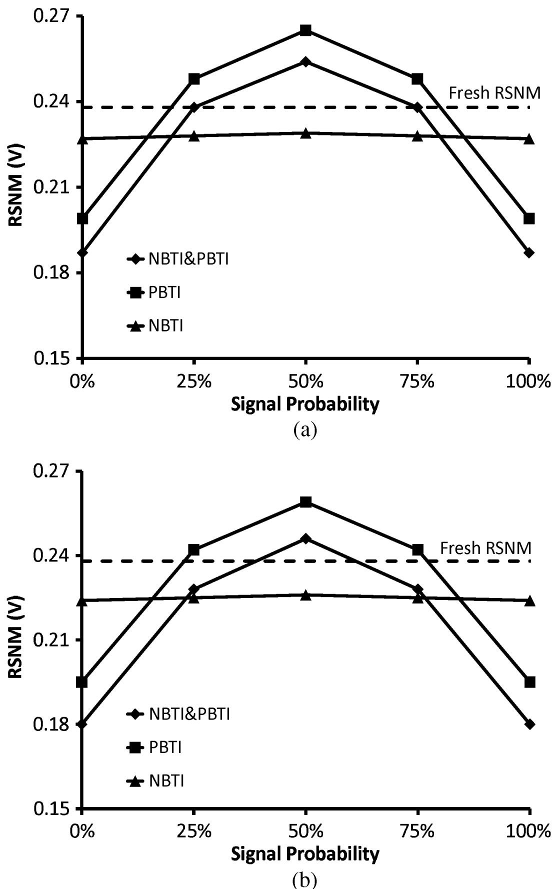


Fig. 7. Relation between RSNM and signal (stress) probability when stress time is 10^6 s in (a) header and (b) footer structure.

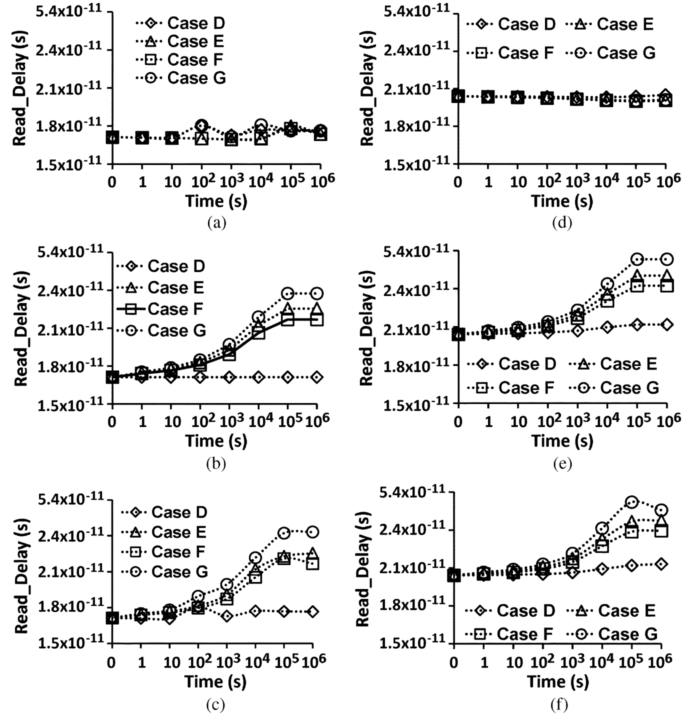


Fig. 8. Read delay of header structure impacted by (a) NBTI, (b) PBTI, and (c) NBTI&PBTI; read delay of footer structure impacted by (d) NBTI, (e) PBTI, and (f) NBTI&PBTI.

V_{TH} drifts of the PFET loading transistors due to NBTI [see Fig. 8(a) and (d)]. In contrast, Read delay becomes worse when PBTI is present/considered [see Fig. 8(b) and (e)] as the driving NFET is weakened. Moreover, after NBTI/PBTI stressing, the current flowing through the power switch and SRAM array decrease, and the Read power of both header/footer-gated SRAM decrease with the stress time.

C. Write Operation

WRITE occurs by first discharging the "logic 1" storage node through the access NFET, and then charging the "logic 0" storage node towards "1" through the pull-up PFET once the original "logic 1" storage node is pulled down below the trip voltage of the inverter. The cross-coupled feedback inverter action then kicks in to complete the Write operation. When a cell is affected by NBTI and the cell signal (stress) probability is not 100% (0%), both PFET loading transistors become weaker. A weaker holding PFET helps the initial discharging of the "logic 1" storage node through the access NFET, while a weaker pull-up PFET impedes the subsequent pull-up of the "logic 0" storage node. Since the initial discharging of the "logic 1" storage node tends to be the dominating factor for Write operation, the WM improves with both PFET weakened. However, when the cell signal (stress) probability is 100% (0%), only one PFET loading transistor becomes weaker. For the worst case pattern, the PFET holding the original "logic 1" storage node is not stressed/weakened, so the pull down of the "logic 1" storage node is not getting easier. The PFET corresponding to the original "logic 0" storage node, however, would be fully stressed/weakened, and thus slowing down the charging of its storage node to "logic 1" during Write operation.

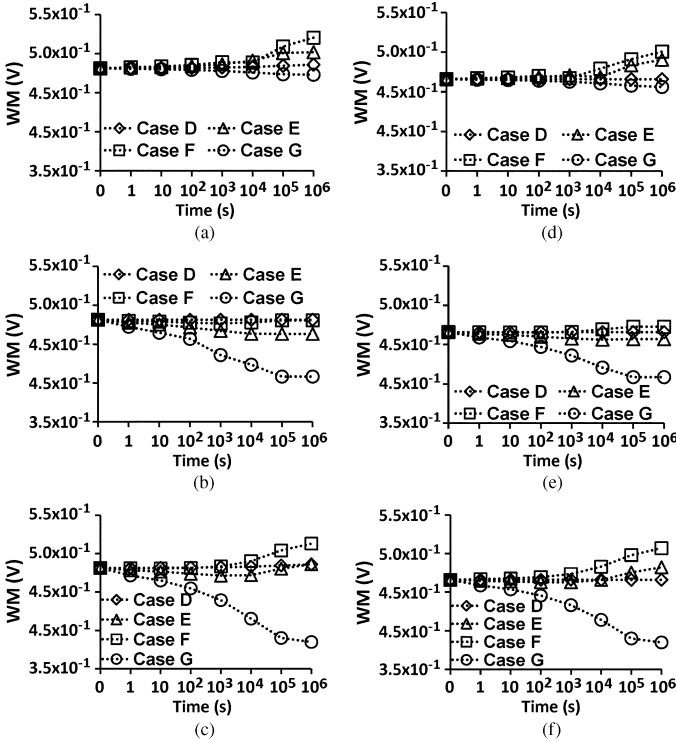


Fig. 9. WM of header structure impacted by (a) NBTI, (b) PBTI, and (c) NBTI&PBTI; WM of footer structure impacted by (d) NBTI, (e) PBTI, and (f) NBTI&PBTI.

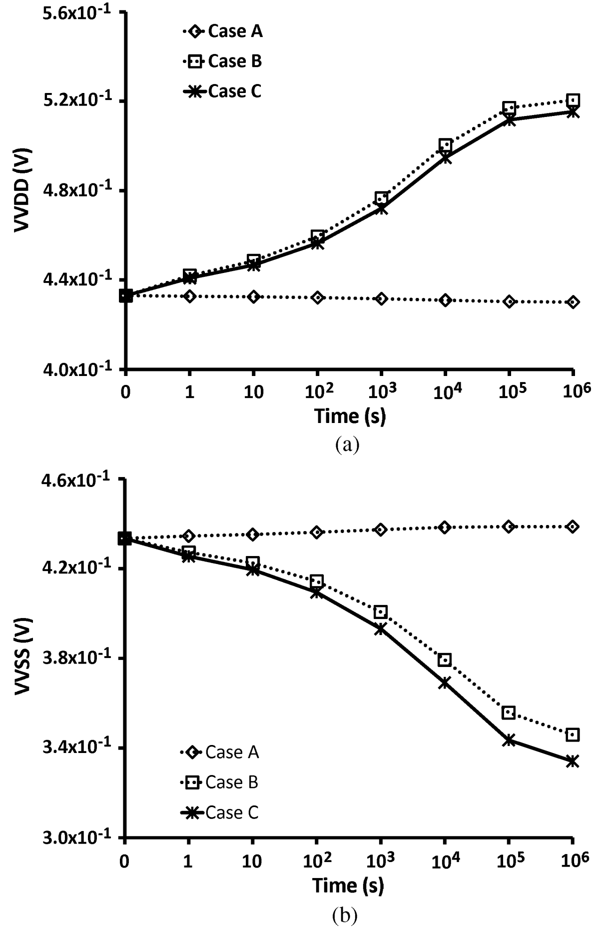


Fig. 10. (a) Change in VVDD of header structure by NBTI&PBTI and (b) change in VVSS of footer structure by NBTI&PBTI during standby/sleep mode.

As a result, the WM degrades [see Fig. 9(a) and (d)]. On the other hand, when a cell is affected by PBTI and cell signal (stress) probability is not 0% or 100%, both NFET driving transistors degrade. Nevertheless, during a Write operation, the pull-down of the "logic 1" storage node is dictated initially by the strength of the access NFET and the loading PFET, and then by the cross-coupled feedback inverter action. Weakening both driving NFETs helps the pull-up of the "logic 0" storage node, while impedes the pull-down of the "logic 1" storage node through the cross-coupled feedback inverter action, and the two effects compensate each other. Thus, the WM is relatively insensitive to PBTI. However, if the cell signal (stress) probability is 0% or 100%, only one NFET driving transistor's V_{TH} increases, leading to higher trip point of one of the inverter. For the worst-case pattern, the higher trip point of the inverter would impede the final pull-down of its "logic 1" storage node through the cross-coupled feedback inverter action, thus degrading the WM [see Fig. 9(b) and 9(e)]. Finally, the combined impact of NBTI and PBTI on the WM are shown in Fig. 9(c) and (f).

The Write delay of a cell has a positive correlation with its WM. Thus, the Write delay decreases when WM improves, and the Write delay becomes worse when WM degrades. The Write power also decreases with stress time due to the lower current flowing through the power-gated SRAM after stressing.

D. Standby/Sleep Mode Virtual Supply and Wake-Up Transition

During Standby or Sleep mode, the power switch turns off while the clamping device biases VVDD (for header-gating) or VVSS (for footer-gating) to appropriate level for data retention. Because the clamping device is not stressed as explained in Section II, VVDD (VVSS) is dominated by V_{TH} drifts of the SRAM array devices during Standby or Sleep mode. As such, the Standby/Sleep mode VVDD of the header structure increases with the stress time, while the Standby/Sleep mode VVSS of the footer structure decreases with the stress time as shown in Fig. 10. Additionally, due to the increased equivalent "OFF" resistances of the SRAM array, the leakages of both header and footer structures decrease as shown in Fig. 11.

During wake-up transition, the power switch turns on, leading to virtual supply line bounce due to large current flowing through the parasitical capacitance, inductance, and resistance of the package and interconnect. After stressing, the V_{TH} and equivalent resistance of the power switch and SRAM array increase, so the wake-up current of the SRAM array decreases. As a result, the virtual supply line bounce reduces during wake-up transition as shown in Fig. 12. Moreover, when only the power switch is impacted by NBTI or PBTI, the wake-up time increases with stress time due to higher V_{TH} of the power switch (Case A of Fig. 13(a), and Case A of Fig. 13(b)). However, if the SRAM cell array also suffers NBTI and/or PBTI stress, the wake-up time decreases, as the Standby/Sleep mode VVDD of the header structure increases

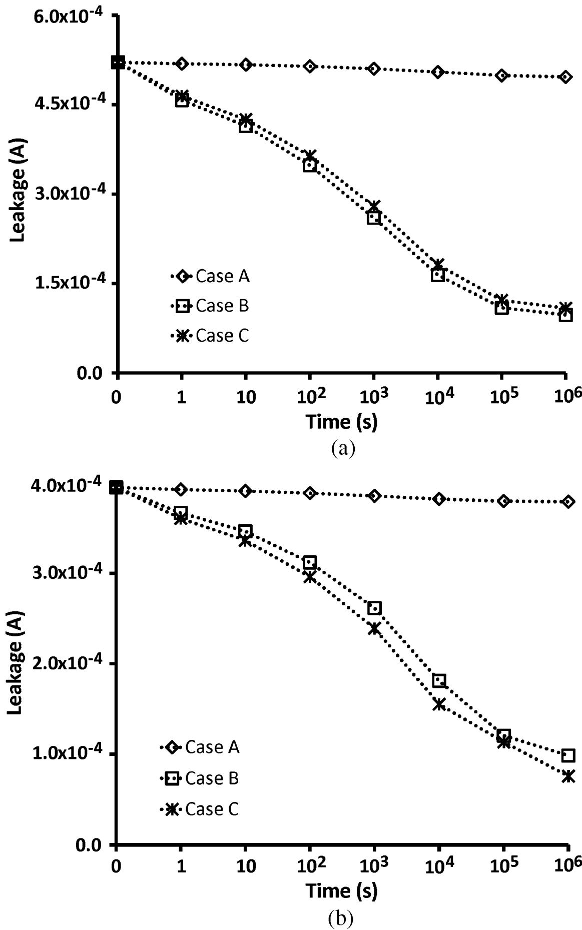


Fig. 11. (a) Leakage of header structure impacted by NBTI&PBTI and (b) leakage of footer structure impacted by NBTI&PBTI during standby/sleep mode.

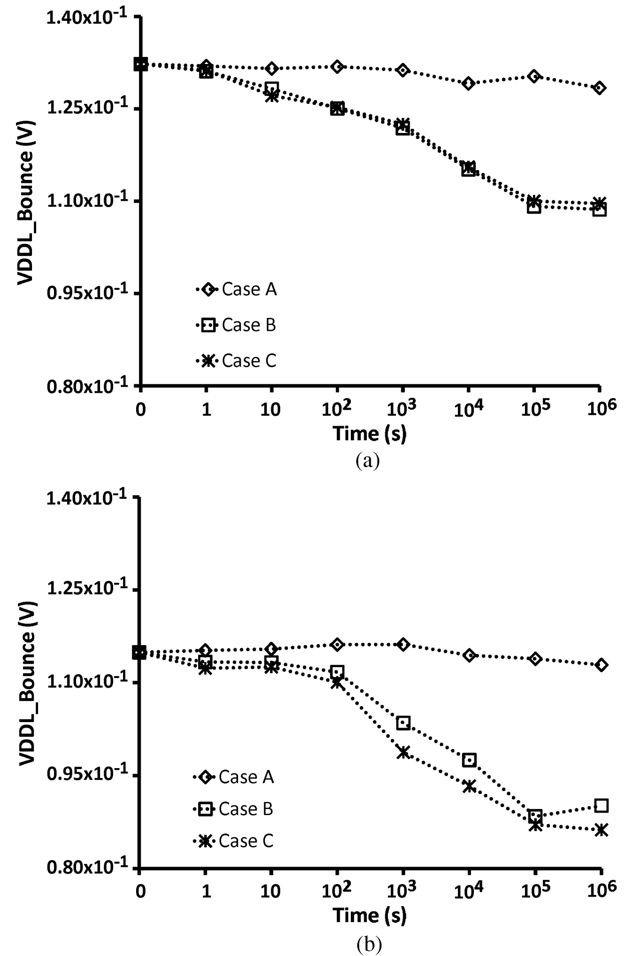


Fig. 12. (a) VVDD bounce of header structure impacted by NBTI&PBTI and (b) VVSS bounce of footer structure impacted by NBTI&PBTI during wake-up transition.

and the Standby/Sleep mode VVSS of the footer structure decreases with the stress time.

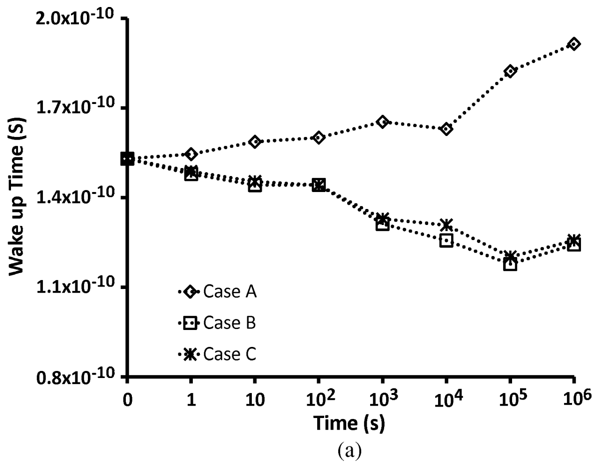
$V_{\rm TH}$ drifts of pMOS and nMOS strongly depend on $V_{\rm GS}$. If $V_{\rm GS}$ increases, $V_{\rm TH}$ drift rises. If $V_{\rm GS}$ decreases, $V_{\rm TH}$ drift induced by NBTI/PBTI also decreases. For power-gated SRAM during Standby/Sleep mode, the voltage across cell array decreases, and the $V_{\rm TH}$ drift during Standby/Sleep mode becomes smaller compared with the drift during Active mode. If the data is not needed, the SRAM can be shut down completely to allow/facilitate the NBTI/PBTI recovery mechanism. Therefore, the lifetime of SRAM can be extended by properly controlling power-gated SRAM into Standby/Sleep mode or aggressively shutting down unused sections.

IV. Combined Impacts of Contact Resistance and NBTI/PBTI

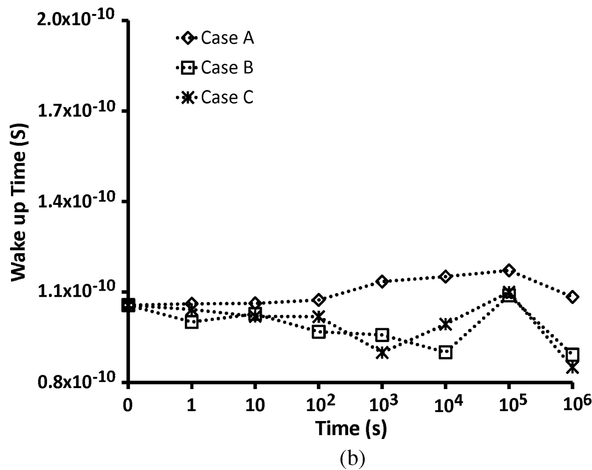
This section investigates the SRAM reliability impact by contact resistance. The combined impacts of contact resistance and NBTI/PBTI on Power-gated SRAM are also analyzed. Based on the MOS model of Fig. 2(a), an SRAM cell with contact resistances is built up as shown in Fig. 14. We assume the cell in Fig. 14 stores “logic 1” $(Q=1)$. The RSNM of the cell is defined as the voltage difference between the trip voltage of $\rm INV_1$ and Read disturb voltage induced by M4 and M6 during Read cycles. WM of the cell is defined as the BL voltage level below which the cell will flip during Write cycles. Reference [3] proposed selective device structure scaling and parasitic engineering as a way to improve transistor performance and extend the technology roadmap. The contact resistance was shown to play an important role, and various contact resistance values were assumed/used. In our analysis, the contact area is assumed as $0.05\times 0.05\ \mu{\rm m}^2$ based on scaling from UMC 65 nm CMOS process technology in accordance with the scaling factor from ITRS Road-map.[2] The ranges of values for sheet resistance and specific contact resistivity are based on scaling/extrapolation from UMC 65 nm CMOS process, published data, as well as ITRS projection [3].[2] The contact resistance at 32 nm node ranges from around 100 to 500 Ω.

A. Read Operation

Referring to Fig. 14, when the diffusion contact resistances, R1, R5, R7, and R9, increase, the trip voltage of INV_1 decreases and RSNM degrades. If the diffusion contact resistance, R3, increases, the trip voltage of INV1 increases and RSNM improves. On the other hand, M4 and M6 form a voltage divider and induce Read disturb during Read cycle. The Read disturb voltage increases with larger R4 but decreases with larger R2.



(a)



(b)

Fig. 13. (a) Wake-up time of header structure impacted by NBTI&PBTI and (b) wake-up time of footer structure impacted by NBTI&PBTI.

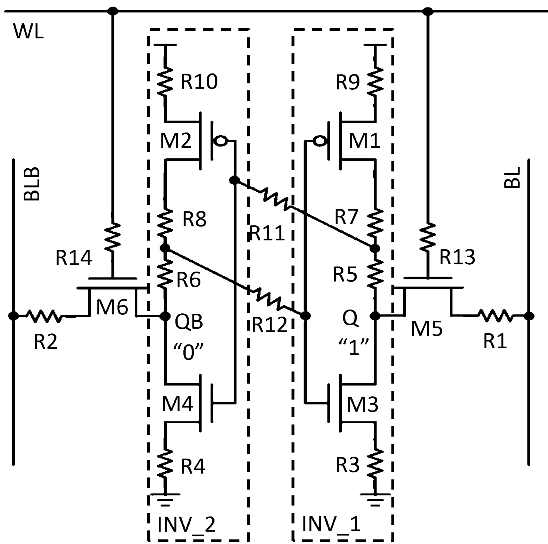


Fig. 14. (a) Wake-up time of header structure impacted by NBTI&PBTI and (b) wake-up time of footer structure impacted by NBTI&PBTI.

All gate-poly contact resistances affect neither the trip voltage because they are in series with the "infinite" gate resistance, nor the RSNM as they are not on the Read current paths.

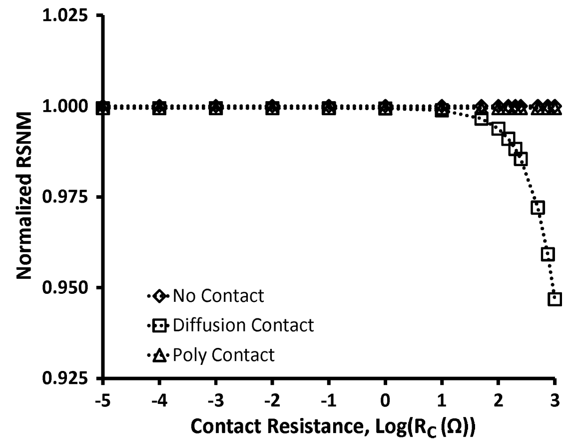


Fig. 15. Normalized RSNM versus contact resistance. RSNM is normalized with respect to the case with no contact resistance. RSNM degradation at 32 nm node from diffusion contact resistance is around 1% to 3%.

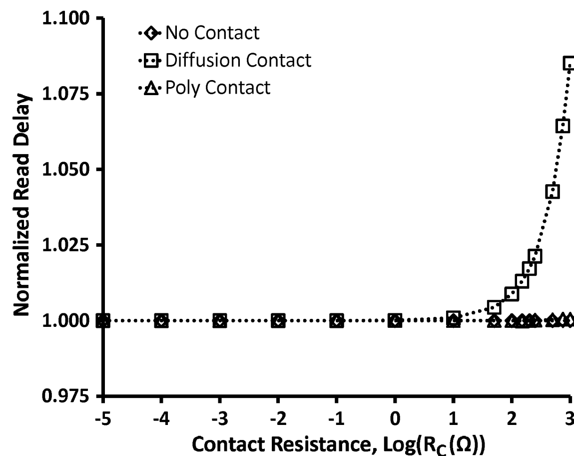


Fig. 16. Normalized read delay versus contact resistance. Read delay is normalized with respect to the case with no contact resistance. Read delay degradation at 32 nm node from diffusion contact resistance is around 1% to 4.5%.

RSNM decreases with increasing contact resistance as shown in Fig. 15. When the contact resistance approaches 1 kΩ, RSNM would degrade 6%. The reason is that R5, R7, and R9 form a series resistance chain, causing the trip voltage to decrease. Although R3 increases the trip voltage, its effect is smaller than the R5/R7/R9 resistance chain. Notice that R2 compensates the Read disturb increase caused by R4, thus the Read disturb voltage remains almost unchanged. Fig. 15 also shows the RSNM is not impacted by the increase in gate-poly contact resistance as discussed in the previous section.

Notice that when the diffusion contact resistance increases, Read delay becomes longer as shown in Fig. 16. This is due to increased R2 and R4 on the Read current (bit-line discharge) path. As a result, the discharge time of BLB increases with increasing diffusion contact resistance. Moreover, Read delay is insensitive to the gate-poly contact resistances because they are not on the Read current path of a SRAM cell.

When NBTI and PBTI are considered, in the worst case, $V_{\rm TH}$ of M1 and M4 increase while $V_{\rm TH}$ of M2 and M3 remain unchanged. Because access transistors, M5 and M6, are stressed

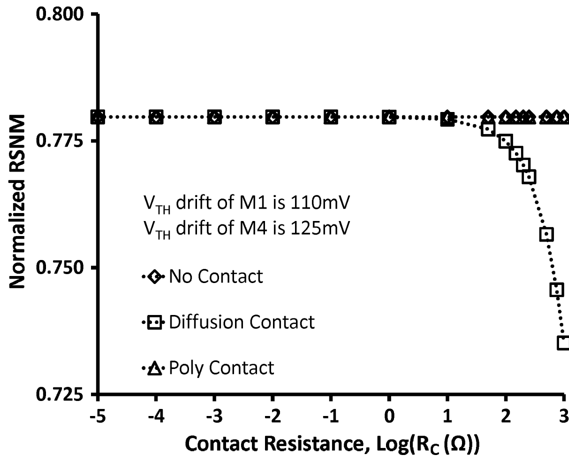


Fig. 17. Normalized RSNM under NBTI and PBTI versus contact resistance. RSNM is normalized with respect to the case with no contact resistance and no NBTI/PBTI stress. RSNM degradation at 32 nm node caused by the combined effects of NBTI/PBTI and diffusion contact resistance is around 23% to 26%.

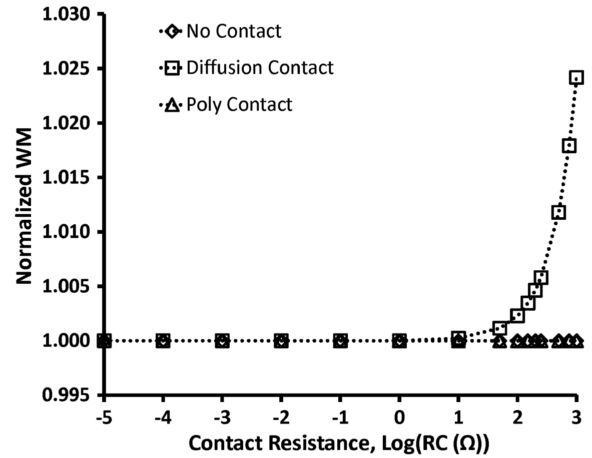


Fig. 19. Normalized WM versus contact resistance. WM is normalized with respect to the case with no contact resistance. WM improvement at 32 nm node caused by diffusion contact resistance is around 0.3% to 1.2%.

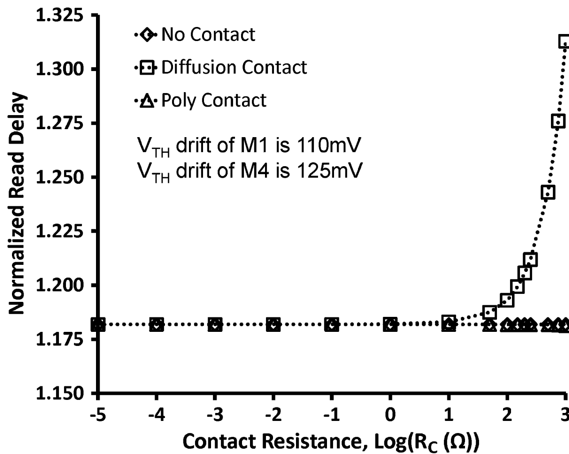


Fig. 18. Normalized read delay under NBTI and PBTI versus contact resistance. Read delay is normalized with respect to the case with no contact resistance and no NBTI/PBTI stress. Read delay degradation at 32 nm node caused by the combined effects of NBTI/PBTI and diffusion contact resistance is around 20% to 24%.

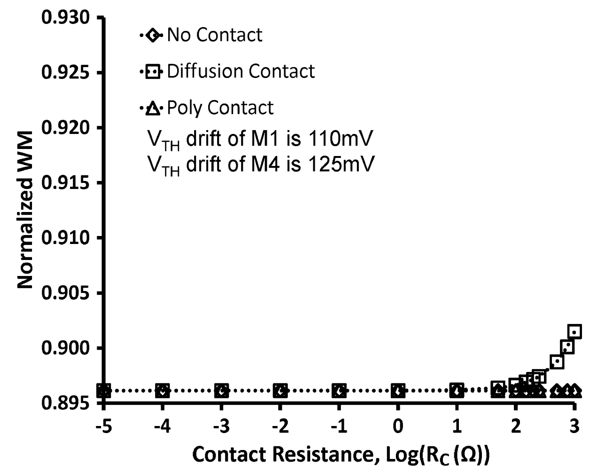


Fig. 20. Normalized WM under NBTI and PBTI versus contact resistance. WM is normalized with respect to the case with no contact resistance and no NBTI/PBTI stress. WM degradation at 32 nm node caused by the combined effects of NBTI/PBTI and diffusion contact resistance is around 10.3% to 10.1%.

only during WL turning on period, the $V_{\rm TH}$ drifts of access transistors are negligible. $V_{\rm TH}$ drift of M1 lowers the trip point of INV_1, and $V_{\rm TH}$ drift of M4 causes increase of the Read disturb voltage, resulting in RSNM degradation with usage time.

By using ac Reaction-Diffusion model, $V_{\rm TH}$ drifts induced by NBTI and PBTI for 10^6 s of M1 and M2 are calculated to be 110 and 125 mV, respectively, in the worst case, leading to RSNM degradation of about 22% without considering contact resistance effect as shown in Fig. 17. Fig. 17 also shows that RSNM degradation becomes more serious when the cell is impacted by both NBTI/PBTI and the diffusion contact resistance. Furthermore, the Read delay increases when the cell is impacted by NBTI and PBTI according to Fig. 18. The reason is that M4 is on the BLB discharging path, leading to longer Read delay with larger $V_{\rm TH}$ of M4. Fig. 18 also shows that NBTI/PBTI and the diffusion contact resistance degrade SRAM Read performance cumulatively.

B. Write Operation

Referring to Fig. 14, larger R5, R7, and R9 reduce the holding strength of pMOS M1, thus facilitating pull-down of the storage node Q. Larger R1 impedes BL to discharge Q through M5. Larger R6, R8, and R10 impede M2 to charge up node QB, and larger R2 also prevents BLB to charge up QB through M6. Thus, larger R5, R7, and R9 improve WM, while larger R1, R2, R6, R8, and R10 degrade WM. Nevertheless, charging up QB is the second order effect during Write, and WM is mainly impacted by R1, R5, R7, and R9. As shown in Fig. 19, WM is improved by larger diffusion contact resistance, but is relatively insensitive to the gate-poly contact resistance because gate-poly contacts are not on the access paths of Q and QB. When the diffusion contact resistance approaches 1 kΩ, WM improves by about 2.5%.

When the cell is also impacted by NBTI and PBTI, in the worst case, $V_{\rm TH}$ of M2 and M3 increase, while $V_{\rm TH}$ of M1 and M4 remain unchanged. The $V_{\rm TH}$ drifts of M5 and M6 are negligible. Weak M2 slows down the charging of QB, and weak M3 slightly impedes the discharging of Q. Consequently, WM of SRAM cell under NBTI and PBTI degrades in the worst case. Fig. 20 shows the relation between WM and contact resistance when $V_{\rm TH}$ of M2 and M3 are 110 and 125 mV, respectively. As can be seen, WM degrades about 10% due to NBTI and PBTI.

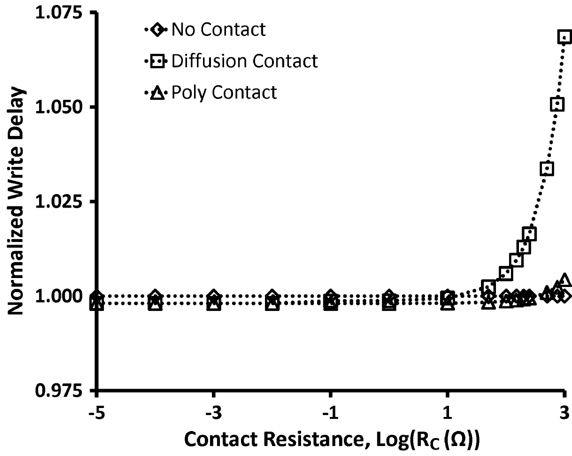


Fig. 21. Normalized write delay versus contact resistance. Write delay is normalized with respect to the case with no contact resistance. Write delay degradation at 32 nm node by diffusion contact resistance is around 0.6% to 3.4%.

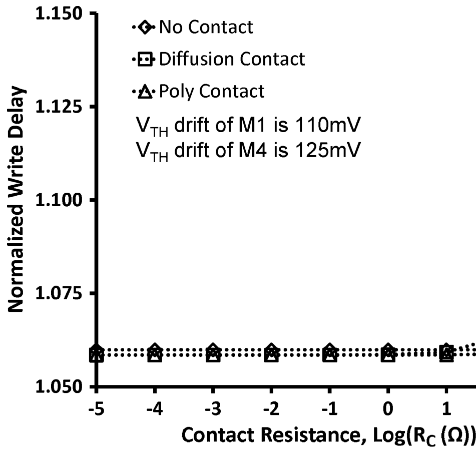


Fig. 22. Normalized write delay under NBTI and PBTI versus contact resistance, write delay is normalized with respect to the case with no contact resistance and no NBTI/PBTI stress. Write delay degradation at 32 nm node caused by the combined effects of NBTI/PBTI and diffusion contact resistance is around 6.62% to 9.65%.

In contrast with RSNM, larger diffusion contact resistance improves WM slightly (about 0.5%), as the current charging QB is limited by M2 under NBTI effect.

Write delay is defined as the latency between the time WL rises to half V_{DD} and the time Q and QB cross each other. Write delay normally tracks WM, and better (higher) WM would improve Write delay in general. However, Write delay is also affected by the R_C time constant, and larger diffusion contact resistances lead to longer Write delay as shown in Fig. 21. Additionally, Fig. 22 shows the relation between Write delay and the contact resistance when the cell is under NBTI and PBTI stress. The Write delay can be seen to degrade about 6% with NBTI and PBTI. The Write delay also increases sharply when the diffusion contact resistance is larger than 100 Ω.

C. SRAM Power-Gating Structure

In power-gated SRAM, when diffusion contact resistances increase, the equivalent resistance between VVDD and VDD (header-gated structure) and VVSS and VSS (footer-gated structure) also increase. It causes decrease of VVDD in a header-gated structure and increase of VVSS in a footer-gated structure as shown in Figs. 23 and 24, respectively. Consequently, the voltage across the SRAM array reduces, and RSNM degrades while WM improves. On the other hand, larger diffusion contact resistances reduce the leakage during Standby mode. It also reduces Standby VVDD of header-gated structure, and increases Standby VVSS of footer-gated structure shown in Figs. 25 and 26, respectively. However, the changes in virtual supply/GND voltage during Standby mode are smaller than those during Active mode. Since the current flowing through the SRAM during Standby is significantly smaller than that during Active mode.

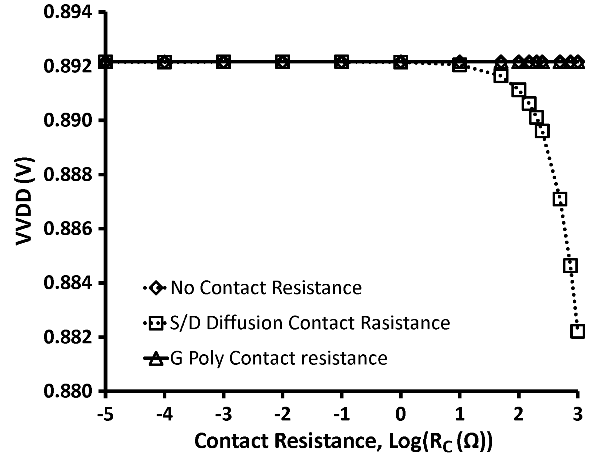


Fig. 23. Active mode VVDD of a header power-gating structure. Active mode VVDD degradation at 32 nm node by diffusion contact resistance is around 1.03 to 5.06 mV.

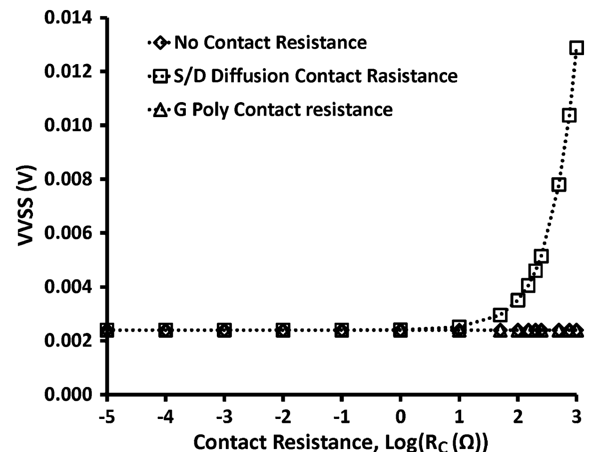


Fig. 24. Active mode VVSS of a footer power-gating structure. Active mode VVSS degradation at 32 nm node by diffusion contact resistance is around 1.11 to 2.74 mV.

When the power switch turns on during wake-up transition, large wake-up current flows through the package parasitic capacitors, inductors, and resistance, resulting in VVDD bounce in header-gated structure or VVSS bounce in footer-gated structure. As the diffusion contact resistance increases, the wake-up current reduces and virtual supply/GND bounce is mitigated. However, due to reduced wake-up current, the wake-up time becomes longer.

V. NBTI/PBTI ON SRAM SENSING STRUCTURE

Two commonly used differential sensing amplifier structure, AMP_A [see Fig. 27(a)] and AMP_B [see Fig. 27(b)] are compared. These two amplifiers would have similar performance if

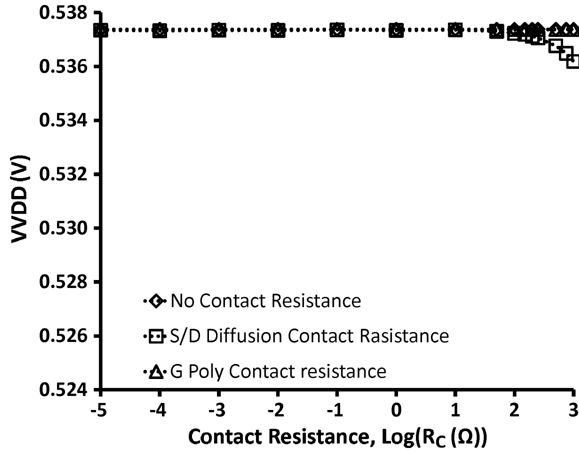


Fig. 25. Standby mode VVDD of header power-gating structure. Standby mode VVDD degradation at 32 nm node by diffusion contact resistance is around 0.15 to 0.61 mV.

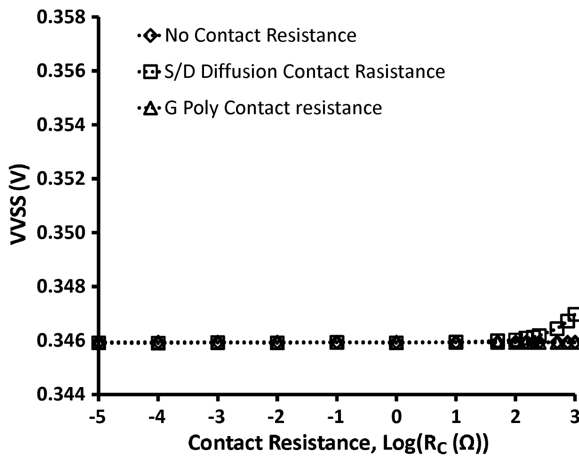


Fig. 26. Standby mode VVSS of footer power-gating structure. Standby mode VVSS degradation at 32 nm node by diffusion contact resistance is around 0.08 to 0.5 mV.

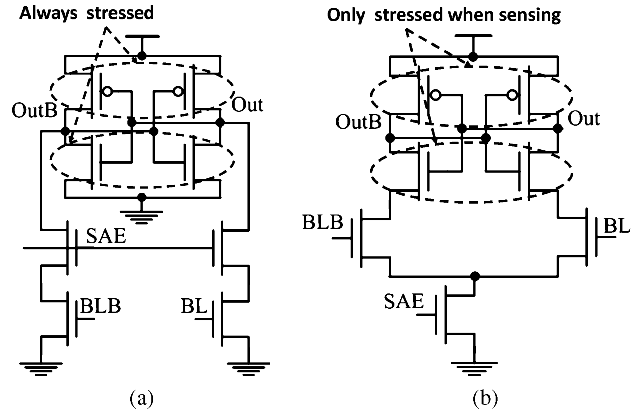


Fig. 27. Two commonly used differential sensing amplifier structures: (a) AMP_A and (b) AMP_B.

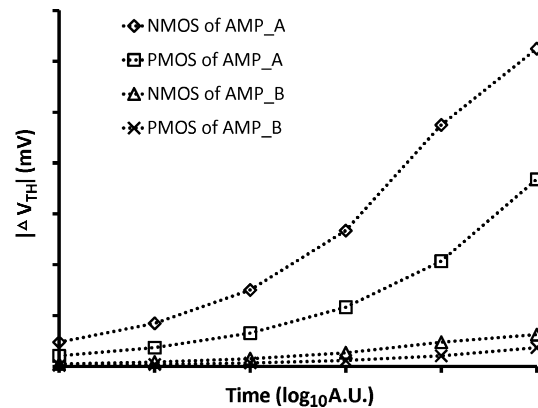


Fig. 28. V_{TH} drifts of sense amplifiers due to NBTI and PBTI.

they were not impacted by NBTI and/or PBTI. In reality, the pMOS pair and nMOS pair of AMP_A's latch are under NBTI and PBTI stress respectively all the time even if AMP_A is in Standby mode. In contrast, when AMP_B is during standby, the signal, SAE, turns off. V_{GS} of the pMOS pair and nMOS pair are zero and suffer no NBTI and PBTI stress respectively. The pMOS pair and nMOS pair of AMP_B are only stressed when it senses data. Therefore, the nMOS and nMOS degradation in AMP_A is much more serious than AMP_B (see Fig. 28). Moreover, if the signal (stress) probabilities of the amplifier are not close to 50% (50%), serious V_{TH} mismatch can occur in AMP_A. As a result, the performance degradation of AMP_A is much more significant than AMP_B.

Recently, large signal single-ended sensing scheme becomes popular due to its process variation tolerance. NAND gate [15], [16], inverter gate [17], and PFET pull-up [18] are often used as in single-ended sensing structures. Because BL pairs are precharged to VDD, the sensing PFETs of these single-ended sensing schemes are not stressed during Standby, and only suffer NBTI stress during SRAM Read cycle. Furthermore, single-ended sensing schemes have no V_{TH} mismatch problem that plagues the small signal differential amplifier. Thus, their long-term degradations are very small. Hence, large signal single-ended sensing scheme has better NBTI/PBTI tolerance than differential sensing scheme.

VI. Conclusion

In this paper, we presented a comprehensive analysis on the impacts of NBTI and PBTI on power-gated SRAM stability, margin, and performance based on BSIM 32 nm high-κ metal-gate Predictive Model. The combining effects of NBTI and PBTI with contact resistance on SRAM array are also investigated. Differential sensing scheme and large signal single-ended sensing structure were also compared when NBTI/PBTI were considered.

We showed that the header/footer structure played an important role in determining the VVDD and VVSS. In the worst case, contact resistant and NBTI/PBTI jointly degraded SRAM RSNM and Read performance. Nevertheless, if a SRAM cell suffered PBTI only, the impact on RSNM would depend on the signal (stress) probability. When both NBTI and PBTI were present, and both NFET driving transistors were stressed, the RSNM degradation induced by NBTI could be partially mitigated by PBTI. The WM could improve or degrade, depending on the presence of NBTI, PBTI, or both, and the signal (stress) probability. With contact resistance, the Write delay increased

but WM improved. The SRAM active power and standby/sleep power decreased with the stress time. After power switch was stressed, the virtual supply bounce decreased. The wake-up time increased if only the power switch was stressed due to higher $V_{\rm TH}$ of the power switch, and decreased if the SRAM array was also stressed due to higher Standby/Sleep mode VVDD or lower Standby/Sleep mode VVSS. When contact resistance impacts were also considered, virtual supply/GND bounce during wake-up transition was reduced with increasing contact diffusion resistances, but wake-up time became longer. Finally, we showed that by judiciously choosing the sense amplifier structure, the performance degradation induced by NBTI and PBTI could be significantly reduced.

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