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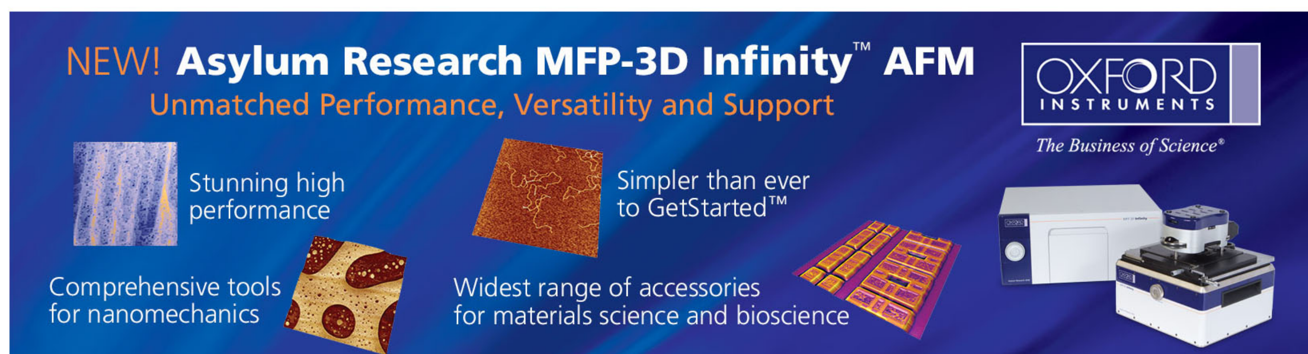

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Mechanism of Schottky barrier height modulation by thin dielectric insertion on n-type germanium

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Although high channel electron mobility has been reported after some passivation techniques, the performance of n-channel Ge metal-oxide-semiconductor field-effect transistor is still limited by the high Schottky barrier height at the metal/n-Ge contact interface, which comes from the Fermi level pinning effect. Recent experiments demonstrated that the Schottky barrier height can be reduced by inserting a thin dielectric layer between metal and Ge. However, the mechanism has not been well clarified. In this paper, the metal induced gap state model, the dipole layer model, and the fixed charge model are verified by varying contact metals, dielectric thicknesses, as well as the annealing temperatures. The pinning factor is improved slightly by dielectric insertion but its value is independent of the dielectric thickness and is still much lower than the ideal value of the non-pinning case. This pinning effect is consistent with the Fermi level pinning at the metal/TiO_2 interface. After thermal process, no interfacial layer forms at the TiO_2/Ge interface and the TiO_2 crystallizes gradually after annealing but the Schottky barrier height increases. Since the amount of fixed charges in the thin dielectric layer estimated from a metal-insulator-semiconductor structure is about 2×10^{11} cm^{-2} and is insufficient to produce the observed 0.5 eV Schottky barrier height reduction, it is thus recommended that the main mechanism comes from the change of interface dipoles and the annealing effect is attributed to the short-range ordering of the TiO_2 layer. Furthermore, dielectric with low conduction band offset which has good thermal stability should be explored. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4813834]

Improving the performance of Si-based metal-oxide-semiconductor field-effect transistor (MOSFET) devices by scaling down has encountered many limitations. Because Ge has higher electron (3900 vs 1400 cm^2/Vs) and hole (1900 vs 500 cm^2/Vs) bulk mobility than Si, it becomes one of the potential candidates to replace Si as the channel material in the future.[1] Although high channel electron mobility has been measured after some passivation techniques, the driving current of n-channel Ge MOSFET is still poor than that of Si MOSFET due to the high contact resistance between metal and n$^+$ Ge source/drain region.[2–5] To reduce contact resistance, high doping concentration and low Schottky barrier height are the most critical factors. Unfortunately, the low solid-state solubility of n-type dopants in Ge causes incomplete activation.[6–8] Furthermore, the specific contact resistance at the metal/n$^+$ Ge contact is high due to the high Schottky barrier height at the metal/n-Ge interface, which comes from the Fermi level pinning (FLP) effect.[9,10]

Recent experiments demonstrated that the Schottky barrier height can be reduced by inserting a thin dielectric layer between metal and Ge as a tunneling barrier. Several dielectrics have been employed. They are Si_3N_4,[12–15] Ge_3N_4,[16] MgO,[17–19] Al_2O_3,[15,19–25] GeO_x,[23] and TiO_2.[23–25] Schottky barrier height as low as 65 meV has been reported on the Al/TiO_2/Ge structure.[24] Three possible mechanisms have been proposed. Originally, it was proposed that the inserted dielectric layer can block the electron wave function from metal to semiconductor and therefore decrease the number of metal induced gap states (MIGS).[11,14,17,18,23] Latter researches suggest that the dipole formed at the metal/semiconductor interface would cause potential drop to modulate the Schottky barrier height.[13,15,21,22,26–29] Hu *et al.* proposed that the fixed charges in the non-ideal dielectric layers would also cause an extra potential drop across the dielectric layer.[29] In this work, sequential experiments were designed to clarify which mechanism dominates the Schottky barrier height modulation on Ge. The thickness effect and the post deposition annealing effect on the Schottky barrier height are also investigated.

N-type Sb doped (100)-oriented Ge wafer with resistivity of 0.01 Ω-cm was used. Samples were dipped in diluted HF solution (H_2O:HF = 20:1) and DI-water for 1 min circularly by three times to clean the surfaces. Then samples were loaded to an atomic layer deposition (ALD) system to deposit thin TiO_2 layer immediately. The TiO_2 layer was deposited using Tetrakis(dimethylamino) titanium (TDMAT) and H_2O as precursors at 250 °C. The thicknesses of 1 nm and 7 nm are grown by 22 and 154 cycles, respectively. Some samples were then *in-situ* deposited by a 5-nm-thick TiN layer in the same ALD system using TDMAT as precursor and N_2 plasma. After ALD deposition, samples were annealed in vacuum furnace at 300 °C, 400 °C, and 600 °C for 30 min. Then a 300-nm-thick Al was deposited on these samples by a thermal coater and was patterned by a typical lithography process and reactive ion etching process. The samples without TiN contact metal were deposited with different metals, including Pt by a sputtering system, and Ni and Co by an e-gun system. The contact metal was patterned by lift-off process. The other processes were identical to

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those of the samples using TiN as contact metal. Finally, after removing the native oxide on the sample backside by buffered oxide etchant (BOE), backside contact was completed with a 300-nm-thick Al deposition by a thermal coater. The electrode area is $4.9 \times 10^{-4}\,\mathrm{cm}^{-2}$ for all metals.

The work functions of Pt, Ni, Co, and TiN are 5.65 eV, 5.15 eV, 5 eV, and 4.5 eV, respectively.[30,31] Metal with further lower work function was not used in this experiment because the Schottky barrier height on the 7-nm-thick TiO_2 contact would be very low (about 0.04 eV for TiN) so that we cannot extract the Schottky barrier height accurately. Figs. 1(a) and 1(b) show the I-V characteristics of the 1-nm-thick and 7-nm-thick TiO_2 contacts, respectively. With higher work function metal, the current densities are lower, which indicates that Schottky barrier height increases with the work function.

Fig. 2 shows the extracted Schottky barrier height of the 1-nm-thick and 7-nm-thick TiO_2 contacts with different contact metals. The Schottky barrier height of the pure metal/Ge contact is also shown in the figure. These Schottky barrier height values were extracted by the thermionic emission model at reverse bias at temperatures from 25 °C to 100 °C.[20] The inset shows an example of the TiN/TiO_2(7 nm)/Ge contacts. The slopes of the linear regression lines give the pinning factors S. The pinning factor is about 0.052 for the pure Ge junction which is consistent with that reported in literatures.[9,10] For the contacts with TiO_2 insertion layer, the pinning factor is 0.144 for the contacts with 1-nm-thick TiO_2 and 0.126 for the contact with 7-nm-thick TiO_2. These values are larger than that of the pure Ge junction which means that the FLP effect is mitigated by the TiO_2 insertion layer. The improvement of pinning factor compared with pure Ge may come from the alleviating of MIGS effect. However, it should be noticed that the pinning factors of the contacts with both TiO_2 thicknesses are about the same, which indicates that the depinning effect of the 7-nm-thick TiO_2 is not better than that of the 1-nm-thick TiO_2. In the case of complete depinning, the pinning factor should approach to 1; the small pinning factors indicate that the FLP effect is not solved completely by the TiO_2 insertion layer. According to the MIGS model, the pinning factor S can be estimated as $S = \frac{1}{1+0.1(\varepsilon_\infty - 1)^2}$, where ε_∞ is the electronic component of dielectric constant.[32] Applying this model at the metal/TiO_2 interface, the pinning factor S is estimated to be 0.153 as $\varepsilon_\infty(TiO_2) = 8.427$.[33] Since the calculated pinning factor is close to the experimental pinning factor, it is possible that the FLP with TiO_2 insertion is due to the FLP at the metal/TiO_2 interface.

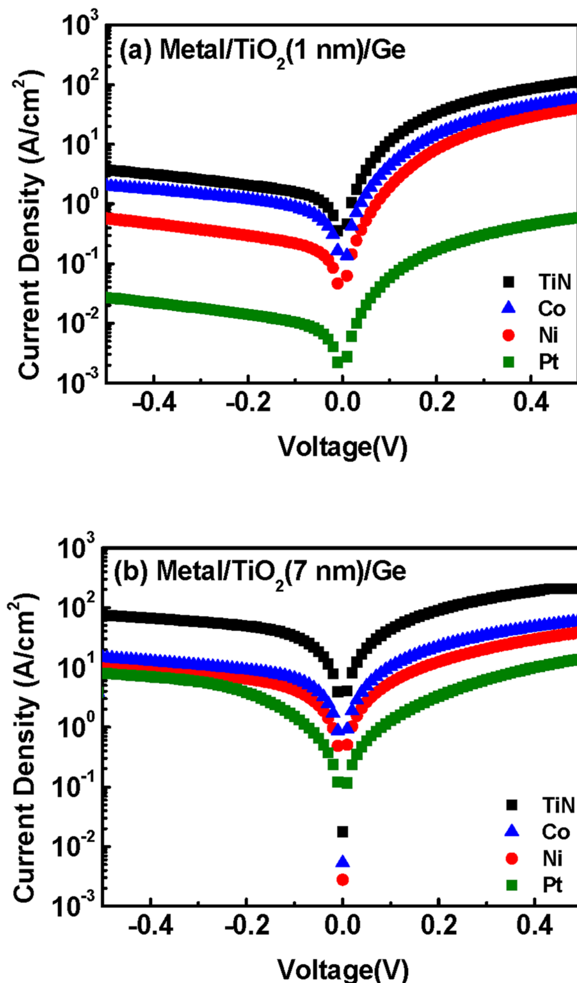

FIG. 1. Current-voltage characteristics of the Schottky contacts with different contact metals. The contact structure is (a) metal/TiO_2 (1 nm)/Ge and (b) metal/TiO_2 (7 nm)/Ge.

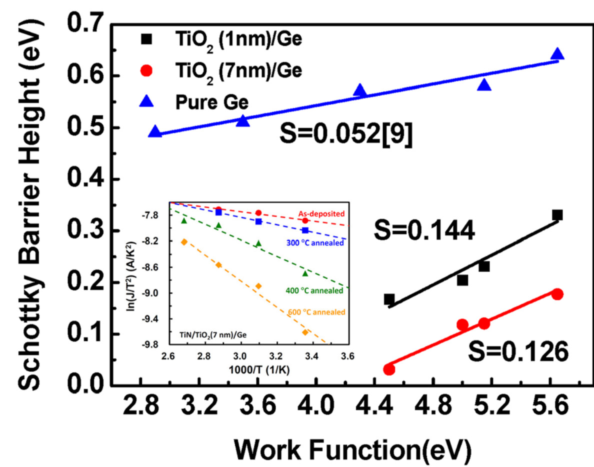

FIG. 2. Extracted effective Schottky barrier height of the contacts without TiO_2 insertion layer, with 1-nm-thick TiO_2 insertion layer, and with 7-nm-thick TiO_2 insertion layer. The inset shows the extraction of the Schottky barrier height of the TiN/TiO_2 (7 nm)/Ge contacts as an example.

Since the lower Schottky barrier height of the 7-nm-thick TiO_2 contact than the 1-nm-thick contact cannot be explained by the more effective suppression of the MIGS effect by the thicker dielectric, but because the pinning position is changed more for thicker TiO_2 layer. The change of pinning position may result from two factors, fixed oxide charges or dipoles formed at metal/TiO_2 interface and/or TiO_2/Ge interface; both can introduce an additional potential drop in the current conduction path and results in the reduction of the Schottky barrier height.[29]

Either dipoles or fixed charges may be changed after thermal process, which in turn changes the effective Schottky barrier height. Fig. 3 shows the Schottky barrier heights of the contacts with 1-nm-thick and 7-nm-thick TiO_2 insertion layer before and after annealing in vacuum at 300 °C, 400 °C, and 600 °C for 30 min. As the annealing temperature increases, the Schottky barrier height increases,

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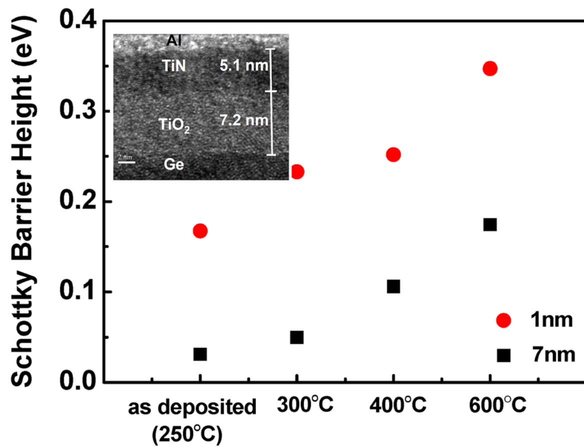

FIG. 3. Extracted effective Schottky barrier height of the contacts after thermal annealing. The inset is the cross-sectional TEM micrograph of the contact with 7-nm-thick TiO_2 insertion layer after 600 °C annealing.

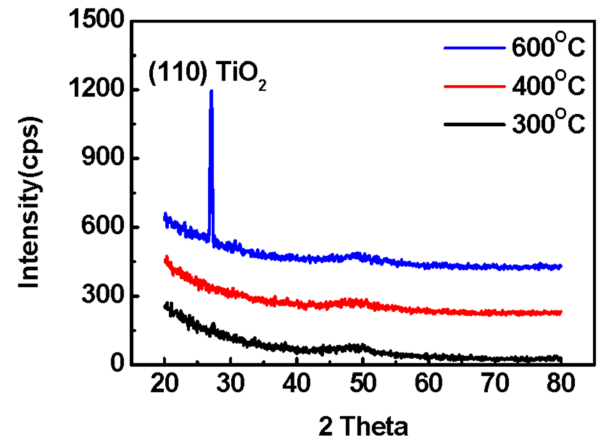

FIG. 4. X-ray diffraction spectra of the contacts with 7-nm-thick TiO_2 insertion layer after annealing at 300, 400, and 600 °C.

too. It is noticed that the increments of the Schottky barrier height of the 1-nm-thick and the 7-nm-thick TiO_2 contacts are similar, and the Schottky barrier heights of the 7-nm-thick TiO_2 contact are still lower than those of the 1-nm-thick TiO_2 contact after annealing. To observe if there is a new interfacial layer formed after annealing, the cross-sectional structure of the 600 °C annealed TiN/TiO_2/Ge contact was inspected by the high-resolution transmission-electron-microscope (TEM) and the micrograph is inserted in Fig. 3. It is clearly that there is no interfacial layer formed at the TiO_2/Ge interface and the TiN/TiO_2 interface. This result suggests that the Schottky barrier height increment is not due to new layer formation after annealing. If the Schottky barrier height modulation mechanism of the TiO_2-inserted contacts mainly results from the fixed charges in TiO_2 and these charges are reduced by the annealing process, the Schottky barrier height of the 7-nm-thick TiO_2 contact should be close to that of the 1-nm-thick TiO_2 contact. However, this prediction conflicts with the experimental results. It could be estimated that if the Schottky barrier height modulation comes from the fixed charges, the charge density should be as high as 3×10^{13} cm^{-2} to produce a 0.5 eV Schottky barrier height reduction assuming the relative dielectric constant of TiO_2 is 80.[34] Lee has studied the C-V characteristics of the TiO_2/Ge and TiO_2/SiO_2/Ge structures.[35] Although the TiO_2/Ge sample showed distorted C-V curve due to its high leakage current, the difference in total charge between the two samples is only 2×10^{11} cm^{-2}, which is much lower than that required to produce a 0.5 eV Schottky barrier height reduction. Therefore, it is recommended that the Schottky barrier height modulation of the TiO_2-inserted contact is mainly caused by the interface dipoles.

Fig. 4 shows the XRD spectra of the 7-nm-thick TiO_2-inserted junction after annealing at 300 °C, 400 °C, and 600 °C for 30 min, respectively. The TiO_2 and TiN layers remain in amorphous state after 400 °C annealing. The (110)-oriented rutile phase of TiO_2 is detected on the 600 °C annealed sample. However, Raman analysis suggested short-range ordering in the amorphous TiO_2 phase at annealing temperatures of 200–400 °C.[36] Thus, it is postulated that with the increase in annealing temperature, the TiO_2 layer is gradual crystallized and the interface dipoles change simultaneously. The change of dipoles affects the stability of the Schottky barrier height modulation.

In summary, we examined the three possible mechanisms, MIGS model, dipole model, and fixed charge model, of the dielectric insertion induced Schottky barrier height modulation of the metal/TiO_2/n-type Ge contact. The main cause is not the release of FLP effect but the shift of pinning position. Interface dipole plays more significant role than the fixed charge. Thermal annealing in vacuum at temperature as low as 300 °C changes the interface dipole due to the short-range ordering of the TiO_2 layer so that the Schottky barrier height changes. The Schottky barrier height of the Al/TiO_2(7 nm)/Ge contact increases from 0.03 to 0.11 eV after 400 °C annealing. Beyond 400 °C, the Schottky barrier height would be too high to maintain good contact property.

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