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Abnormal sub-threshold swing degradation under dynamic hot carrier stress in HfO_2/TiN n-channel metal-oxide-semiconductor field-effect-transistors

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This work finds abnormal sub-threshold swing (S.S.) degradation under dynamic hot carrier stress (HCS) in n-channel metal-oxide-semiconductor field-effect-transistors with high-k gate dielectric. Results indicate that there is no change in S.S. after dynamic HCS due to band-to-band hot hole injection at the drain side which acts to diminish the stress field. Moreover, the impaired stress field causes the interface states to mainly distribute in shallow states. This results in ON state current and transconductance decreases, whereas S.S. degradation is insignificant after dynamic HCS. The proposed model is confirmed by one-side charge pumping measurement and gate-to-drain capacitance at varying frequencies. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4811784]

Consumer electronic products which are combined display design,[1–5] memory circuits,[6–10] and IC circuits have popularized considerably in the last few years. To achieve high speed and lightweight, the continuous scaling-down of metal oxide semiconductor field effect transistors (MOSFETs) is driving conventional SiO_2-based dielectric to only a few atomic layers thick, leading to excessive gate leakage current and reliability issues.[11] To solve the leakage current problem, a high-k material is utilized as gate insulator to reduce both tunneling gate leakage and power consumption in complementary MOS (CMOS) circuits.[12–14] Furthermore, the high-k/metal gate can be integrated with silicon-on-insulator techniques.[15–18] Additionally, charge trapping in high-k gate stacks remains a key reliability issue, since it causes threshold voltage (V_{TH}) shift and drive current degradation[19–22] due to the filling of pre-existing traps in the high-k dielectric layer.[23–25] In addition, charge trapping effect is found to have great impact on hot carrier stress (HCS)-induced device instability since carriers tend to be injected into the high-k layer.[26,27] Hot carrier injection is a critical issue for submicron transistors since devices encounter higher lateral electric fields, and this issue is even more severe in high-k/metal gate MOSFETs. Moreover, in circuit applications, the CMOS inverter is always operated with dynamic gate voltage (V_G) rather than a constant V_G. Therefore, in this experiment, dynamic HCS has been simulated to resemble real CMOS operation conditions for high-k/metal gate n-MOSFETs. The dynamic HCS condition was with square waveform of VG switching from −2 V to 2 V and a fixed $V_D = 3$ V with source and body grounded. The $V_G = -2$ V, $V_D = 3$ V condition can induce band-to-band hot hole generation, and the $V_G = 2$ V, $V_D = 3$ V condition can lead to the most serious HCS degradation. Additionally, abnormal sub-threshold swing (S.S.) degradation could be observed after dynamic HCS, which is a degradation trend different from previous studies.[28] This unusual phenomenon is analyzed by the saturation drain current-gate voltage (I_D-V_G), gate induced drain leakage (GIDL) current, and one-side charge pumping measurements. In addition, the drain-to-gate capacitance (C_{GD}) at varying frequencies was used to explain the model proposed in this work.

High-performance TiN/HfO_2 n-MOSFETs with an interfacial layer (IL) thickness of 30 Å fabricated via 28-nm CMOS technology were studied in this paper. Devices were fabricated using a conventional self-aligned transistor which progressed via the gate-first process. For gate-first process devices, high quality thermal oxides with thicknesses of 30 Å were grown on a (100) Si substrate as an IL oxide layer. After standard cleaning procedures, 30 Å of HfO_2 film was sequentially deposited by atomic layer deposition. Next, 10 nm of TiN film was deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The activation for source/drain and poly-Si gate was performed at 1025 °C. The channel and source/drain doping concentrations were about 1×10^{18} cm^{-3} and 1×10^{21} cm^{-3}, respectively. In this study, the dimensions of the devices were width (W)/length (L) = 10/1 μm. The dynamic HCS condition was with square waveform of V_G switching from −2 V to 2 V and a fixed $V_D = 3$ V with source and body grounded. The stress was briefly interrupted to measure the linear I_D-V_G, saturation I_D-V_G, GIDL current, charge pumping, and gate-to-drain capacitance (C_{GD}) at various frequencies. In the C_{GD} measurement, measurement signals were applied to the gate electrode, and drain electrode was connected to a capacitance sensing unit with frequency = 2 MHz. In the charge pumping measurement, the base of V_G pulse (V_G-base) was fixed at −0.8 V and the peak of V_G pulse ($V_{G,\,high}$) was ranging from −0.4 V to 2 V with frequency = 5 MHz. GIDL current was measured at $V_G = -0.5$ V and $V_D = 2.4$ V. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer and a Cascade M150 probe station.

Figure 1(a) shows the I_D-V_G and corresponding transconductance-gate voltage (Gm-V_G) at linear region measurement after dynamic HCS for high-k/metal gate n-MOSFETs. For dynamic HCS, the drain is biased at 3 V and the gate bias is square waveform switching from −2 V to 2 V, where $V_G = 2$ V was where the most serious HCS degradation occurred for the device. It can be seen that both ON state current (I_{ON}) and Gm degrade under dynamic HCS, while there is no significant change in S.S. This abnormal S.S. degradation phenomenon is different from general dynamic HCS, where S.S. shows a clear degradation.

Figure 1(b) shows the forward I_D-V_G and the reverse I_D-V_G curves (source/drain interchanged) measured at the saturation region after dynamic HCS for high-k/metal gate n-MOSFETs. It can seen that in the forward saturation I_D-V_G curve, there is only an insignificant decrease in I_{ON} because measured V_D depletes the main interface states and trapping charge. However, in the reverse I_D-V_G operation, there is an early turn on at the OFF state with S.S. degrading at the sub-threshold region after dynamic HCS. These phenomena may be due to the hole injection and interface state generation at the drain side, as shown in the inset of Fig. 1(b).

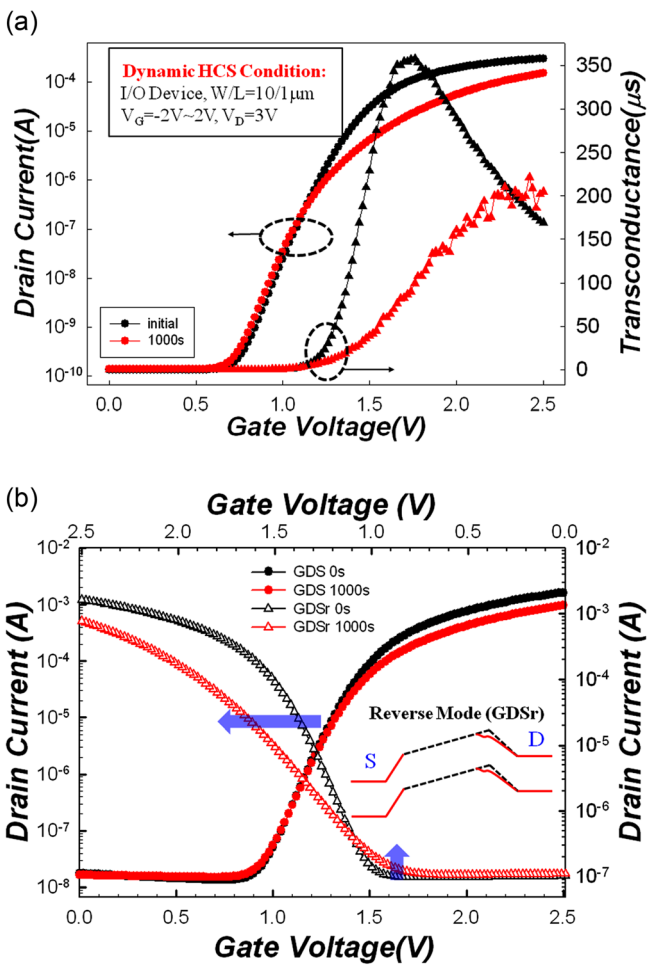

FIG. 1. (a) I_D-V_G and corresponding Gm-V_G at linear region measurement shows no significant change in S.S. (b) Forward I_D-V_G and the reverse I_D-V_G (source/drain interchanged) at the saturation region measurement after dynamic HCS for high-k/metal gate n-MOSFETs. Inset shows the lateral energy band diagram with hole trapping lowering the V_{TH} at the reverse I_D-V_G measurement.

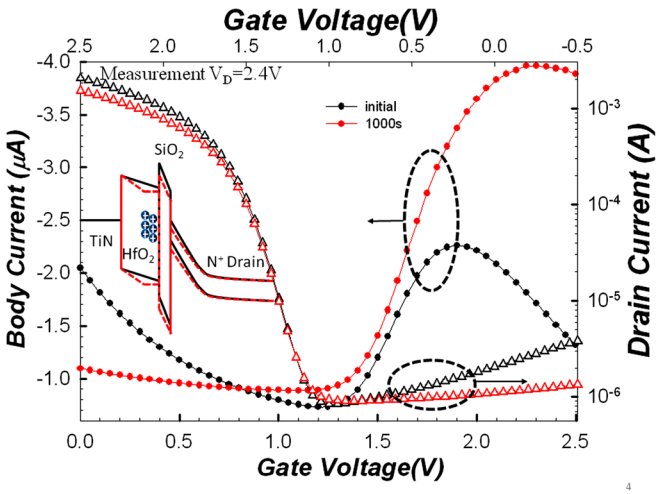

FIG. 2. I_D-V_G and corresponding I_B-V_G measurement at $V_D = 2.4$ V showing GIDL current decrease after dynamic HCS. Inset shows that hole trapping increases band-to-band tunneling distance.

To confirm the phenomenon of hole injection, Fig. 2 shows measurements of I_D-V_G corresponding to body current-V_G (I_B-V_G) at $V_D = 2.4$ V. It can be observed that the GIDL current decreases after HCS due to hole trapping increasing the band-to-band tunneling distance, as shown in the inset of Fig. 2. Obviously, the trapping holes is generated by band-to-band hot hole tunneling when the dynamic V_G switches to −2 V at constant $V_D = 3$ V. Then the band-to-band hot hole prefers to inject into the high-k layer because of a strong electric field towards the gate. To further confirm the presence of hole trapping and interface state generation, the charge pumping method was utilized.[29] Figure 3 shows charge pumping current (I_{CP}) versus $V_{G,high}$ and shows that I_{CP} increases by about 330% and flat band voltage (V_{FB}) shifts 0.5 V toward the negative direction after dynamic HCS. Nevertheless, this I_{CP} increase and V_{FB} shift were due to interface state generation and hole trapping, respectively. Since hole trapping can lead to V_{FB} and V_{TH} downward band bending, $V_{G,high}$ contacts the V_{FB} and V_{TH} curves to produce an earlier I_{CP}. Moreover, by measuring I_{CP} with

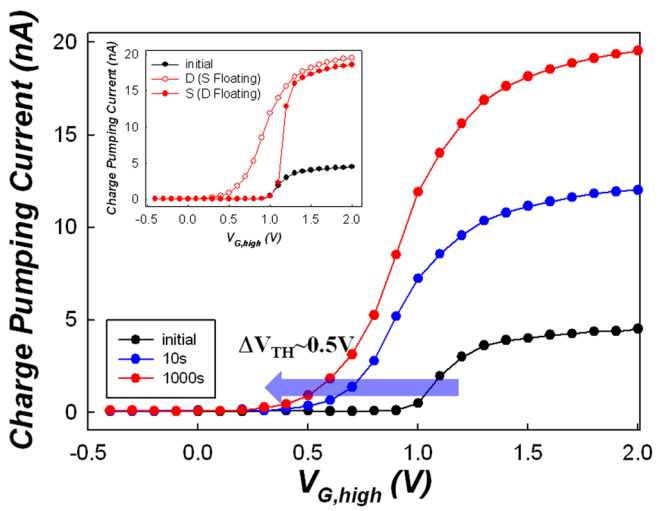

FIG. 3. I_{CP}-$V_{G,high}$ shows an increase of 330% and V_{FB} shift of 0.5 V toward the negative direction during dynamic HCS. Inset shows one-side floating CP technique with floating source or drain terminal to measure I_{CP}.

floating source or drain terminal, the location of charge trapping can be determined. The inset of Fig. 3 shows the one-side floating CP technique with floating source or drain terminal to measure I_{CP}. Clearly, the drain floating only results in an increasing I_{CP}, but no shift in V_{FB}. However, the source floating shows not only increasing I_{CP} but also V_{FB} shifting 0.5 V toward the negative direction after dynamic HCS. Therefore, the hole trapping at the drain side can be confirmed by this one-side floating CP technique.

Based on the experimental analysis above, a physical model is proposed to explain the abnormal S.S. degradation under dynamic HCS. Our experimental observations confirm both hole trapping at the high-k layer and interface state generation near the drain side, as shown in Fig. 4(a). Corresponding to the lateral energy band diagram, as shown in Fig. 4(b), the trapped holes can form a buffer region at the depletion region to reduce the stress electron field, in turn reducing electron kinetic energy.[30] Therefore, the weakened hot electron kinetic energy is not enough to generate a deeper level interface states during dynamic HCS, but mostly shallow states, as shown in Fig. 4(c). Consequently, when a small sweep Vg is applied ($V_G < V_{TH}$) at the linear I_D-V_G measurement, the Fermi energy is still insufficient to cover the shallow states at the sub-threshold region, resulting in an insignificant change in S.S. after dynamic HCS, as shown in Fig. 1(a). However, when a large sweep V_G is applied ($V_G > V_{TH}$), the Fermi energy moves up to cover the shallow states; thus, the shallow states fill with electron to form negative charge states and then lower the I_{ON}.

To further prove the presence of shallow state generation after dynamic HCS, the capacitance measurement technique can be utilized to confirm our assumption. Figure 5 shows normalized C_{GD} curves at various measured frequencies before and after dynamic HCS. It can be clearly seen that capacitance rises early, indicated by the blue dashed circle, due to hole trapping at the drain side, which is in agreement with previous experimental data. In addition, the blue dashed circle marks a stretched out capacitance for different frequencies, indicating that there was interface state generation at the drain side after dynamic HCS, also in agreement with previous analyses. More worthy of mention is the green dashed circle region which marks a two-step capacitance that become less apparent at lower frequencies. This behavior is dominated by channel carrier trapping and detrapping time when capacitance is measured. For higher frequency measurements, the electron can fill up interface states, because there is insufficient time to allow the trapping electron to drop out from shallow states. Therefore, the trapping electron forms a higher barrier height at the drain side, as shown in the upper left inset of Fig. 5, leading an evident two-step capacitance at higher frequency measurements. For the lower frequency measurements, the electron also can fill up interface states but has enough time to allow the trapping electron to drop from shallow states. Thus, the trapping electron forms a lower barrier height at the drain side, as shown in the bottom right inset of Fig. 5, leading to only a slight two-step capacitance at lower frequency measurements. By this capacitance measurement technique at various frequencies, the contribution of shallow states can be known after dynamic HCS.

It has been generally thought that dynamic HCS could generate many interface states, resulting in serious S.S. degradation in n-MOSFETs with high-k gate dielectric. However, this work finds abnormal S.S. degradation in that there is no change after dynamic HCS. This is due to band-to-band hot hole injection at the drain side where hot holes act to diminish the stress field. Moreover, the reduced stress field decreases the impact ionization rate; this weaker impact ionization rate leads to the generation of only shallow interface states. Consequently, the shallow states result in decreases in both ON state current and Gm but no significant S.S. degradation after dynamic HCS. The proposed model is explained by one-side charge pumping measurement and

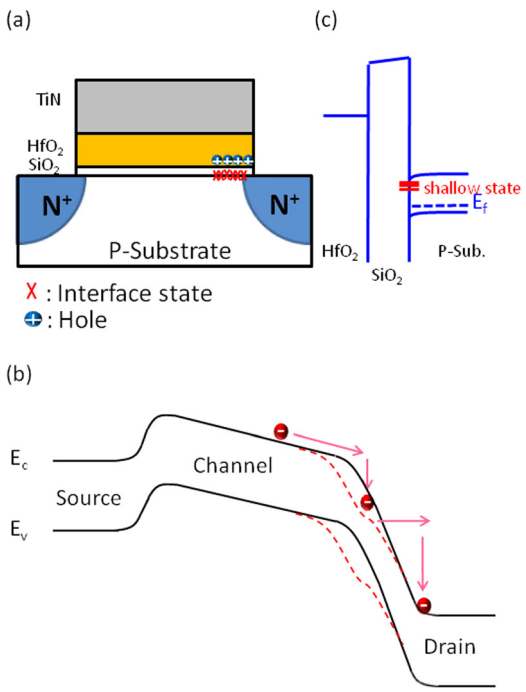

FIG. 4. (a) Diagram of n-MOSFET structure showing hole trapping and interface state generation at the drain side. (b) The lateral energy band diagram indicating that trapping holes form a buffer region at the depletion region to reduce the stress electron field. (c) The energy band diagram shows only shallow states generated after dynamic HCS.

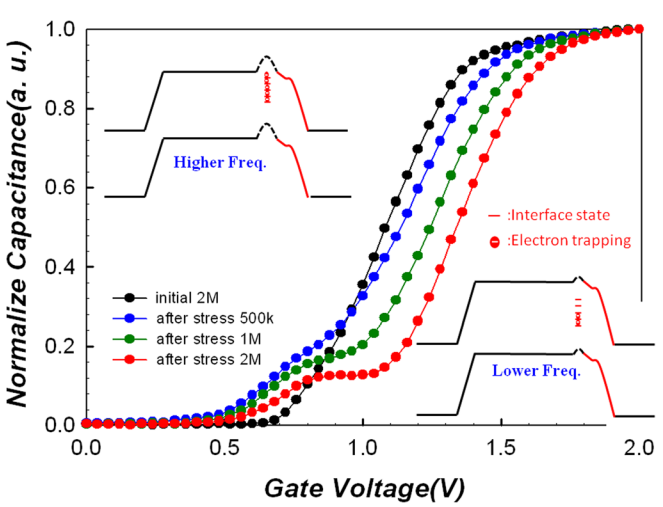

FIG. 5. Normalized C_{GD} curves at various frequencies before and after dynamic HCS. Inset shows the lateral energy band diagram of electron trapping and detrapping behavior for higher and lower measurement frequencies.

C_{GD} at various frequencies. Therefore, the mechanism of abnormal S.S. degradation can be illustrated after dynamic HCS in n-MOSFETs with high-k gate dielectric.

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