Threshold Voltage Design of UTB SOI SRAM With Improved Stability/Variability for Ultralow Voltage Near Subthreshold Operation

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***Abstract*—This paper analyzes and compares the stability, margin, performance, and variability of ultrathin-body (UTB) SOI 6T SRAM cells operating near the subthreshold region with different threshold voltage ($V_{\rm th}$) design. Our results indicate that UTB SOI 6T SRAM cell using low $V_{\rm th}$ devices ($|V_{\rm th}| = 0.19$ V) shows a comparable read static noise margin (RSNM), 41% improvement in σRSNM, 84% improvement in write static noise margin (WSNM), and 67% improvement in σWSNM as comparaed with the case using higher $V_{\rm th}$ devices ($|V_{\rm th}| = 0.49$ V). As $V_{\rm th}$ decreases (work function moves to the band edge), the "cell" access time improves significantly with correspondingly higher standby leakage. For low $V_{\rm th}$ devices ($|V_{\rm th}| = 0.19$ V), it is shown that lowering bit-line precharge voltage by 50 mV reduces the standby leakage by 20%. Our study suggests that the lower $V_{\rm th}$ devices operating slightly into super-threshold region improve the stability/variability significantly and offer higher performance for ultralow voltage SRAM applications.**

***Index Terms*—Metal gate, SOI, subthreshold SRAM, ultrathin-body, variability.**

I. Introduction

SUBTHRESHOLD operation is an efficient technique to achieve ultralow power consumption for circuits by lowering the power supply ($V_{\rm dd}$) below the threshold voltage ($V_{\rm th}$) [1], [2]. UTB SOI MOSFET with thin buried Oxide (BOX) has emerged as a promising candidate to extend CMOS scaling [3]–[5]. Due to its better control of short-channel effects, lower subthreshold swing, and reduced leakage and random dopant fluctuation (RDF) resulting from the use of undoped (or lightly doped) thin silicon film, UTB SOI MOSFET is very attractive for subthreshold circuit applications.

Metal-gates and high-k dielectrics are key performance boosters for CMOS technology in the sub-45 nm nodes. Work function engineering for metal-gates devices has been intensively researched to obtain adequate/low threshold voltages for high performance CMOS devices [6]–[11]. The use of a single midgap metal-gate such as TiN on SOI MOSFET provides suitable threshold voltage for n-channel and p-channel devices simultaneously while keeping the channel undoped [9]. Single-metal single-dielectric (SMSD) engineering remains the simplest and most cost effective of many techniques proposed to achieve the need for multi-$V_{\rm th}$ devices [10]–[12]. UTB SOI SRAM cells with midgap work function devices ($|V_{\rm th}|\sim$0.49 V, $V_{\rm dd} =$ 0.4 V) operating in the subthreshold region show sufficient margin [13]–[15]. However, the impact of threshold voltage design on the stability, performance, and variability of UTB SOI SRAM for ultralow voltage near subthreshold operation has rarely been examined.

In this paper, we analyze and compare the stability, margin, performance, and variability of UTB SOI 6T SRAM cells with lower and higher $V_{\rm th}$ devices. We assess the feasibility of using lower $V_{\rm th}$ devices for ultralow voltage near subthreshold SRAM design. The lower $V_{\rm th}$ devices (with quarter band gap work function) are shown to be capable of supporting the high performance applications, and improving the stability/variability and offering higher performance while trading off leakage for the ultralow voltage SRAM applications. This paper is organized as follows. Section II describes the device design and characteristics used in this study. Section III investigates the impact of $V_{\rm th}$ design on the UTB SOI SRAM cells for ultralow voltage near subthreshold operation, including RSNM, WSNM, "cell" read access time, time-to-write, and cell leakage. Section IV evaluates the effectiveness of commonly used circuit techniques, such as word-line voltage lowering, bit-line precharge voltage lowering, and negative bit-line voltage, for improving the stability, standby leakage, and write ability of the UTB SOI SRAM cell for ultralow voltage near subthreshold opeartion with lower $V_{\rm th}$ devices. Section V compares the variability (σRSNM, σWSNM) of the 6T UTB SOI SRAM cells with low and high $V_{\rm th}$ devices. Section VI concludes the paper.

II. Device Design and Characteristics

In the following sections, we investigate the cell stability, performance, leakage, and variability of UTB SOI 6T SRAM cells with channel doping concentration = 1e16 cm^{-3}, BOX thickness = 10 nm, gate length = 40 nm, EOT = 1 nm, and

Manuscript received May 25, 2010; accepted December 28, 2010. Date of publication May 2, 2011; date of current version July 3, 2013. This work was supported in part by the National Science Council of Taiwan under Contract NSC 99–2221-E-009–174, in part by the Ministry of Education in Taiwan under the Aiming for the Top University Program, and in part by the Ministry of Economic Affairs in Taiwan under Contract 99-EC-17-A-01-S1–124. The review of this paper was arranged by Associate Editor B. Yu.

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Digital Object Identifier 10.1109/TNANO.2011.2105278

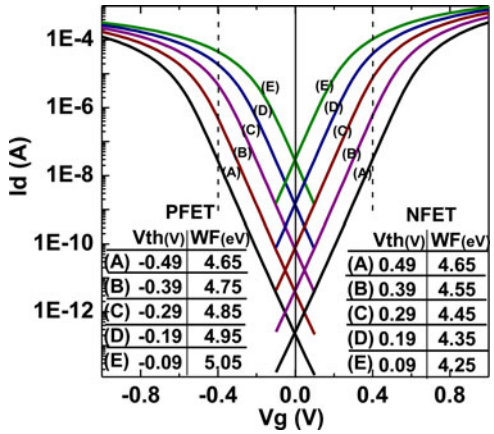


Fig. 1. Log(Id)–Vg characteristics for UTB SOI MOSFETs with various threshold voltages (Vth)/work functions (WF) at Vd = 0.4 V. The |Vth| of NFET and PFET in each case (A–E) are designed with the same absolute value. (V_g = Vth @ Id = 3e–7 A).

channel thickness = 10 nm. The mobility ratio of NFET to PFET is around 2.5. TCAD mixed-mode device/circuit simulations [16] are employed to analyze the performance of UTB SOI SRAM cells. Fig. 1 shows the log(Id)–Vg characteristics of five cases analyzed in this study. Case (A) uses midgap work function for N/PFET and shows higher $V_{\rm th}$ ($|V_{\rm th}| = 0.49$ V). Case (B), (C), (D), and (E) employ dual work functions for N/PFETs and show $|V_{\rm th}| = 0.39, 0.29, 0.19, 0.09$ V, respectively. For each case in Fig. 1, the absolute value of threshold voltages for NFET and PFET are the same. From case (A) to (E), the work function moves successively to the bandedge, and hence successively lower threshold voltage for the devices.

III. UTB SOI SRAM Cells for Ultralow Voltage Near Subthreshold Operation

A. Read Static Noise Margin

Fig. 2 shows the read static noise margin (RSNM) comparison between higher $V_{\rm th}$ (case A) and lower $V_{\rm th}$ (case B, C, D, and E) UTB SOI SRAM cells at $V_{\rm dd} = 0.4$ V. The inset of Fig. 2(a) shows the schematic of a 6T SRAM cell. The inset of Fig. 2(b) illustrates the static voltage transfer characteristics (VTC) during read/write operations. The RSNM is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell. $\rm V_{read,0}$ is the read disturb voltage determined by the voltage divider effect between pass-gate and pull-down transistors (NR). $V_{\rm trip}$ is the voltage needed to flip the cell inverter. $V_{\rm gain}$ is defined as the voltage when the slope of static VTC equals -1. Increase in $\rm V_{read,0}$, decrease in $V_{\rm trip}$, or decrease in $V_{\rm gain}$ will degrade the RSNM. $\rm V_{write,0}$ is determined by the voltage divider effect between pull-up PFET and pass-gate transistors. Lower $\rm V_{write,0}$ will benefit the write static noise margin (WSNM).

Fig. 2(a) shows that cases (A), (B), and (C) have comparable RSNM. Although the threshold voltages of cases (A), (B), and (C) are different, the threshold voltages of NFET and PFET in each case are balanced. Devices in cases (A), (B), and (C) with relatively higher threshold voltage are operating mostly in the subthreshold region through the switching period at $V_{\rm dd} = 0.4$ V. Fig. 2(b) shows that the $\rm V_{read,0}$ increases slightly in case (D) compared with case (A). $\rm V_{read,0}$ occurs with the $V_{\rm gs}$ of NR equals 0.4 V and the $V_{\rm gs}$ of pass-gate transistor equals (0.4 V-$\rm V_{read,0}$). Case (D) with quarter bandgap work functions has lower threshold voltage ($|V_{\rm th}| = 0.19$ V), the NR and pass-gate transistor operate in the super-threshold region at $V_{\rm gs} = 0.4$ V. The current (strength) ratio of the NR to the pass-gate transistor is thus lower in case (D) than in case (A), resulting in higher Vread,0. Fig. 2(b) also shows the $V_{\rm gain}$ is lower in case (E) than in case (A). $V_{\rm gain}$ can be seen to occur around VL = 0.17 V, where $V_{\rm gs}$ of NR equals 0.17 V and the $V_{\rm gs}$ of pull-up transistor (PR) equals -0.23 V. PFET in case (E) with near band-edge work function (lower threshold voltage = 0.09 V) operates in super-threshold region at $V_{\rm gs} = -0.23$ V. Hence, the current (strength) ratio of the PR to the NR is lower in case (E) than in case (A). Thus, $V_{\rm gain}$ decreases in case (E), squeezing RSNM. The $V_{\rm trip}$ is almost the same for all cases.

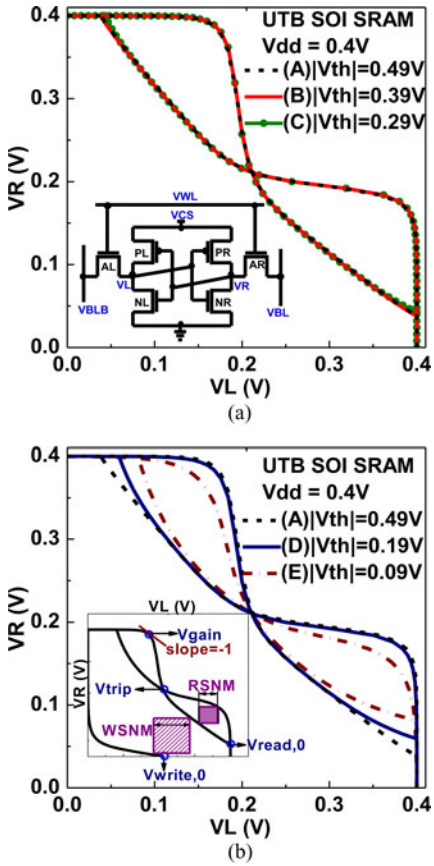


Fig. 2. Read static noise margin comparison between (a) case A, B, and C, (b) case A, D, and E. The inset of Fig. 2(b) shows the definition of RSNM, WSNM, $\rm V_{read,0}$, $\rm V_{trip}$, $\rm V_{gain}$, $\rm V_{write,0}$.

Fig. 3 shows the $V_{\rm gain}$, $V_{\rm trip}$, and $\rm V_{read,0}$ comparison at $V_{\rm dd} = 0.4$ V. As the NFET moves into the super-threshold region, $\rm V_{read,0}$ increases; as the PFET moves into super-threshold region, $V_{\rm gain}$ decreases. Fig. 4 shows the RSNM comparison with various $V_{\rm dd}$. At $V_{\rm dd} = 0.4$ V, transistors with $V_{\rm th} \sim 0.09$ V (case E) are prone to move into the super-threshold region. Therefore,

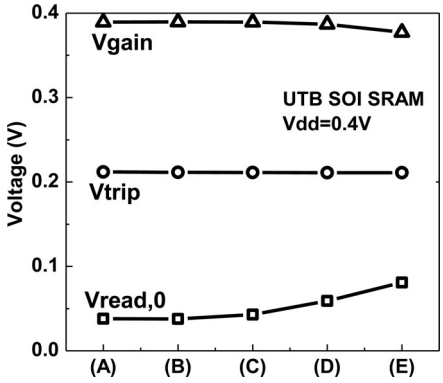


Fig. 3. V_{gain}, V_{trip}, and $V_{read,0}$ comparison of UTB SOI 6T SRAM cells using different threshold voltage designs.

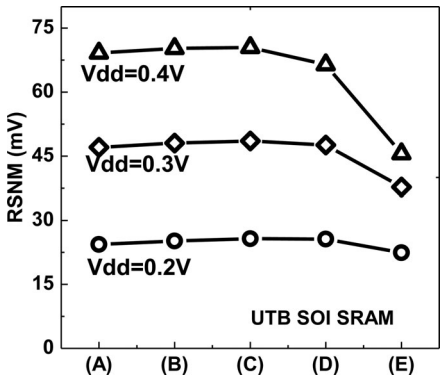


Fig. 4. RSNM comparison between UTB SOI 6T UTB SRAM cells using different threshold voltage designs with Vdd = 0.2, 0.3, 0.4 V.

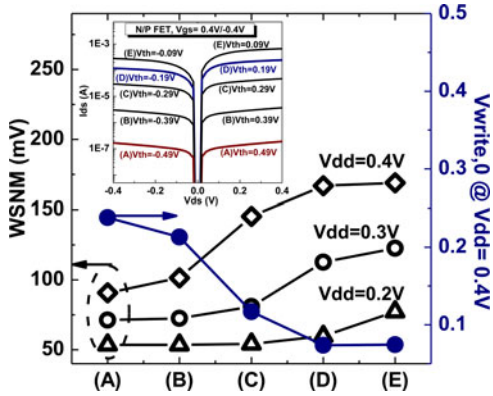


Fig. 5. WSNM comparison with Vdd = 0.2, 0.3, 0.4 V and $V_{write,0}$ comparison for Vdd = 0.4 V. Inset shows the log(Id)–Vd characteristics for N/PFET UTB SOI MOSFETs with several threshold voltages.

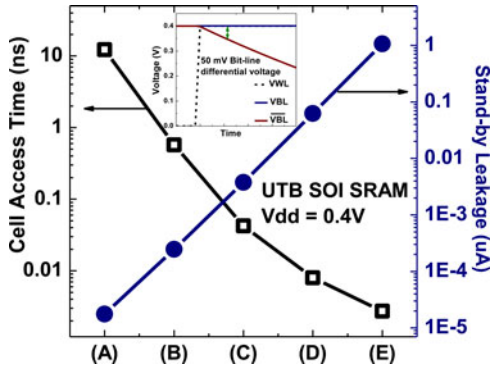


Fig. 6. "Cell" Read access time and stand-by leakage comparisons at Vdd = 0.4 V. Inset shows the definition of "cell" access time.

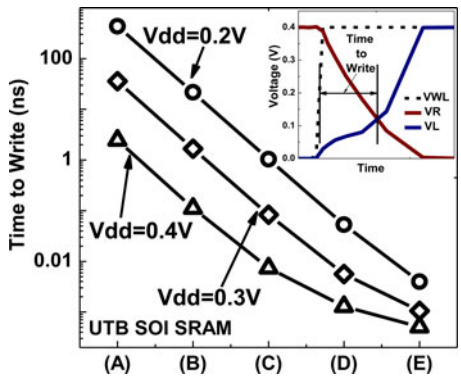


Fig. 7. Time-to-Write comparison at Vdd = 0.2, 0.3, 0.4 V. Inset shows the definition of time-to-write.

case (E) shows 35% decrease in RSNM as compared with case (A). At $V_{dd} = 0.2$ V, the RSNM difference between cases (A) and (E) is reduced because transistors operate mostly in the subthreshold region. Case (D) with $|V_{th}| = 0.19$ V (quarter band gap work functions) shows comparable RSNM to case (A) with $|V_{th}| = 0.49$ V (single midgap work function).

B. Write Static Noise Margin

$V_{write,0}$ (VL) occurs when the V_{gs} of pass-gate transistor (AL) is equal to 0.4 V (VBLB = 0 V, $V_R = 0$ V) and the V_{gs} of PL is equal to −0.4 V. The inset of Fig. 5 shows the log(Id)–Vd characteristics for N/PFET UTB SOI MOSFET with various threshold votlages. With balanced N/PFET ($|V_{th}|$ the same for N/PFET), NFET is stronger than PFET in the super-threshold region as compared with that in the subthreshold region (see Fig. 5 inset). This is because compared with $(V_{gs} - V_{th})$, the contribution of mobility to drain current is more significant in the super-threshold region than in the subthreshold region. $V_{gs} - V_{th}$ contributes to current in the exponential term which influences the subthreshold current more significantly than mobility. The lower mobility in PFET leads to weaker PFET (compared with NFET) in the super-threshold region. Fig. 7(b) shows that case (E) with weaker PL has lower $V_{write,0}$ and shows 84% improvement in WSNM compared with case (A) at $V_{dd} = 0.4$ V. As V_{dd} decreases, the difference in WSNM from case (A) to case (E) becomes smaller because transistors operate mostly in the subthreshold region.

C. "Cell" Read Access Time

"Cell" read access time and time-to-write are analyzed by connecting a column of 64 UTB SOI 6T SRAM cells (64 cells

per bit line). A capacitive load is added onto each bit line to account for the capacitance of wires and the connected devices. The bit-line length and capacitance are calculated based on the actual layout of a 65-nm 6T SRAM cell. Fig. 6 shows the "cell" read access time and standby leakage comparisons for UTB SOI SRAM cells near the subthreshold region. The "cell" read access time is defined as the time required for developing 50 mV bit-line differential voltage after the word-line is activated during a read operation. The "cell" read access time depends on the value of the read current through the pass-gate and NR. As $V_{\rm th}$s are lowered (from case A to case E), the "cell" access time improves significantly with correspondingly higher standby leakage, thus trading off standby leakage with performance. Case (D) with quarter band gap work function and lower (yet adequate) threshold voltage has higher drain current and shows around three orders of magnitude lower "cell" read access time and higher standby leakage than case (A). Case (E), with $|V_{\rm th}| = 0.09$ V (near bandedge work function), has lowest "cell" read access time. However, it suffers severe RSNM degradation as shown in Fig. 4.

D. Time-to-Write

For write operation, the "cell" write time is defined as the time from the 50% activation of the word-line to the time when the voltages of two cell storage nodes cross each other (see the inset in Fig. 7). Fig. 7 shows the time-to-write comparison for UTB SOI SRAM cells near the subthreshold region. UTB SOI SRAM with lower $V_{\rm th}$ devices (case D, |Vth| = 0.19 V) shows much lower time-to-write than case (A).

E. Cell Leakage

UTB SOI MOSFET, due to its better short-channel effects, lower subthreshold swing, and reduced RDF, significantly reduces the leakage compared with Bulk CMOS devices. Fig. 8(a) shows the worst case bit-line cell data pattern for read operation. All unselected cells (enclosed by dotted lines) have stored logic value opposite to that of the selected cell (enclosed by dashed line). The leakage through pass-gate transistors of the unselected cells rivals the read current of the selected cell to charge up the low-going bit line, while discharge the bit line which is supposed to be held at "high." Thus, the bit-line differential voltage is reduced, resulting in the degradation of sensing margin and speed. Fig. 8(b) and (c) shows the bit-line voltage versus sensing time with various number of cells per bit-line for case (D) (solid line), (C) (dash line), and (A) (dot line) at $V_{\rm dd} = 0.4$ V. For case (D) with $|V_{\rm th}| = 0.19$ V, the bit-line voltage difference can be seen to develop significantly faster than case (C) and case (A). Although case (D) has larger bit-line leakage than case (A), case (D) can still support adequately large number of cells per bit-line (e.g., 256 cells per bit-line) due to its larger read current and the well controlled short-channel effects and superior leakage of UTB SOI MOSFETs. The real density constraint comes from the overall leakage and power for the intended subthreshold applications.

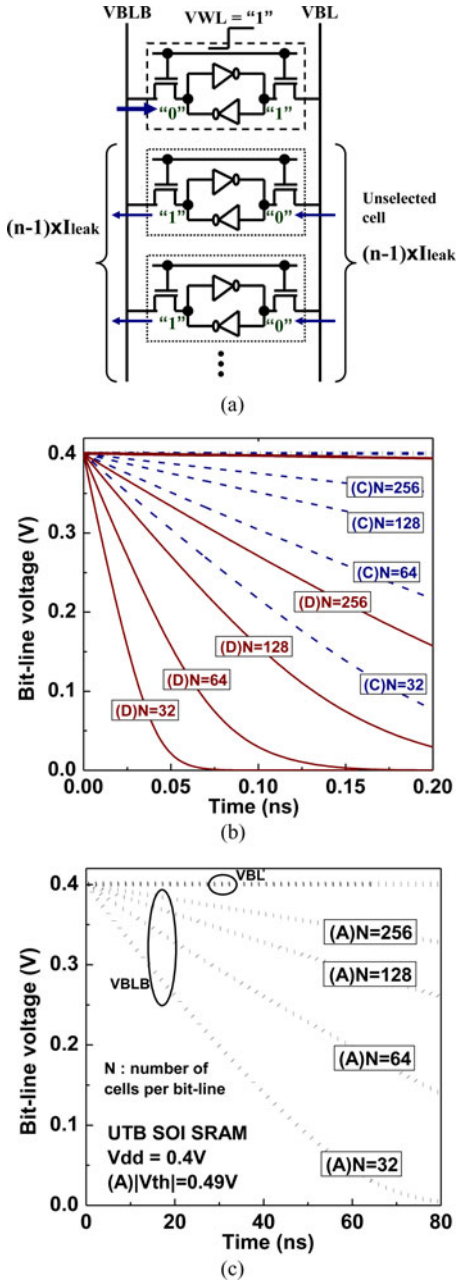
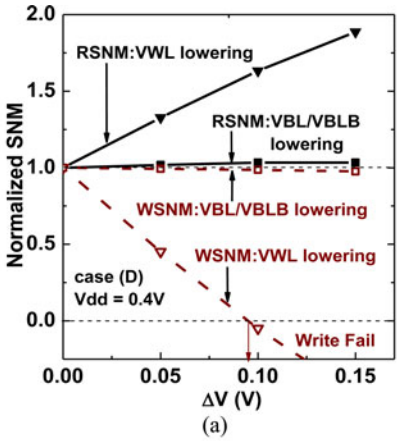


Fig. 8. (a) Worst case bit-line cell data pattern for Read operation. (b) Bit-line voltage versus sensing time with various number of cells per bit-line for case (D) (solid line), case (C) (dash line), and case (A) (dot line) at Vdd = 0.4 V. N is the number of cells per bit-line. (c) Bit-line voltage versus sensing time for case (A) (dot line) in expanded time scale at Vdd = 0.4 V.

IV. Circuit Techniques for Stability and Leakage Improvement

Section III demonstrates that using the lower $V_{\rm th}$ devices (case D, $|V_{\rm th}| = 0.19$ V) significantly improves the WSNM and offer higher performance while trading off leakage for the subthreshold SRAM applications. This section evaluates the effectiveness of commonly used circuit techniques, such as word-line voltage lowering [22], bit-line precharge voltage lowering [17], and negative bit-line voltage [18]–[20], [23], [24], for improving the stability, standby leakage, and write ability of



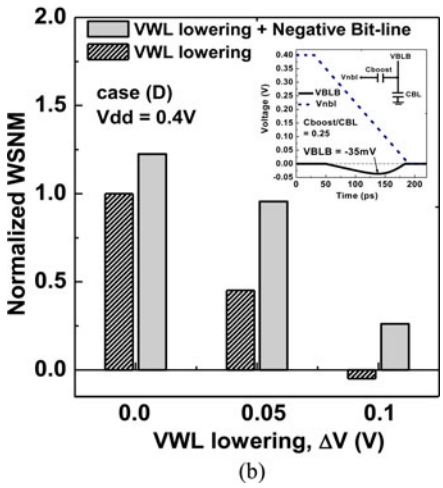


Fig. 9. (a) Impact of word-line voltage lowering (VWL = Vdd – ΔV) and bit-line precharge voltage lowering (VBL/VBLB = Vdd–ΔV) on the RSNM/WSNM, respectively. (b) Impact of the word-line voltage lowering on the normalized WSNM with and without using negative bit-line voltage technique, respectively. Inset shows the negative bit-line voltage is −35mV.

the UTB SOI ultralow voltage SRAM cell with lower $V_{\rm th}$ devices (case D). Fig. 9(a) shows the impact of word-line voltage lowering and bit-line precharge voltage lowering on the normalized RSNM/WSNM, respectively. Lowering the word-line voltage reduces the strength of pass-gate transistors, thus improving RSNM and degrading WSNM. Lowering bit-line precharge voltage reduces the read-disturb voltage ($V_{\rm read}$, 0), hence improving RSNM. On the other hand, during write operation, the bit-line that is supposed to stay at "high" is held at lower voltage level, thus degrading the push–pull write effect and WSNM. For the subthreshold SRAM operation, lowering word-line voltage shows larger improvement in RSNM than lowering bit-line precharge voltage. RSNM improves by 33% as VWL is lowered by 50 mV (ΔV = 0.05 V). However, the word-line voltage lowering also significantly degrades WSNM. The degraded WSNM can be mitigated using negative bit-line (NBL) technique [18]–[20] where a capacitively coupled transient negative pulse is introduced into the low-going bit line to facilitate write operation. Fig. 9(b) illustrates that using word-line voltage lowering (ΔV = 0.05 V) and negative bit-line voltage (VBLB = –35 mV) show comparable WSNM

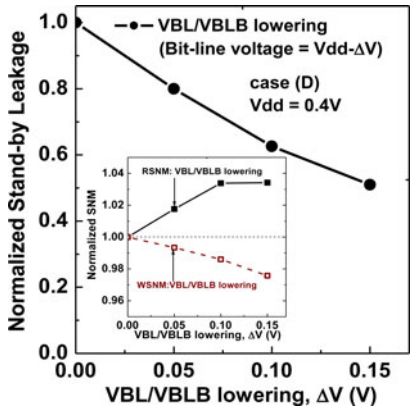


Fig. 10. Impact of bit-line precharge voltage lowering on the normalized standby leakage. Inset shows the impact of bit-line precharge voltage lowering on the normalized RSNM/WSNM.

as compared with the case without word-line voltage lowering (ΔV = 0 V). In other words, using negative bit-line voltage in the write operation can compensate for the WSNM degradation due to word-line voltage lowering. Fig. 10 shows the impact of bit-line precharge voltage lowering on the standby leakage. As the bit-line precharge voltage is lowered by 50 mV (ΔV = 0.05 V), the standby leakage is reduced by 20%. Therefore, using lower $V_{\rm th}$ devices (case D) with word-line voltage lowering, bit-line precharge voltage lowering, and negative bit-line voltage can enhance RSNM, reduce standby leakage, and improve WSNM and write ability of UTB SOI SRAMs for ultralow voltage near subthreshold opeartion.

V. Variability of RSNM/WSNM Comparison

Fig. 11 shows the RSNM/WSNM characteristics for case (A) and case (D) 6T UTB SOI SRAM cells considering line-edge-roughness (LER) at $V_{\rm dd}$ = 0.4 V. For the lightly doped UTB SOI MOSFETs we used in this study (gate length = 40 nm, channel thickness = 10 nm), gate LER is the dominate variation source [25]. To assess the LER in UTB SOI MOSFETs, the line edge patterns were derived using the Fourier synthesis approach [21] with correlation length = 20 nm and rms amplitude = 1.5 nm. Monte Carlo simulations with 150 samples were performed for each case. The insets in Fig. 11(a) and (b) are the log(Id)–Vg characteristics considering LER for case (A) and case (D), respectively. As can be seen, case (D) shows smaller drain current variation as its operation region moves slightly into the super-threshold region. Thus, case (D) shows smaller variation in RSNM and WSNM. Fig. 12 shows the RSNM and WSNM variability comparison between case (A) and case (D). For read operation, case (D) with smaller $V_{\rm th}$ shows 41% improvement in σRSNM and comparable mean of RSNM as compared with case (A) [see Fig. 12(a)]. For Write operation, case (D) shows 67% improvement in σWSNM and 84% improvement in the mean of WSNM as compared with case (A) [seeFig. 12(b)].

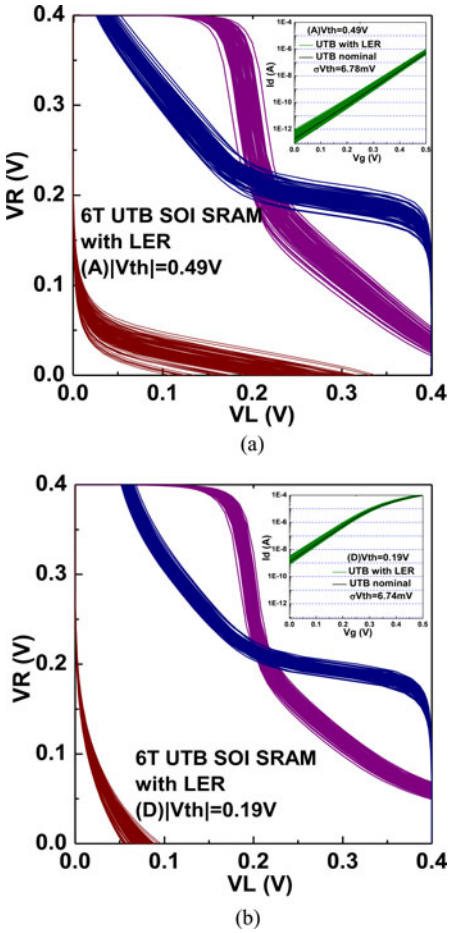


Fig. 11. RSNM/WSNM characteristics consider line-edge-roughness for (a) case A (|Vth| = 0.49 V) and (b) case D (|Vth| = 0.19 V). Inset shows the log(Id)–Vg characteristics for case A and D considering LER. (Correlation length = 20 nm, Rms amplitude = 1.5 nm).

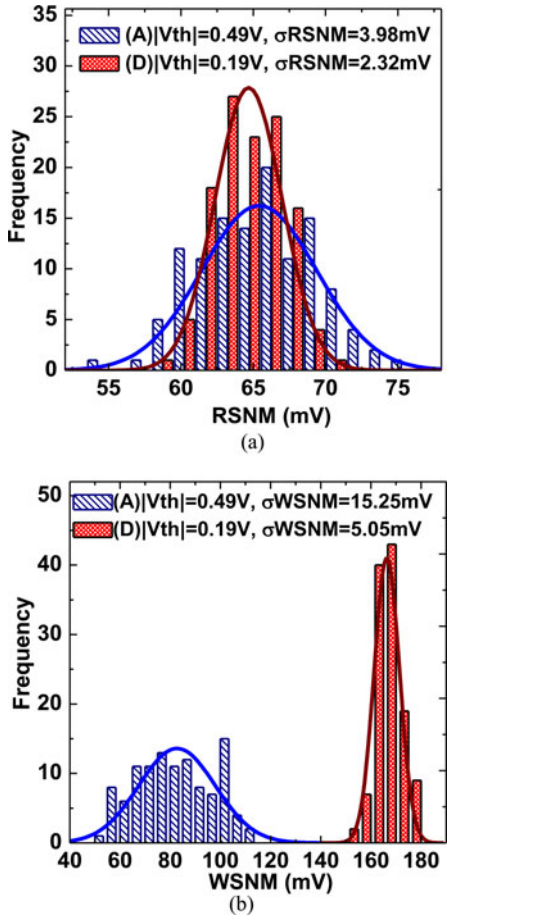


Fig. 12. (a)RSNM variability (σRSNM considering LER) comparison between case (A) and (D). (b) WSNM variability (σWSNM considering LER) comparison between case (A) and (D). Case (D) shows smaller variation due to its operation region slightly getting into the super-threshold region.

VI. Conclusion

We have investigated the impact of threshold voltage design on the stability, margin, performance, and variability of UTB SOI 6T SRAM cells operating near the subthreshold region. Our results indicated that UTB SOI 6T SRAM cell using lower $V_{\rm th}$ devices ($|V_{\rm th}| = 0.19$ V, $V_{\rm dd} = 0.4$ V) showed comparable RSNM, 84% improvement in WSNM, and significant improvement in variability (σRSNM, σWSNM) as compared with that using the higher $V_{\rm th}$ devices ($|V_{\rm th}| = 0.49$ V, $V_{\rm dd} = 0.4$ V). For the UTB SOI 6T SRAM cells using lower $V_{\rm th}$ devices, the "cell" access time improved significantly with correspondingly higher standby leakage. Lowering word-line voltage by 50 mV resulted in 33% improvement in RSNM while degrading WSNM simultaneously. Using NBL voltage in the write operation could compensate for the WSNM degradation due to word-line voltage lowering. Lowering bit-line precharge voltage by 50 mV reduced the standby leakage by 20%. Our study suggest that the lower $V_{\rm th}$ UTB SOI devices not only support the high performance applications but also offer higher performance and improve the stability/variability for ultralow voltage near subthreshold SRAM applications.

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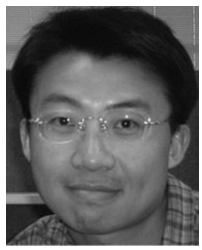

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