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Polycrystalline silicon thin-film transistor utilizing self-assembled monolayer for crystallization

Yosuke Tojo [a], Atsushi Miura [a,b], Yasuaki Ishikawa [a,c,*], Ichiro Yamashita [a,c,d], Yukiharu Uraoka [a,c]

[a] Graduate School of Materials Science, Nara Institute of Science and Technology, 8916-5 Takayama, Ikoma, Nara 630-0192, Japan
[b] The Department of Applied Chemistry and Institute of Molecular Science, National Chiao Tung University, 1001 TaHsueh Road, Hsinchu 30010, Taiwan
[c] CREST, 4-1-8, Honcho, Kawaguchi, Saitama 332-0012, Japan
[d] Panasonic Co., 3-4 Hikaridai, Seika, Kyoto 619-0237, Japan

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ABSTRACT

Crystallization employing an N-(2-aminoethyl)-3-aminopropyltrimethoxysilane self-assembled monolayer (AEAPS-SAM) to coordinate Ni metal catalyst was found to produce large grain poly-Si. A small concentration of Ni could be deposited controllably onto an AEAPS-SAM covered with Si by immersing it in Ni solution for 1–60 min. Larger grains and a lower Ni concentration in the poly-Si could be obtained by shorter immersion. Immersion for 1 min produced grains, as large as 47 μm and a Ni concentration as low as 7.4×10^{18} atoms/cm^3. A poly-Si thin-film transistor fabricated with AEAPS-SAM poly-Si of 1 min immersion had a field-effect mobility of 98 cm^2/(V s), which is one order of magnitude higher than that of a thin-film transistor fabricated without the AEAPS-SAM treatment.

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1. Introduction

In this paper, we present a crystallization method for decreasing leakage current in polycrystalline silicon (poly-Si) thin-film transistors (TFTs) by employing nickel (Ni)-induced crystallization, a technique that can be used as an alternative to excimer laser annealing. Poly-Si films with sufficiently high electrical and crystallographical quality are critical for achieving high-performance TFTs. Metal-induced crystallization is a method utilizing a silicide as a metal catalyst to produce poly-Si thin films with large grains [1]. To induce the crystallization, Ni is widely used because the lattice constant of Ni silicide is only slightly different from that of crystalline Si (c-Si) [2]. However, excess Ni atoms behave as an impurity in a poly-Si thin film, and increase the off-state leakage current of TFTs [3]. To solve this problem, the introduction of a silicon-nitride (SiN_x) layer as a Ni diffusion barrier [1] and the utilization of a cage-shaped supramolecular protein have been proposed [4,5]. In the case of using a SiN_x layer, the SiN_x and NiO layers must be removed before the TFT is fabricated. When using a cage-shaped supramolecular protein, Ni nanoparticles must be formed within the vacant cavity by biomineralization. In this study, a self-assembled monolayer (SAM) was employed to achieve efficient and simple Ni adsorption and to avoid the use of a complicated process. SAMs are widely used for the functionalization of solid substrate surfaces [6–9]. An N-(2-aminoethyl)-3-aminopropyltrimethoxysilane (AEAPS)-SAM can bind to metal ions via the terminal ethylenediamine ligand and form a homogeneous metal-coordinated monolayer [10–12]. Previous reports suggest that the use of an AEAPS-SAM can markedly decrease the amount of Ni catalyst needed while maintaining a sufficient amount to induce crystallization. In this study, we report an original crystallization process using AEAPS-SAM to prepare poly-Si thin films. A small amount of Ni, used as a metal catalyst to induce the formation of crystalline nuclei, was adsorbed on amorphous silicon (a-Si) by AEAPS-SAM, yielding a poly-Si thin film with low metal impurity concentration. This process does not require complicated and expensive equipment such as a high-vacuum system, and is suitable for large substrates.

2. Experimental details

A small amount of Ni was adsorbed on an a-Si film via the terminal ethylenediamine ligand of an AEAPS-SAM as shown in Fig. 1(a). This process results in a very low concentration of Ni in the poly-Si thin film after crystallization. However, there is sufficient Ni to act as a catalyst for metal-induced lateral crystallization (MILC) [13], enabling the growth of poly-Si thin films.

The crystallization process is shown in Fig. 1(b). A 50-nm-thick a-Si thin film deposited by low-pressure chemical vapor deposition (CVD) was irradiated by ultraviolet (UV) in an ozone atmosphere at 110 °C for 10 min to render the surface hydrophilic. An a-Si thin film and

* Corresponding author at: 8916-5 Takayama, Ikoma, Nara 630-0192, Japan. Tel.: +81 743 72 6061; fax: +81 743 72 6069.
E-mail address: yishikawa@ms.naist.jp (Y. Ishikawa).

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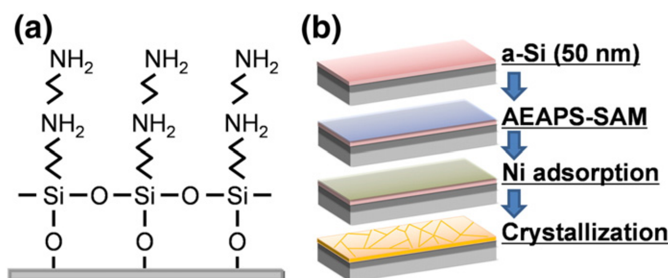

Fig. 1. Crystallization process: (a) AEAPS-SAM on amorphous Si (a-Si) surface and (b) schematic drawing of the steps in this process.

AEAPS solution were placed in a closed container, and an AEAPS-SAM was formed on the a-Si thin film at 100 °C over 1 h by thermal CVD. Next, the a-Si thin film with the AEAPS-SAM was immersed in a 3 mM Ni acetate solution ($Ni(CH_3COOH)_2$) at room temperature between 1 min and 60 min, and Ni was adsorbed on the a-Si surface by the AEAPS-SAM. Subsequent UV irradiation in ozone atmosphere at 110 °C for 1 h was carried out to remove the AEAPS-SAM, leaving the Ni behind. Finally, the Ni-containing a-Si thin films were annealed at 550 °C for 24 h to induce crystallization. To fabricate top-gate poly-Si TFTs, a gate insulator of 100-nm-thick silicon dioxide (SiO_2) was then deposited by plasma enhanced CVD. Phosphorous implantation was performed to the source and drain region with the energy of 90 keV at a dose of 1.2×10^{15} cm^{-2}, and dopant activation was carried out at 600 °C for 2 h. For source and drain electrodes, a 300-nm-thick titanium layer was deposited by RF sputtering. Channel width and length were 10 μm and 5 μm ($W/L = 10$ μm/5 μm), respectively. The characteristics of the TFTs were measured in the dark at room temperature using a precision semiconductor parameter analyzer (Agilent 4156C).

X-ray photoelectron spectroscopy (XPS, SHIMADZU, KRATOS AXIS-165) was performed to confirm the existence of AEAPS-SAM and metal adsorption. The sputtering ion beam species, beam energy, and beam current density were Al Kα, 80 eV, and 10 mA, respectively. Carbon (C), nitrogen (N), and nickel (Ni) were measured. It has been reported that C1s, N1s, and Ni2p3/2 peak were detected at 284.5 eV, 398.1 eV, and 852.7 eV, respectively [14]. The background was eliminated by Shirley method. Grain observation of the poly-Si was carried out by scanning electron microscope (SEM, JEOL, JSM-7400 F). The operating voltage was 3.0 kV. Crystallinity of the poly-Si was analyzed by Raman spectroscopy (JASCO, NRS-2100). The laser intensity, exposure time, and cumulative number were 10 mW, 5 s, and 2 times, respectively.

3. Results and discussion

3.1. Surface analyses

At first, we investigated the metal-ligand coordination of the Ni, C, and N on the a-Si film with the AEAPS-SAM. Fig. 2 shows XPS spectra of these elements after each process. The intensity of all these peaks is very weak, indicating a low amount of adsorption of each atom during the formation and coordination of the AEAPS-SAM. As can be seen in the XPS spectra of C1s [Fig. 2(a)] and N1s [Fig. 2(b)], the intensities of the peaks at 284.5 (C1s) and 398.1 (N1s) eV increased as a result of AEAPS-SAM formation, then decreased to almost the same level as those of the clean a-Si substrate after UV ozone treatment, suggesting that the AEAPS-SAM was completely removed by the UV ozone treatment. Meanwhile, the peak intensity of $Ni2p_{3/2}$ [Fig. 2(c)] increased after the a-Si film was immersed in Ni acetate solution ($Ni(CH_3COO)_2 = 3$ mM) for 20 min, and Ni remained after the UV ozone treatment. When a-Si thin film without the AEAPS-SAM was immersed in a Ni acetate solution, the $Ni2p_{3/2}$ peak was absent, as shown in Fig. 2(d), indicating that Ni was indeed captured on

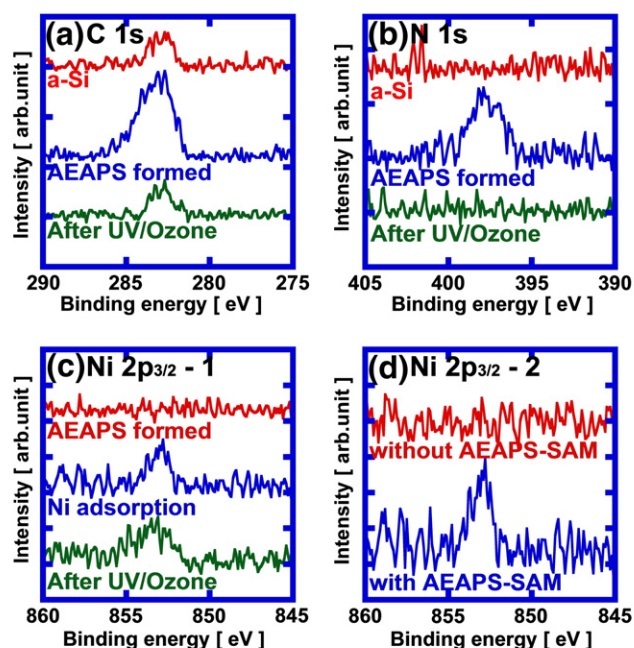

Fig. 2. XPS spectra: (a) C1s, (b) N1s to confirm AEAPS elimination, (c) Ni2p3/2 after each experimental process, and (d) Ni2p3/2 with and without AEAPS-SAM.

the a-Si surface by binding to the AEAPS-SAM. After UV ozone treatment, the $Ni2p_{3/2}$ peak shifted slightly, and broadened implying that the Ni silicide, which exhibits a peak at 853.3 eV [14], was formed as a result of the UV ozone treatment. These results reveal that the UV ozone treatment can remove unnecessary C and N, which act as impurities, and that a small amount of Ni is present on the a-Si surface in the form of Ni silicide after AEAPS-SAM elimination.

3.2. Crystallization

The Ni-containing a-Si thin films were annealed at 550 °C for 24 h to induce crystallization. The grain boundaries were etched by a Secco etch [15] to increase their contrast in SEM observation. For comparison, an annealed Si thin film made from an a-Si thin film without AEAPS-SAM was also prepared. The crystallinities of the Si thin film with and without AEAPS-SAM formation were compared using Raman spectroscopy. Fig. 3 shows SEM images of the grain morphology and Raman spectra of the annealed Si films after immersion in Ni acetate solution for 20 min. The Raman spectrum of the a-Si thin film has a broad maximum, as shown in Fig. 3(a), that is absent after annealing as shown in Fig. 3(b) and (c), indicating its transformation into c-Si. The annealed Si thin film using AEAPS-SAM had an average grain size of about 17.5 μm [Fig. 3(c)]. In addition, the symmetric peak at 520 cm^{-1} of the c-Si [16], was only observed in annealed Si thin film formed using the AEAPS-SAM. On the other hand, no grains could be seen in the SEM in Secco etched films without AEAPS-SAM [Fig. 3(b)]. The asymmetric Raman peak at 520 cm^{-1} of the annealed Si thin film without AEAPS-SAM can be decomposed into two peaks centered at 500 cm^{-1} and 520 cm^{-1}. The peak at 500 cm^{-1} is assigned to nanocrystalline Si (nc-Si) [17], indicating the existence of nanometer-scale grains in the poly-Si thin film formed without the AEAPS-SAM. The crystallization process without the AEAPS-SAM was very similar to conventional solid-phase crystallization without a metal catalyst. According to these results, poly-Si thin films with large crystal grains were formed by the capture of Ni on the a-Si surface by our process.

The average grain diameter and Ni concentration of crystallized Si thin films as a function of immersion time were measured by SEM and secondary ion mass spectrometry, respectively. As seen in Fig. 4, the average grain diameter increases from 4.6 μm to 43 μm as the immersion

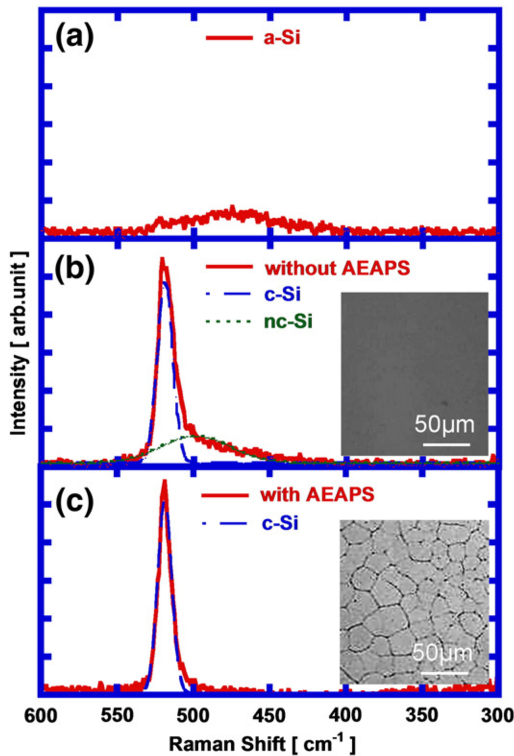

Fig. 3. Raman spectra and grain images of crystallized layer: (a) before crystallization, (b) after crystallization with and (c) without the use of AEAPS-SAM (Ni concentration = 3 mM, immersion time = 20 min, annealing conditions = 550oC for 24 h). Literature as references for amorphous Si (a-Si), crystalline Si (c-Si), and nanocrystalline Si (nc-Si) are Refs. [17,16] and [17], respectively.

time is reduced from 60 min to 1 min, concomitant with a fall in Ni concentration from 1.03×10^{19} atoms/cm^3 to 7.3×10^{18} atoms/cm^3.

During AEAPS-SAM formation, AEAPS molecules bind to hydroxyl groups on the SiO_2 surface and to neighboring AEAPS molecules via the dehydration reaction shown in Fig. 1(a) [18]. Therefore, it is estimated that the density of ethylenediamine is equal to the OH density at the surface of a-Si. In order to estimate the amount of Ni atoms, we utilized 2.5 to 3.4 OH/nm^2, which was estimated from the flame made silica powder [19], since this value is the highest

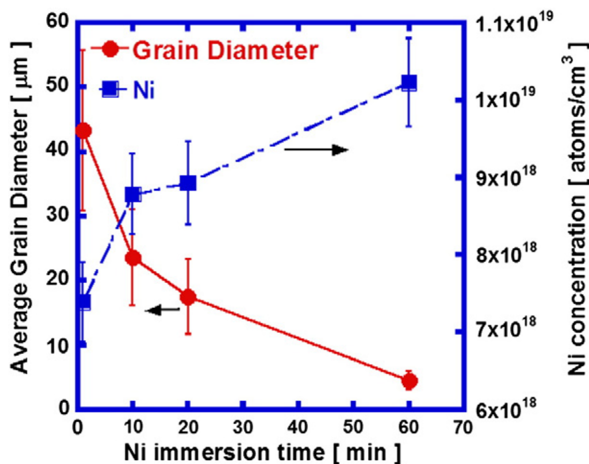

Fig. 4. Ni immersion time dependence of average grain diameter and Ni concentration in Si layer (Ni concentration = 3 mM, immersion time = 1, 10, 20, and 60 min).

value in various reports. Ni atoms in silicon film behave as contamination, and the large amount of Ni is detrimental for electrical characteristics of the fabricated silicon films. Furthermore, when a Ni complex is formed by using ethylenediamine, one Ni atom is captured by two or three terminal of ethylenediamine ligands [20,21], and hence the estimated maximum concentration of Ni on the surface is 1.1 to 1.7 Ni/nm^2. The Ni concentration in the 50-nm-thick silicon layer is estimated to be 2.2–3.4 $\times 10^{19}$ atoms/cm^3. The experimental value of Ni concentration shown in Fig. 4 ranges between 7.3×10^{18} to 1.03×10^{19} atoms/cm^3. It implies that the OH density at the surface of a-Si film after AEAPS-SAM formation is less than one third of that of the flame made silica powder. Note that the estimated value is much lower than that of the conventional MILC method [1].

Fig. 4 also indicates that the grain diameter can be increased up to about 47 μm by decreasing the amount of Ni adsorption by shorting the Ni immersion time, resulting in the formation of poly-Si with larger grains with Ni concentration less than 10^{19} cm^{-3} orders. However, Ni immersion shorter than 1 min was found not to yield crystal grains such as those shown in Fig. 3(c), indicating insufficient Ni adsorption to promote MILC. Therefore, to create poly-Si thin films with large grains over the entire substrate area, we subsequently performed a 1 min Ni immersion, to fabricate poly-Si TFTs. In addition to these TFTs, we fabricated poly-Si TFTs using the same Ni immersion time but without employing the APEAPS-SAM coating.

3.3. TFT performances

Fig. 5 shows drain current (I_d) versus drain voltage (V_d) for both TFTs types for $W/L = 10$ μm/5 μm as a function of gate bias (V_g). I_d for both types increased with V_d. However, the value of I_d for AEAPS-SAM TFTs (Fig. 5(b)) at $V_g = 1$ V exceeds that of the TFT without the AEAPS-SAM by about an order of magnitude at the same V_g, and at $V_g = 4$ V by about two orders of magnitude. Fig. 6 shows I_d vs. V_g at $V_d = 0.1$ V of the three highest performing devices of both types. The distribution of the transfer characteristics is typical for both processes. Note that the on-current of the poly-Si TFTs using AEAPS-SAM exceeds that of TFTs without the AEAPS-SAM by two to three orders of magnitude while the leakage current is similar, about 10^{-12} A. The average device characteristics of both types of TFT are listed in Table 1 with their distribution estimated from six TFTs, respectively. We confirmed that a similar trend was obtained for device performance and their distribution, in three samples, in each case. The AEAPS-SAM-utilized poly-Si TFTs had a threshold voltage of 4.8 V compared to 18.5 V for TFTs without AEAPS-SAM treatment, a subthreshold slope of 1.2 V/dec compared to 2.4 V/dec, and an on/off ratio of 1×10^7 as compared to 10^6. In addition, the highest field effect mobility (μ_{FE}) of 104.8 cm^2/(V s) was recorded at $V_d = 0.1$ V. The better performance is due to the larger grain size and improved crystallinity. On the other hand, the lowest μ_{FE} of the AEAPS-SAM-utilized poly-Si TFT was 49.5 cm^2/(V s) while that without AEAPS-SAM was only 6.1 cm^2/(V s), since the channel region of the poly-Si TFT without AEAPS-SAM treatment has a lot of grain boundaries.

We presume that the three best devices with AEAPS-SAM treatment depicted in Fig. 6(b) had no grain boundary in the channel region, and TFT with low mobility have one or more grain boundaries. In addition, it is known that the area of a crystalline nucleus has a high contamination of Ni [22]. This implies that the small scattering of device characteristics in the three best devices was affected by metal contamination in the channel region originated from the crystalline nucleus site, since the excess metal impurity increases the off-current [3]. However we see no large difference in the off-current between the poly-Si TFTs with and without the AEAPS-SAM process. In addition, this process can easily be applied to larger substrates since the main step is just dipping. This proposed process is a promising method to provide high-quality poly-Si thin films with large grains for industrial production.

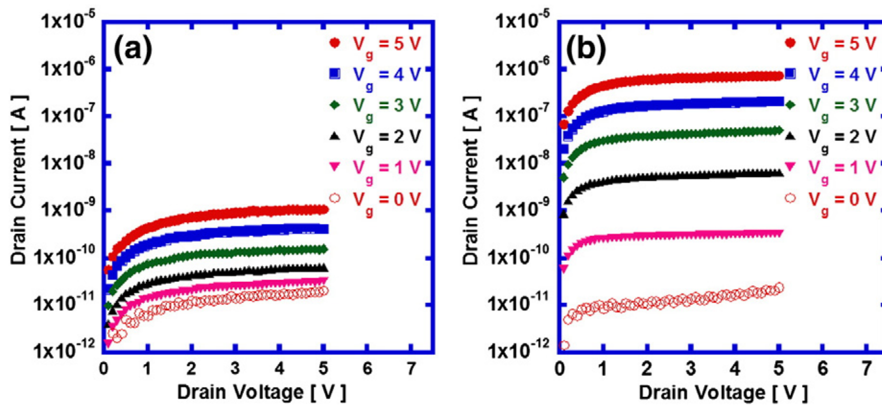

Fig. 5. Output characteristics of poly-Si TFTs (a) without and (b) with AEAPS-SAM process at *Vg*, and *Vd* = 0 to 5 V; channel width/length = 10 μm/5 μm, Ni concentration = 3 mM, immersion time = 1 min.

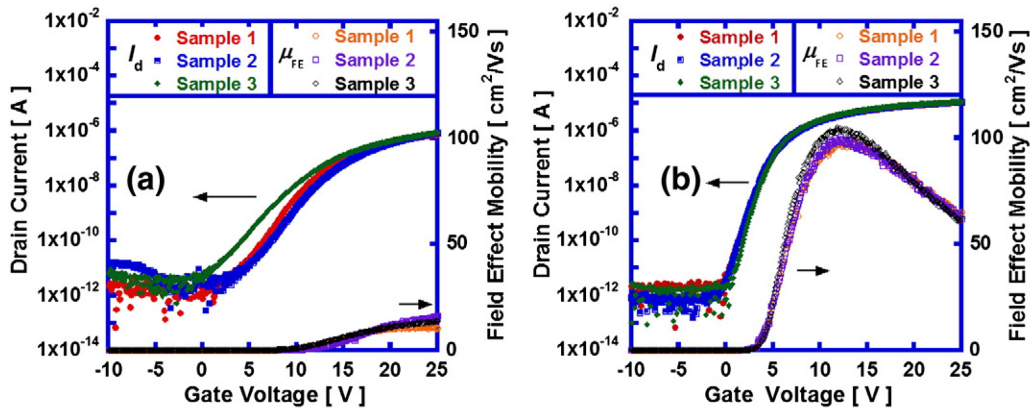

Fig. 6. Transfer characteristics of poly-Si TFTs (a) without and (b) with AEAPS-SAM process at *Vd* = 0.1 V; channel width/length = 10 μm/5 μm, Ni concentration = 3 mM, immersion time = 1 min.

4. Conclusions

We investigated an original crystallization process using the binding of Ni ions to an AEAPS-SAM. This process provides sufficient Ni to promote the MILC process, but results in very low metal contamination of the formed poly-Si layer. We confirmed that the organic components of the SAM can be removed by a UV ozone treatment, leaving Ni nuclei behind. The average grain diameter was controllable by adjusting the Ni immersion time, and crystalline grain as large as 47 μm was formed. The very low amount of metallic impurity compared to that of conventional Ni crystallization processes resulted in improved device characteristics. We conclude that our crystallization process is a promising method for the realization of high-performance TFTs on large substrates.

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Table 1
Average device characteristics of poly-Si TFTs with and without utilization of AEAPS-SAM at *Vd* = 0.1 V. The error value indicates the standard deviation value.

	Threshold voltage [V]	Subthreshold slope [V/dec]	On/off ratio	μFE [cm2/(V × s)]			Number of samples
				Average	Max.	Min.	
Without AEAPS-SAM (solid-phase crystallization)	18.5 ± 3.2	2.4 ± 0.2	1.1×10^6	14.0	18.1	6.1	6
With AEAPS-SAM	4.8 ± 1.2	1.2 ± 0.2	1.0×10^7	67.9	104.8	49.5	6

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