High-κ Eu_2O_3 and Y_2O_3 Poly-Si Thin-Film Transistor Nonvolatile Memory Devices

Tung-Ming Pan, Li-Chen Yen, Sheng-Hao Huang, Chieh-Ting Lo, and Tien-Sheng Chao

***Abstract*— In this paper, we have successfully fabricated low-temperature polycrystalline silicon thin-film transistor (LTPS-TFT) nonvolatile memory devices employing high-κ Eu_2O_3 and Y_2O_3 films as the charge trapping layer. The LTPS-TFT memory device uses band-to-band tunneling-induced hot hole injection and gate Fowler–Nordheim injection as the program and erase methods, respectively. Compared with the Y_2O_3 film, the LTPS-TFT memory device using an Eu_2O_3 charge-trapping layer exhibited a lower subthreshold swing and a larger memory window, a smaller charge loss, and a better endurance performance, presumably because of the higher charge-trapping efficiency of the Eu_2O_3 film.**

***Index Terms*— Charge-trapping layer, Eu_2O_3, low-temperature polycrystalline silicon thin-film transistor (LTPS-TFT), Y_2O_3.**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon thin-film transistors (LTPS-TFTs) are extensively employed to integrate driver circuits for active-matrix liquid crystal displays and active-matrix organic light-emitting-diode displays because of their high field-effect mobility and driving current [1], [2]. In addition, the improvement in LTPS-TFT performance can enable various functional devices, such as logic, memory, and controller, to be integrated into the 3-D circuits or multilayer Si ICs for the applications of system-on-chip (SOC) and system-on-panel (SOP) on a glass panel [3]–[7]. The low power consumption is an essential requirement for SOC and SOP applications. The nonvolatile memory is widely utilized for data storage in portable electronic systems because of its low power consumption and nonvolatility. Silicon-oxide-nitride-oxide-silicon (SONOS)-type charge trapping memory devices is widely used in nonvolatile memories because of their advantages such as high program/erase (P/E) speed, low programing voltage and power consumption, good endurance, and high density integration [8], [9]. The SONOS-type memory may be a promising candidate for SOP application because of its full process compatibility. However, the conventional charge-trapping memory device has the issues surrounding the tradeoff between erasing speed and the data retention. When the tunneling oxide is thin, the P/E process become faster but a charge leakage degrades the data retention. High-κ materials, including HfO_2 [9], [10], ZrO_2 [11], and Y_2O_3 [12], are being considered as charge storage materials to improve P/E speed and data retention performance. This improvement is attributed to the higher trap density and the larger bandgap offset between the high-κ material and the tunnel oxide layer [13].

Rare-earth (RE) oxide materials, such as Pr_2O_3 [14] and Tb_2O_3 [15], are recently investigated as gate dielectrics for applications in LTPS-TFTs because of their high permittivity, large energy bandgap, and high thermodynamic stability with poly-Si. However, the application of RE oxide materials as charge trapping layers in LTPS-TFT memory devices is not reported. Among the RE oxide films, europium oxide (Eu_2O_3) film can be considered as a charge trapping layer because of its large dielectric constant (~ 15) and wide bandgap energy (~ 4.5 eV) [16]. In this paper, we developled new SONOS-type LTPS-TFT nonvolatile memory devices using Eu_2O_3 and Y_2O_3 charge trapping layers.

II. Experimental Setup

The Eu_2O_3 and Y_2O_3 LTPS-TFT nonvolatile memory devices are fabricated from 6-in Si substrates in this paper. First, a 500-nm-thick thermal oxide is grown on the Si wafer by a furnace system. A 50-nm-thick undoped amorphous-Si (α-Si) layer is deposited on thermal oxide in a low-pressure chemical vapor deposition (LPCVD) system at 550 °C. Then, a 50-nm-thick α-Si layer is recrystallized by solid-phase crystallization process at 600 °C for 24 h in a N_2 ambient. The source and drain regions are formed by the phosphorous atoms implantation with implant energy of 17 keV and dose of 5×10^{15} cm^{-2}, then activated by furnace at 600 °C for 24 h. The device active region is formed by patterning and dry etching. After a standard RCA cleaning, a ~ 10-nm tetraethyloxysilane film as a tunneling oxide (SiO_2) is deposited through LPCVD system at 550 °C. The following deposition of Eu_2O_3 or Y_2O_3 thin film (~ 3 nm) is conducted by an evaporation system. A blocking oxide of SiO_2 (~ 20 nm) is then deposited by plasma-enhanced chemical vapor deposition at 350 °C. After the patterning of contact holes, a 500-nm-thick Al is deposited by physical vapor deposition and patterned as Al gate and source/drain contact pads. The cross-sectional view of the Eu_2O_3 or Y_2O_3 LTPS-TFT nonvolatile memory structure is shown in Fig. 1. The length and width of the n-channel LTPS-TFT memory device are 10 and 10 μm, respectively.

The film thickness of tunneling oxide and charge trapping layers is determined by ellipsometer. The film composition of

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T.-M. Pan, S.-H. Huang, and C.-T. Lo are with the Department of Electronics Engineering, Chang Gung University, Taoyuan 33302, Taiwan (e-mail: tmpan@mail.cgu.edu.tw).

L.-C. Yen and T.-S. Chao are with the Department of Electrophysics, National Chiao Tung University, Hsinchu 30010, Taiwan.

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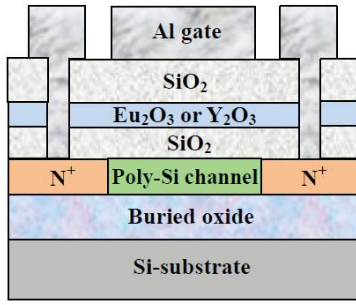

Fig. 1. Cross-sectional view of the Eu_2O_3 or Y_2O_3 LTPS-TFT device memory structure.

the Eu_2O_3 and Y_2O_3 films is examined using X-ray photoelectron spectroscopy (XPS). The bonding structures of the films are analyzed using a monochromatic Al K_α (1486.7 eV) source. The chemical shift in the spectra is corrected using the C ls peak from adventitious carbon at a binding energy of 285 eV. The curve-fit analyses are performed for Eu 4d, Y 4d, and O 1s photopeaks using Lorentzian–Gaussian functions in an effort to identify the functionalities associated with each element. When peak fitting is necessary to locate peak position or integrate area, Lorentzian-Gaussian functions are produced by minimizing the misfit error. High frequency capacitance–voltage (CV) measurements are recorded at 0.1 MHz using an Agilent 4284A LCR meter. The dielectric constant of the films is determined from the capacitances measured in the accumulation regions of the CV curves. The current–voltage (I_{DS}–V_{GS}) characteristics of high-κ Eu_2O_3 and Y_2O_3 LTPS-TFT memory devices are measured using an HP 4156C semiconductor parameter analyzer.

III. Results and Discussion

We used XPS to examine the structural and compositional changes in the Eu_2O_3 and Y_2O_3 charge trapping films on the tunnel oxide (SiO_2). The Eu 4d and O 1s XPS spectra of the Eu_2O_3 films are shown in Fig. 2(a) and (b), respectively, with their appropriate peak curve-fitting lines. The Eu $4d_{3/2}$ and $4d_{5/2}$ double peaks of the Eu_2O_3 reference appeared at 141.1 and 135.6 eV [17], respectively. The position of the Eu 4d peak of the Eu_2O_3 film shifted to a higher binding energy by $\sim$0.3 eV compared with that of the Eu_2O_3 reference, indicating the formation of a silicate layer at the Eu_2O_3–oxide interface [16]. The O 1s signal of Eu_2O_3 film comprised three peaks at 530.7, 532, and 533 eV, which we assign to Eu–O, Eu–O–Si, and Si–O binding [17], respectively. The O 1s peak of the Eu_2O_3 film exhibits a large intensity peak corresponding to Eu–silicate and two small intensity peaks corresponding to Eu_2O_3 and SiO_2. Fig. 2(c) and (d) shows the Y 4d and O 1s XPS spectra of the Y_2O_3 film, respectively. The Y 4d double peaks (Y $4d_{3/2}$ and $4d_{5/2}$ located at 159.3 and 157.2 eV, respectively), are shifted [Fig. 2(c)] to higher binding energies relative to those of the Y_2O_3 reference (158.9 and 156.8 eV, respectively) [18], presumably because of the formation of a thicker Y silicate layer [19]. In addition, the O 1s spectra of Y_2O_3 film can be deconvoluted into three peaks located at 529.6, 531.9, and 533 eV, corresponding to Y_2O_3,

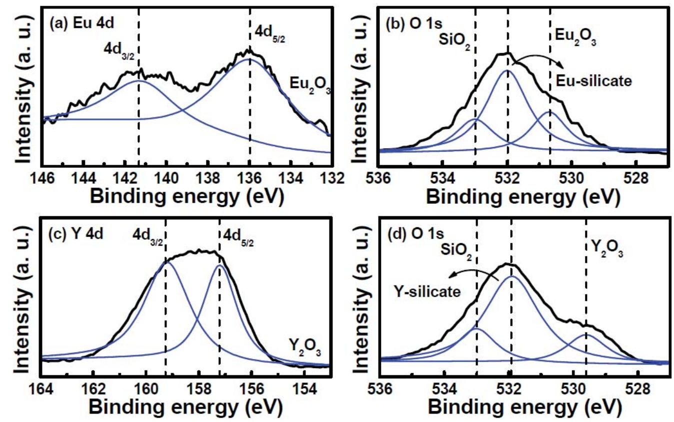

Fig. 2. XPS spectra of (a) Eu 4d, (b) O 1s for the Eu_2O_3 charge trapping layer, (c) Y 4d, and (d) O 1s for the Y_2O_3 charge trapping layer.

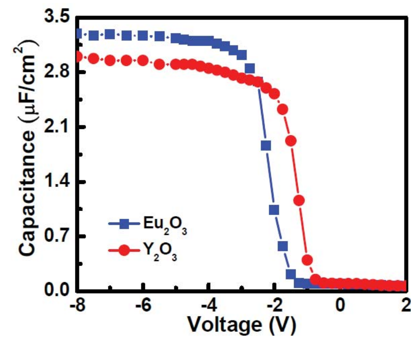

Fig. 3. CV curves of the Al/Eu_2O_3/p-Si and Al/Y_2O_3/p-Si structure devices.

Y-silicate, and SiO_2 [18], respectively. The intensity of O 1s peak corresponding to silicate layer for the Y_2O_3 film is wider compared with the Eu_2O_3 film, suggesting a higher degree of reaction between the Y and Si atoms leading to more of a Y silicate layer. In turn, experiment indicates that the reaction between Y_2O_3 and SiO_2 readily forms Y-silicates (Gibbs free energy of formation $\Delta G = -1728.18$ kJ/mol), much more that in the case of Eu_2O_3 ($\Delta G = -1472.36$ kJ/mol) [19], [20], which implies that the formation of an yttrium silicate layer is thermodynamically more favorable. In other words, the Eu_2O_3 film is thermodynamically stable.

Fig. 3 shows the CV curves measured at frequency of 0.1 MHz for the Al/Eu_2O_3/p-Si and Al/Y_2O_3/p-Si capacitors. The Al/Eu_2O_3/p-Si device exhibited a higher capacitance density than the Al/Y_2O_3/p-Si one. The κ value of the Eu_2O_3 and Y_2O_3 dielectric films is determined to be about 11 and 9.6, respectively. It is reported that high-κ materials possess better charge-trapping efficiency than Si_3N_4 materials [21]. As expected, a higher field is induced at the tunnel barrier, enabling faster P/E speed. In addition, the Al/Eu_2O_3/p-Si capacitor exhibited a larger flatband voltage (V_{FB}) compared with the Al/Y_2O_3/p-Si one. A larger V_{FB} may be because of a significant number of positive charges into the oxide [16].

Fig. 4 shows the transfer characteristics of the Eu_2O_3 and Y_2O_3 LTPS-TFT memory devices. The measured conditions for programing are $V_{GS} = -10$ V, $V_{DS} = 5$ V, and 0.1 s, and for erasing are $V_{GS} = 15$ V and 0.1 s. Therefore, a band-to-band tunneling-induced hot hole (BTBT HH) is used

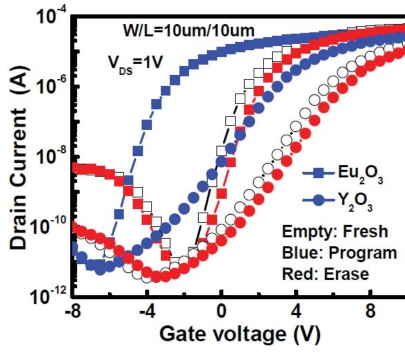

Fig. 4. Transfer and P/E characteristics of the high-κ Eu_2O_3 and Y_2O_3 LTPS TFT memory devices.

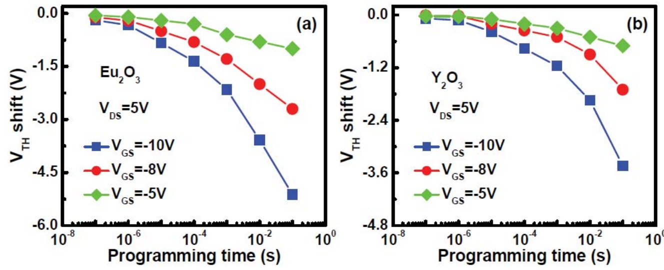

Fig. 5. Programming characteristics of (a) Eu_2O_3 and (b) Y_2O_3 LTPS TFT memory devices.

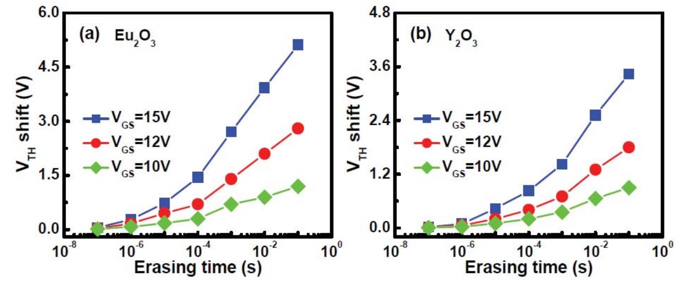

Fig. 6. Erasing characteristics of (a) Eu_2O_3 and (b) Y_2O_3 LTPS TFT memory devices.

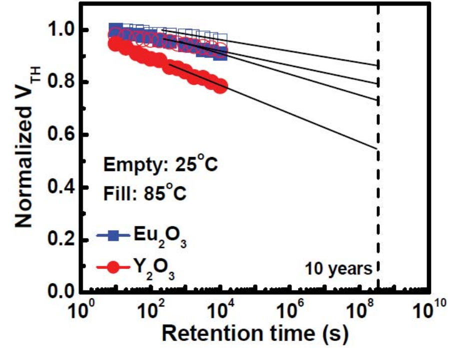

Fig. 7. Retention characteristics of the high-κ Eu_2O_3 and Y_2O_3 LTPS TFT memory devices.

to program, and Fowler–Nordheim (FN) tunneling is used to erase these devices hereafter. We have tried to program by injecting the electrons (by applying a positive voltage to both the gate and drain), but no significant shift of the I_{DS}–V_{GS} curve is observed. The Eu_2O_3 LTPS-TFT memory device exhibits superior electrical performance than the Y_2O_3 LTPS-TFT memory one, including subthreshold swing (SS) that improved from 1525 to 617 mV/dec, and memory window that increased from $\sim$3.4 to $\sim$5.2 V. The degradation of the SS of the Y_2O_3 LTPS-TFT memory device may be attributed to the specific property of this film and the formation of a thicker silicate layer at the Y_2O_3–oxide interface.

To further observe the program and erase characteristics of the memory cell as a function of operating time, we have monitored an evolution of I_{DS}–V_{GS} curve under different operation voltages. Fig. 5 shows the program characteristics of the Eu_2O_3 and Y_2O_3 LTPS-TFT memory devices as a function of pulsewidth for various operation conditions. The V_{TH} values are obtained from the I–V curves for achieving the current value of 100 nA (100 $\times$ W/L nA) at $V_{DS} = 1$ V. The V_{TH} shift is defined as the change of threshold voltage of a device between the programed and the erased states. For the condition of $V_{GS} = -10$ V and $V_{DS} = 5$ V at 0.1 s, high programing performance of Eu_2O_3 LTPS-TFT memory can be obtained with a memory window of $\sim$5.1 V. The SONOS-type memory device using an Eu_2O_3 charge-trapping layer exhibited higher values of V_{TH} shift relative to that of the device featuring the Y_2O_3 charge-trapping layer. This result presumably arises from the high charge-trapping efficiency of the Eu_2O_3 layer, because of the Eu_2O_3 film possessing a high dielectric constant, and the formation of a thin low-κ interfacial layer, which increased the effective electric field across the tunneling oxide, thereby enhancing hole trapping and electron detrapping in the film simultaneously. In contrast, we attribute the small V_{TH} shifts of the low-dielectric-constant Y_2O_3 films to their decreased charge-trapping efficiency caused by decreasing tunneling efficiency.

The erase characteristics of the Eu_2O_3 and Y_2O_3 LTPS-TFT memory devices as a function of various operation voltages are shown in Fig. 6. It is evident that the excellent erase speed of $\sim$0.1 s can be obtained for $V_{GS} = 15$ V. The V_{TH} shift is because of the electron trapping in the Eu_2O_3 or Y_2O_3 film. The Eu_2O_3 LTPS-TFT memory device revealed a large memory window of $\sim$5.2 V at $V_{GS} = -10$ V and $V_{DS} = 5$ V for 0.1 s and $V_{GS} = 15$ V for 0.1 s for the programing and erasing operations, respectively. The introduction of high-κ materials varies the electric field distributions dramatically across the tunnel oxide, charge trapping layer, and blocking layer, respectively. The effective electric field cross the tunneling oxide for the Eu_2O_3 and Y_2O_3 film is 4.83 and 4.8 MV/cm, respectively. Under the erase operation, the electrons tunnel easily into the Eu_2O_3 layer through the SiO_2 tunnel layer from the poly-Si channel. In addition, during the erase operation, at the same gate bias where FN tunneling erases, the electrons would easily tunnel through a tunnel layer to the Eu_2O_3 conduction band, as compared to the Y_2O_3 case. The conduction band offset of Eu_2O_3 with respect to silicon is 2.1 eV, as compared with a 2.3 eV conduction band offset of Y_2O_3 with respect to silicon [22].

One of the most important operating parameters of such a LTPS-TFT memory device concerning its reliability is the

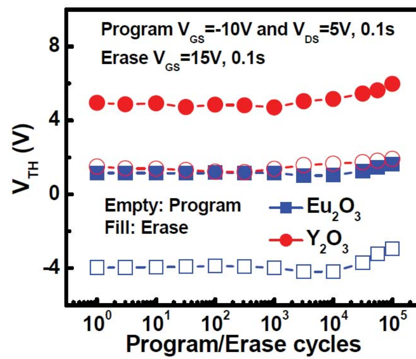

Fig. 8. Endurance characteristics of the high-κ Eu_2O_3 and Y_2O_3 LTPS TFT memory devices.

data retention and endurance characteristics. Fig. 7 shows the retention characteristics of the Eu_2O_3 and Y_2O_3 LTPS-TFT memory devices at room temperature and 85 °C. The retention measurement is performed after the BTBT HH programing. The normalized V_{TH} shift is defined as the ratio of V_{TH} shift at the time of interest and at the beginning. Using this as an indicator, we can see the charge loss for the SONOS-type nonvolatile memory. At room temperature, we observed a $<15\%$ charge loss after ten years for the Eu_2O_3 SONOS-type memory device. The LTPS-TFT memory devices incorporating the Eu_2O_3 charge-trapping layers exhibited longer retention times than those featuring the Y_2O_3 charge-trapping layers. The high charge losses in the Y_2O_3 film arose because of the formation of a thick silicate layer at the Y_2O_3–SiO_2 interface. A large number of holes will leak from the shallow trap sites of the silicate layer [23], presumably due to trap-assisted tunneling. At the hot temperature of 85 °C, the retention capability significantly degrades for Eu_2O_3 LTPS-TFT memory device because of the enhancement of thermal tunneling of carriers from the Eu_2O_3; however, the expected memory window after ten years is charge loss $<30\%$, which could be sufficient for proper memory functioning.

Fig. 8 shows the endurance curves of the Eu_2O_3 and Y_2O_3 LTPS-TFT memory devices. The LTPS-TFT memory device using a Eu_2O_3 the charge-trapping layer exhibited a larger memory window than that featuring the Y_2O_3 charge-trapping layer. The memory window of Eu_2O_3 SONOS-type memory device is 4.6–5.2 V after 10^5 P/E cycles. No significant window narrowing is found. The V_{TH} increase in the later stage of endurance is due to some electron left in the charge-trapping layer after programing. The reason is because of the electrons that are tightly trapped in the charge trapping layer and hard to escape by FN erase. This finding suggests that the endurance characteristics of Eu_2O_3 LTPS-TFT memory device still behave well. The proposed a Eu_2O_3 film as the charge trapping layer exhibits the potential to be incorporated into the future LTPS-TFT nonvolatile memory fabrication processes.

The measured and extracted TFT memory parameters are shown Table I, where the data from TFT memory devices using various charge-trapping layers of SiN_x [24], Hf-silicate [7], Eu_2O_3, and Y_2O_3 are listed for comparison. The Eu_2O_3 charge-trapping layer shows the smallest SS, largest memory, superior data retention, and excellent endurance characteristics. It is believed that the P/E voltage and speed of an Eu_2O_3 LTPS-TFT memory can be further improved through reducing the thickness of the blocking layer.

TABLE I
COMPARISON OF DEVICE PARAMETERS FOR LPTS-TFT MEMORY DEVICES FABRICATED WITH SiN_x, HF-SILICATE, Eu_2O_3, AND Y_2O_3 CHARGE TRAPPLING LAYERS

	SiN_x	Hf-silicate	Eu_2O_3	Y_2O_3
SS (mV/dec)	$\sim$1200	$\sim$1000	617	1525
Program voltage and time	$V_{GS} = 18$ V 100 ms	$V_{GS} = 12$ V $V_{DS} = 12$ V 1 ms	$V_{GS} = -10$ V $V_{DS} = 5$ V 100 ms	$V_{GS} = -10$ V $V_{DS} = 5$ V 100 ms
Erase voltage and time	$V_{GS} = -18$ V 100 ms	$V_{GS} = -10$ V $V_{DS} = 10V$ 10 ms	$V_{GS} = 15$ V 100 ms	$V_{GS} = 15$ V 100 ms
Memory window (V)	$\sim$3	$\sim$3	5.2	3.4
Retention	NA	68% @85 °C	< 30% @85 °C	45% @85 °C
Endurance	~ 500	$\sim 10^4$	$\sim 10^5$	$\sim 10^5$

IV. CONCLUSION

We fabricated LTPS-TFT memory devices using the Eu_2O_3 and Y_2O_3 film as a charge trapping layer. We used the BTBT HH and FN methods to program and erase for Eu_2O_3 and Y_2O_3 LTPS-TFT memory devices, respectively. The LTPS-TFT incorporating a Eu_2O_3 charge trapping layer exhibited a smaller SS of 617 mV/dec, a larger memory window of $\sim$5.2 V ($V_{GS} = -10$ V and $V_{DS} = 5$ V for 0.1 s), a lower charge loss of $<15\%$ (at room temperature), and a better endurance characteristic (P/E cycles up to 10^5) than that featuring the Y_2O_3 charge trapping layer. This result suggested that Eu_2O_3 film featuring a thinner silicate layer and a higher dielectric constant provided a higher probability for trapping of the charge carrier. The Eu_2O_3 thin film is a promising charge trapping layer material for the fabrication of LTPS-TFT memory devices.

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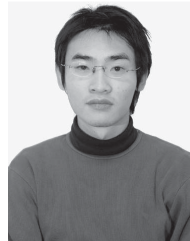
Tung-Ming Pan received the Ph.D. degree from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, in 2001.

He has been a Professor with the Department of Electronics Engineering, Chang Gung University, Taoyuan, since 2009.

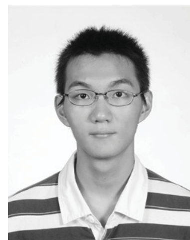
Li-Chen Yen is currently pursuing the Ph.D. degree with the Department of Electrophysics, National Chiao Tung University, Hsinchu, Taiwan.

His current research interests include the study of biosensors, nonvolatile memories, and high-κ technology.



Sheng-Hao Huang received the M.S. degree in electronics engineering from Chang Gung University, Taoyuan, Taiwan, in 2011.

His current research interests include device and process technologies for the high performance and reliability of LTPS-TFT memory devices.



Chieh-Ting Lo received the M.S. degrees in electronics engineering from Chang Gung University, Taoyuan, Taiwan, in 2011.

His current research interests include device and process technologies for the high performance and reliability of LTPS-TFT memory devices.

Tien-Sheng Chao received the Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1992.

He has been a Professor with the Department of Electrophysics, National Chiao Tung University, Hsinchu, since 2002.