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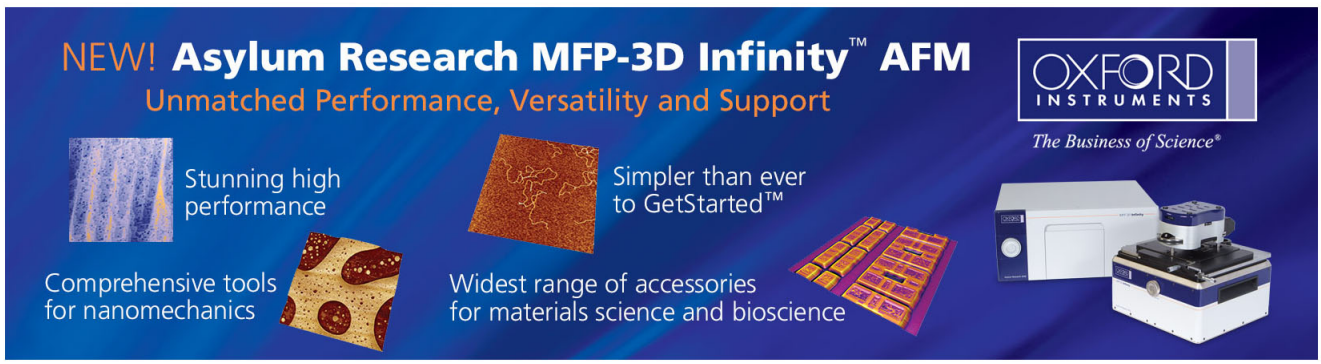

Insertion of a Si layer to reduce operation current for resistive random access memory applications

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In this study, a reduction of low resistive state (LRS) current is discovered in a V:SiO_2/Si bi-layer structure with the addition of a Si layer. A Pt/V:SiO_2/TiN structure is fabricated as the standard sample. The results of conduction mechanism analyses for LRS indicate that a SiO_2 interfacial layer forms through oxidation of the inserted Si layer after the set process. The LRS current reduction can be attributed to the formation of this SiO_2 layer. In addition, self-compliance behavior for the bi-layer structure during the set process further proves the existence of this SiO_2 buffer layer in LRS. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4812304]

Because of the scaling down devices used for conventional charge storage based memories, performance reliability is a significant challenge due to physical limitations.[1–3] Recently, resistive random access memory (ReRAM) has developed and attracted extensive attention as a substitute for next-generation memory because of its superior properties. Such resistive switch (RS) behavior has been found in various materials.[4–9] In this letter, RS studies are performed in an SiO_2-based ReRAM structure due to its high compatibility with current semiconductor manufacturing industry processes.[10,11] In order to promote the application of ReRAM devices, studies have concentrated on issues such as the stability of the switching behavior, a reduction of the operation current (power), and an improvement of the cross-talk issue.[12–15] According to these previous studies, switching stability can be improved by a metal doping system.[16,17] Therefore, a vanadium (V)-doped SiO_2 layer is chosen in this study. In addition, we attempt to reduce the operation current by using a bi-layer stack structure.

In this work, a TiN bottom electrode was deposited on a SiO_2/Si substrate. Contact-holes were defined by patterning the spacer constructed from the SiO_2 formed low temperature oxide (LTO) film by using standard lithography and reactive ion etching on the TiN bottom electrode. The 17-nm-thick vanadium (V)-doped silicon dioxide layer was stacked, followed by the 3-nm-thick Si layer in order to form the bi-layer structure (sample B) by co-sputtering the vanadium and SiO_2 targets. The 3-nm-thick Si layer is pre-deposited on the TiN by sputtering intrinsic Si target in pure Ar ambient. Devices were completed after the lift-off process by the subsequent deposition of a 200-nm-thick Pt top electrode. The devices without an inserted Si layer were simultaneously fabricated with the standard sample, termed sample A. Schematic diagrams of these two structures are shown in Fig. 1(a).

The RS characteristics were measured by using an Agilent B1500 semiconductor characterization analyzer with biasing at the TiN terminal and grounding at the Pt terminal. Devices in this letter were activated by a positive forming process with a compliance current of 1 μA. The reversible RS behavior can be switched from high resistive state (HRS) to low resistive state (LRS) through the set process by positive voltage with compliance current of 3 mA and switched back to HRS through the reset process by negative voltage.

The active layer of vanadium (V)-doped silicon dioxide layer (V:SiO_2) is confirmed by Fourier transform infrared (FTIR) analyses. From the FTIR spectrum shown in Fig. 1(b), the absorption signals of V can be obtained in addition to the Si signals.[18,19] Both V and Si are discovered in the oxidative phase. As a result, V is confirmed to be doped in the SiO_2 film. Subsequently, the RS behaviors of these two devices are performed and compared in Fig. 1(c). A remarkable decrease of the LRS current is presented in the switching characteristic of the V:SiO_2/Si bi-layer structure (sample B). In addition, the reset voltage (V_{reset}), which is defined as the voltage where the current begins to decrease, also increases.

In order to investigate the difference between samples A and B, conduction mechanisms are analyzed. Figure 2(a) shows the analyses of both LRS and HRS for sample A. As the biasing voltage is small, the conducting electrons are driven by the electric field. Ohmic conduction dominates the conduction mechanism. In contrast, Poole-Frenkel emission dominates the conduction mechanism at a higher bias due to the more apparent lowering of the trap barrier, as shown in Fig. 2(b). After a reset process, LRS transforms to HRS by the formation of an interfacial insulator, called as switching layer (SL).[20] As a result, Schottky emission dominates the initial small voltage zone. Afterward, Poole-Frenkel emission becomes the major mechanism due to the charge de-trapping behavior from the CF composed of oxygen vacancies, as shown in Fig. 2(c).

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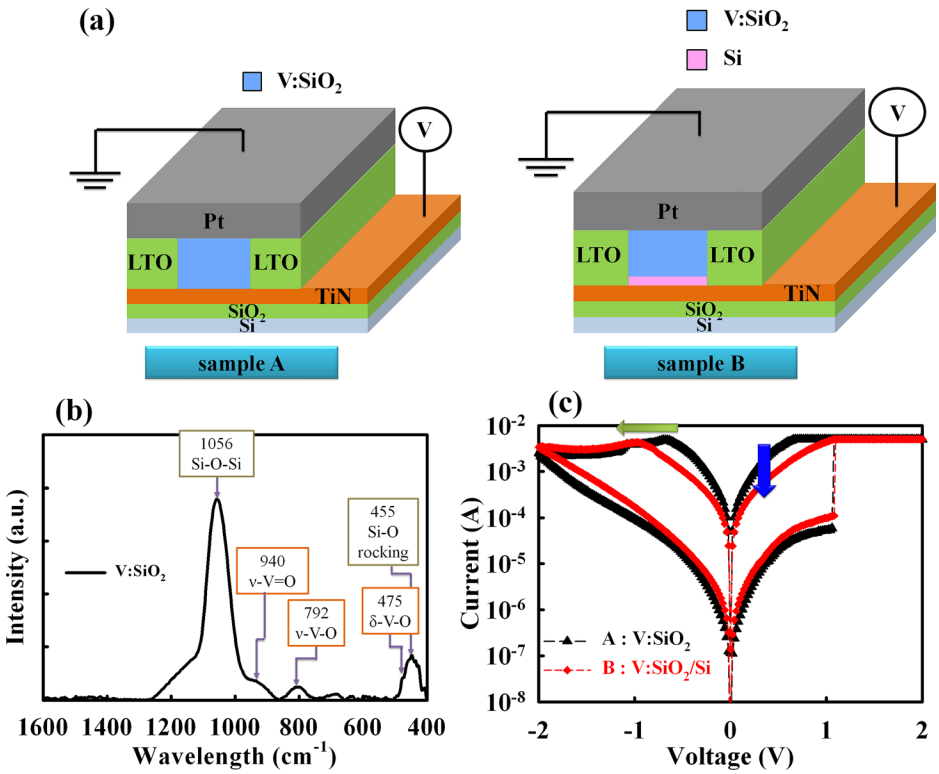

FIG. 1. (a) Schematic diagram of the two deposited structures. (b) FTIR analyses. (c) Resistive switching behavior comparison between the two devices.

The conduction mechanisms of sample B are also analyzed and shown in Fig. 3(a). The conduction mechanism follows Ohmic conduction in LRS, then changing to Schottky emission, unlike in sample A when it changes to Poole-Frenkel emission. Hence, a model is proposed to explain this difference in conduction mechanisms and is shown in Fig. 3(b). The interfacial insulator is formed by the recombination of oxygen ions and oxygen vacancies while the device is at HRS. After a set process by biasing a positive voltage on TiN, the oxygen ions can be driven toward TiN therefore oxidizing the inserted Si layer, causing the formation of a SiO_2 barrier layer between the CF of the $V:SiO_2$ film and the TiN bottom electrode. Owing to the formation of the high band gap SiO_2 barrier layer (9 eV) in LRS, the charge-transporting behavior becomes more difficult. Therefore, this SiO_2 barrier layer formation induced by the inserted Si layer increases the barrier for the transport of charges and thereby reduces LRS current, as shown in Fig. 3(c).

The increase in V_{reset} for sample B compared to that of A, shown in Fig. 1(c), also can be attributed to the formation of this SiO_2 barrier layer in LRS. Since the series resistance is increased by the additional SiO_2 layer, the reset condition that drives the oxygen ions away from TiN and thereby resets the resistance state from LRS to HRS shown in Fig. 4(a) requires a higher reset voltage. In addition, the self-compliance behavior in LRS is obtained for sample B. During the set process, the LRS can be reached without the protection of compliance current while appropriate voltage is swept, as shown in Fig. 4(b). The self-compliance behavior can also significantly act as evidence of the formation of the SiO_2 barrier layer in LRS.[21] The series resistance attributed to the formation of the SiO_2 barrier layer limits the current

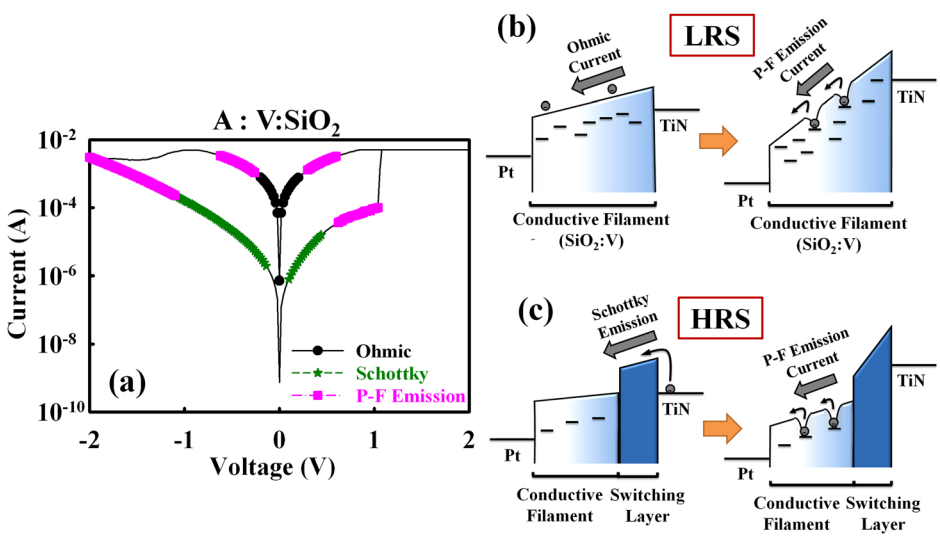

FIG. 2. (a) Conduction mechanism analyses of sample A. (b) The conduction mechanisms in LRS are Ohmic conduction followed by Poole-Frenkel emission. (c) The conduction mechanisms in HRS are a short period of Schottky emission followed by Poole-Frenkel emission.

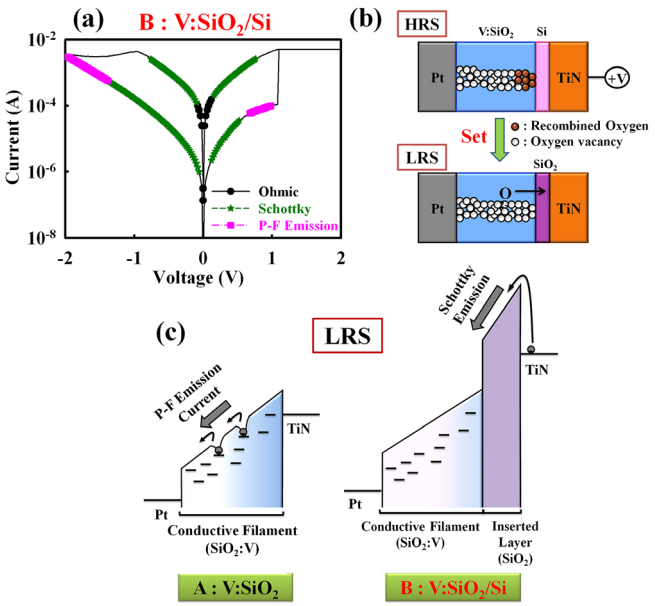

FIG. 3. (a) Conduction mechanism analyses of sample B. (b) The proposed model of the conduction mechanism in LRS during the set process. (c) Comparison of the energy band diagrams in LRS between these two structures.

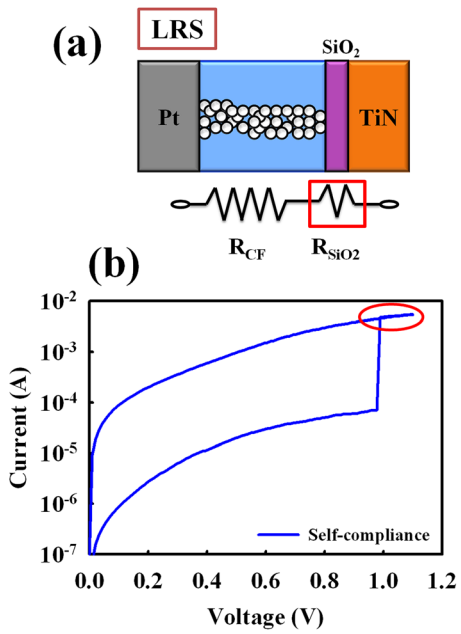

FIG. 4. (a) The schematic diagram in LRS, equivalent to two resistances in series. (b) The self-compliance behavior during set process further confirms the existence of the SiO_2 barrier layer.

characteristic. As a result, self-compliance behavior can be obtained in LRS. Due to the requirement of a compliance current during ReRAM operation, a combination of transistor and ReRAM (1T1R) has been considered as a suitable structure for an array structure nowadays.[22] However, since the large transistor size is a drawback for the development of the device scaling down, various alternative structures have been proposed.[15,23,24] Our noteworthy findings of this situation where compliance current is not required is, therefore, an advantage for the use of ReRAM devices in array structures.

In conclusion, a reduction of the LRS current is discovered in a $V:SiO_2/Si$ bi-layer structure after the addition of an inserted Si layer. The $Pt/V:SiO_2/TiN$ stack structure is fabricated as standard device. Due to the operation polarity, the oxygen ions generated among the set process are driven toward the Si/TiN terminal. Subsequently, the inserted Si layer is oxidized and forms a SiO_2 barrier layer. As a result, the LRS current can be suppressed since the dominated conduction mechanism transfers from Poole-Frenkel emission to Schottky emission. In addition, the current is limited and shows self-compliance behavior owing to the formation of this SiO_2 barrier layer. Due to this self-compliance behavior which was obtained by the insertion of a Si layer, any additional devices that are usually required to attain current compliance to protect the device from hard breakdown for an array application would therefore not be necessary.

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