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Performance and characteristics of double layer porous silicon oxide resistance random access memory

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A bilayer resistive switching memory device with an inserted porous silicon oxide layer is investigated in this letter. Compared with single Zr:SiO_x layer structure, Zr:SiO_x/porous SiO_x structure outperforms from various aspects, including low operating voltages, tighter distributions of set voltage, higher stability of both low resistance state and high resistance state, and satisfactory endurance characteristics. Electric field simulation by COMSOL™ Multiphysics is applied, which corroborates that intensive electric field around the pore in porous SiO_x layer guides the conduction of electrons. The constraint of conduction path leads to better stabilization and prominent performance of bilayer resistive switching devices. © *2013 AIP Publishing LLC*.
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Among the candidates for future non-volatile memory,[1–3] resistive random access memory (RRAM) has great potential for next-generation nonvolatile memory due to their superior characteristics such as low cost, simple structure, high-speed operation, and non-destructive readout.[4–7]

Various materials have been reported to possess the resistive switching behaviors, and silicon oxide based RRAM has shown lots of merits in RRAM switching properties.[8,9] Stable device characteristics such as concentrated distribution of reading states and lower operation power are required for the applications of next generation nonvolatile memory. Various methods can be used to modify the RRAM working properties such as material modification[10,11] and structure alteration.[12] Definitely the research using different methods to improve RRAM performance is worthy of investigation.

In our research, a single layer Zr metal doped into SiO_2 (Zr:SiO_x) by co-sputtering and a porous SiO_x fabricated by inductively coupled plasma (ICP) O_2 plasma processes were constructed to form a Zr:SiO_2/porous SiO_2 structure RRAM (inset of Fig. 2(b) is real picture of the device). ICP etching has always been a popular method to modify film structure, especially fabricating porous structure.[13–15] Moreover, by etching carbon elements in the SiO_2 film, nanopores can be formed.[16] To make a comparison, single Zr:SiO_x layer RRAM was also fabricated. Resistive switching characteristics of both single Zr:SiO_x layer and bilayer Zr:SiO_2/porous SiO_2 RRAM devices have been investigated. Finally COMSOL Multiphysics[17] was applied to simulate the electrical field concentrating capability of nanopores.

The experimental specimens were prepared as follows: for the single layer specimen, the Zr:SiO_x thin film (about 20 nm) was deposited on the TiN/Ti/SiO_2/Si substrate by co-sputtering with the pure SiO_2 and Zr targets. The patterned substrate was obtained by standard deposition and etching process, after which 1 μm × 1 μm via holes were formed. Also, the three dimensional view of the device is shown as the inset of Fig. 4. The sputtering power was fixed at RF power 200 W and 20 W for SiO_2 and Zr targets, respectively. The co-sputtering was executed in argon ambient (Ar = 30 sccm) with a working pressure of 6 mTorr at room temperature. However, for the double resistive switching layer specimen, at beginning a C:SiO_x film (about 6 nm) was deposited by co-sputtering with the SiO_2 and C targets and then processed by ICP O_2 plasma. The sputtering power was fixed at RF power 200 W and 5 W for SiO_2 and C targets, respectively. The co-sputtering was also executed in argon ambient (Ar = 30 sccm) with a working pressure of 6 mTorr at room temperature. The ICP oxygen plasma etching process is shown schematically in Fig. 1. By burning carbon elements in the SiO_2 layer, nanopores are formed. Fourier transform infrared (FTIR) spectroscope was applied after the ICP etching process, from which we found the concentration of carbon elements dropped drastically (not shown here). The ICP power was fixed at 600 W with a treatment period of 5 s. Then the layer of Zr:SiO_x (about 14 nm) was deposited with the same RF power, argon ambient, and working pressure as antecedent single Zr:SiO_x layer specimen.

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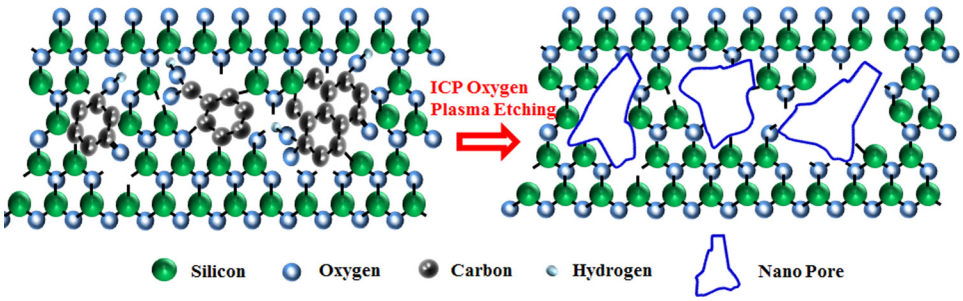

FIG. 1. Schematic view of ICP oxygen plasma process. Nanopores are formed by etching carbon elements in SiO_2 layer.

Ultimately, the Pt top electrode of 200 nm thickness was deposited on both specimens by DC magnetron sputtering. The entire electrical measurements of devices with the Pt electrode were performed using Agilent B1500 semiconductor parameter analyzer.

The electroforming process is required to activate all of the RRAM devices, using dc voltage sweeping with a compliance current of 10 μA. Then, dc voltage sweeping cycling test is performed to evaluate both types of devices. During the dc sweeping test of more than 10 samples, we find that Zr:SiO_x/porous SiO_x RRAM devices have smaller working currents on both low resistance state (LRS) and high resistance state (HRS) compared with single layer devices. Figure 2(a) compares the I-V curve of both types of devices, from which working current reduction phenomenon can be observed. It is also noted that the single Zr:SiO_x layer device has less uniform set voltage during dc sweeping cycles, which is further revealed in the distributions comparison of set voltage of single layer and bilayer RRAM devices (Figure 2(b)). Furthermore, from Figures 2(c) and 2(d) we can see that the stability between HRS and LRS of Pt/Zr:SiO_x/TiN RRAM exhibit more fluctuations compared with Pt/Zr:SiO_x/porous SiO_x/TiN structure devices.

To further evaluate the memory performance, measurement of endurance of both kinds of devices was performed, as shown in Figure 3. During 10^4 sweeping cycles, HRS and LRS of Zr:SiO_x RRAM overlap each other (Figure 3(a)) while to Zr:SiO_x/porous SiO_x RRAM device it exhibits stable HRS and LRS even after more than 10^6 sweeping cycles (Figure 3(b)).

During the test process of endurance, we find porous structure RRAM devices need less time (30 ns) in the setting process compared with single layer structure, whose positive pulse lasts 40 ns, which can been seen from the bottom diagrams of Figure 3. In order to clarify that bilayer RRAM devices need less time in the setting process, we apply fast I-V measurement to measure setting time more accurately. From Figure 4, it can be observed that single Zr:SiO_x layer device needs almost 400 ns to change from HRS to LRS, while it needs only half of that

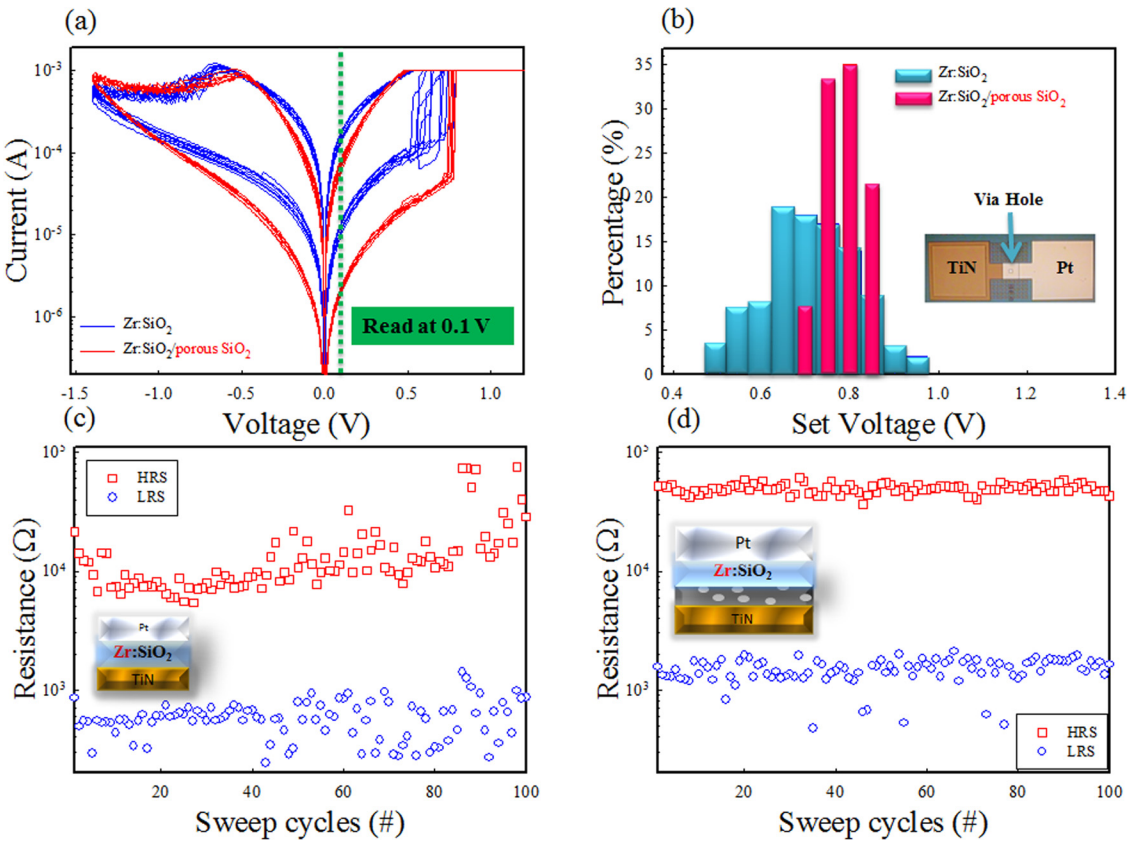

FIG. 2. (a) Resistive switching characteristics comparison of normal and porous oxide structure RRAM. (b) Distributions of set voltage. Inset is the real picture of device. (c), (d) Distributions of HRS and LRS within 100 cycles of single Zr:SiO_2 layer and porous oxide structure RRAM, respectively.

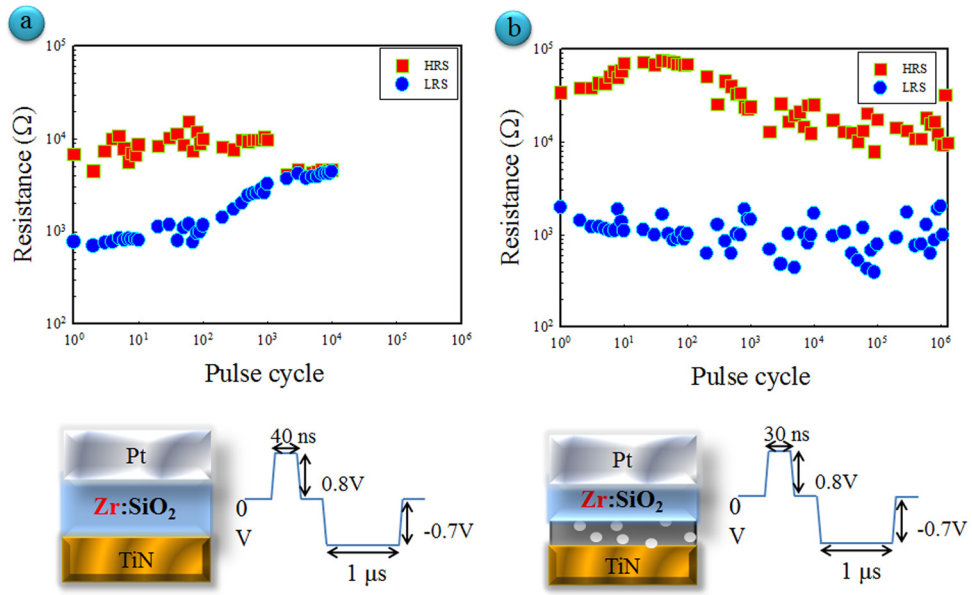

FIG. 3. (a) and (b) Endurance characteristics of $Zr:SiO_2$ and $Zr:SiO_2$/porous SiO_2 RRAM, respectively. The bottom diagrams are the corresponding device structures and endurance testing pulse.

time to $Zr:SiO_x$/porous SiO_x RRAM device for resistance switching.

To understand the impact of the inserted porous SiO_x layer, we utilize COMSOL Multiphysics[17] software to simulate the distribution of electric field and to confirm the electrical field concentrating capability of nanopores. As carbon elements are burned in the ICP process leaving pores in the SiO_2 layer, the permittivity is set as 1, which is equal to the permittivity of vacuum,[18] and the permittivity of silicon dioxide equals to 3.9.[19] The permittivity of metal filament which formed after electro-forming process is set with 1×10^6, high enough to comply with metal property. Besides, because the film fabricated by sputter process has a lower density compared with chemical vapor deposition and the total film thickness of porous SiO_2 layer is 6 nm, pore's size is set with an estimated radius of 0.7 nm in the simulation process.[13,16] The mesh size is applied with extra fine mode with minimum element size of 2.7×10^{-12} m to get precise enough electrical field distribution, and the voltage applied on the bottom electrode is 2 V with the top electrode grounded. Electrostatics(es) under AC/DC module is used to calculate stable state electrical field distribution, as shown in Figure 5; it can be obviously seen that there exists higher density of electric field in and around the area of the pore in porous SiO_x layer, confirming the electrical field concentrating capability of nanopores. Compared with SiO_2, pore in porous SiO_x layer works much like low-k (low dielectric constant) dielectric,[20] which has a tendency to concentrate electric field. Thus during the forming process, metal conduction filaments have an inclination to form towards the direction of pore, which means we can obtain a relative strong and stable filament. As electrons tend to conduct through a relative uniform path, we can observe that $Zr:SiO_x$/porous SiO_x RRAM devices work much more stable and have tighter distribution of set voltage.

The resistive switching mechanism of single $Zr:SiO_x$ layer RRAM can be explained by the stochastic formation and rupture of conduction filaments.[21] Due to the stochastic

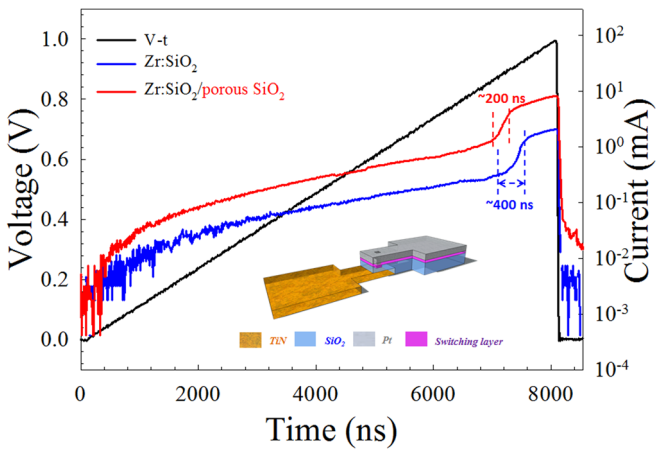

FIG. 4. Setting time comparison under fast I-V test. Inset is the 3-D schematic structure of device.

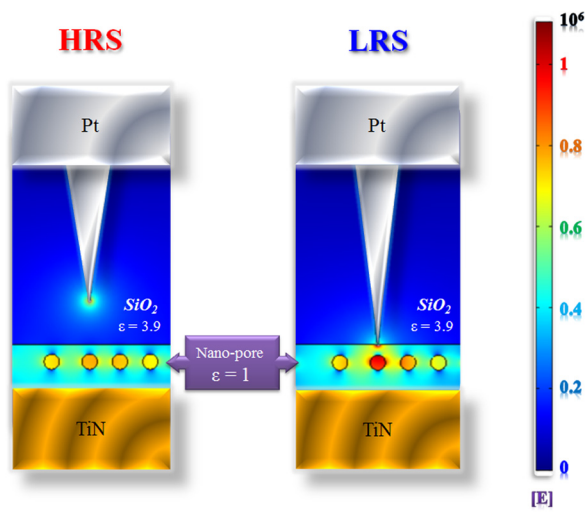

FIG. 5. Electric field simulation of HRS and LRS of $Zr:SiO_x$/porous SiO_x RRAM.

formation of conduction filaments process, single active layer RRAM device exhibits less stable set voltage and lower degree of uniformity in dc sweeping process. However, if the porous SiO_x layer is added at the bottom electrode of TiN, filaments growth has much more directionality, where, in turn, better stabilization can be achieved.

In conclusion, the single layer $Zr:SiO_2$ RRAM and bilayer $Zr:SiO_2$/porous SiO_2 RRAM have been fabricate to investigate the resistive switching characteristics. Bilayer RRAM devices have superior properties owing to the relative stable conduction path, as pore in porous SiO_x layer has an inclination to guide the formation of metal conduction filaments. COMSOL Multiphysics is used to simulate the distribution of electric field, from which mutual verification with experimental data can be obtained.

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