RF Noise Shielding Method and Modelling for Nanoscale MOSFET

Jyh-Chyurn Guo[1], Yi-Min Lin[2] and Yi-Hsiu Tsai[3]

Institute of Electronics, National Chiao-Tung University, 1001 Ta-Hsueh Rd, Hsinchu, Taiwan, R.O.C.

[1]jcguo@mail.nctu.edu.tw

[2]ymlin.ee93g@nctu.edu.tw , [3]goodluck.ee94g@nctu.edu.tw

***Abstract*—RF noise shielding methods with different coverage areas (Pad and TML shielding) were implemented in two port test structures adopting 100-nm MOSFETs. Noise measurement reveals an effective suppression of NF_{min} but increase of NF_{50}, simultaneously from the shielding methods. The suppression of NF_{min} is contributed from the reduction of $Re(Y_{opt})$ while the noise resistance R_n is kept nearly the same. A lossy substrate model developed in our original work for a standard structure without shielding can be easily extended based on the layout and topology of the shielding schemes to predict the noise shielding effect and explain the mechanisms. The extended lossy substrate model indicates that the elimination of substrate loss represented by substrate RLC networks is the major mechanism contributing the reduction of NF_{min}. However, the increase of parasitic capacitance generated from the shielding structures is responsible for the degradation of f_T and NF_{50}. The results provide an important insight and guideline for low noise RF circuit design.**

I. Introduction

Noise coupling through Si substrate has been identified as a critical killer to mixed signal IC with digital and analog circuits on a single chip. To overcome this failure mechanism, many works have been done on substrate noise isolation techniques. Among the proposed methods, heavily doped guard ring (GR), triple well, and deep trench are most frequently used [1-3]. However, their noise isolation capability is generally limited to few GHz [3], and become ineffective in advanced RF CMOS circuits with operating frequency driven by nanoscale technology to well beyond 10 GHz. Besides, most of the characterization and analysis focused on the isolation between two features on the same chip, such as port-to-port, pad-to-pad, or device-to-device isolation in terms of $|S_{12}|$ but quite few literatures covered a systematic study of shielding effect on RF noise in miniaturized devices, which are vulnerable to lossy substrate effect. A ground shielded bond pad structure was proposed and fabricated in Si bipolar technology [4]. A significant improvement over pad-to-pad isolation ($|S_{12}|$) and suppression on LNA noise figure (NF) was demonstrated. The experimental results prove the ground shielding effect on isolation ($|S_{12}|$), gain ($|S_{21}|$), and noise (NF). However, a simple resistance model was assumed and implemented to simulate the substrate coupling effect. This simplified model may be valid in sufficiently low frequency ($\leqq$ 10 GHz) but is no longer accurate to fit high frequency domain up to tens of GHz. The validity of a simple RC model and the limitation of frequency have been investigated through a serious comparison between electroquasistatic (EQS) and electrodynamic (ED) models [5]. The results indicate an inductive like characteristics in noise propagation through the substrate and suggest that ED model is indispensable to realize an accurate simulation in high frequency up to several tens of GHz. Unfortunately, the EM analysis requires complicated computation and extensive memory, and is not suitable for circuit simulations. All the mentioned challenges trigger our motivation of this work.

In our previous work, a lossy substrate model in an equivalent circuit form has been developed to accurately predict the RF noise measured from sub-100 nm MOSFETs under high frequency up to 18 GHz [6-8]. The substrate RLC networks, for the first time proposed in our original model, incorporating inductive impedance together with RC networks can simulate the substrate noise coupling through the pad and transmission line (TML) with a broadband accuracy and scalability over different pad structures and TML topologies [9]. In this paper, we will demonstrate that the original lossy substrate model for standard structure without shielding can be easily extended for those with shielding to predict the influence on high frequency S-parameters and noise parameters. An interesting result with an opposite trend in minimum noise figure (NF_{min}) and 50Ω noise figure (NF_{50}) will be presented and discussed.

II. RF Noise Shielding Structure Design and Extended Lossy Substrate Model

100 nm RF n-MOSFETs were fabricated in 130nm CMOS process as the core devices for this study. Multi-gate-finger structures with various finger widths and numbers, W/N=4μm/6, 2μm/12, 1μm/24 under a fixed total width, W_{tot}=WxN=24μm were designed to investigate the trade-off between gate resistance (R_g) and capacitances. The experimental results indicate that the smaller W and larger N can reduce R_g but increase parasitic capacitances at gate terminal. The former one can help suppress gate induced excess noise. Unfortunately, the later one generally degrades f_T due to increased gate capacitances and may overwhelm the advantage of smaller R_g. In this paper with limited pages, W/N=4μm/6 is selected for presentation due to the best high frequency performance represented by highest f_T. Note that W_{tot}=24μm is a relatively small dimension selected for

achieving lower current and low power, but taking a trade-off with lower g_m and higher noise resistance (R_n), and raised challenge to low noise design.

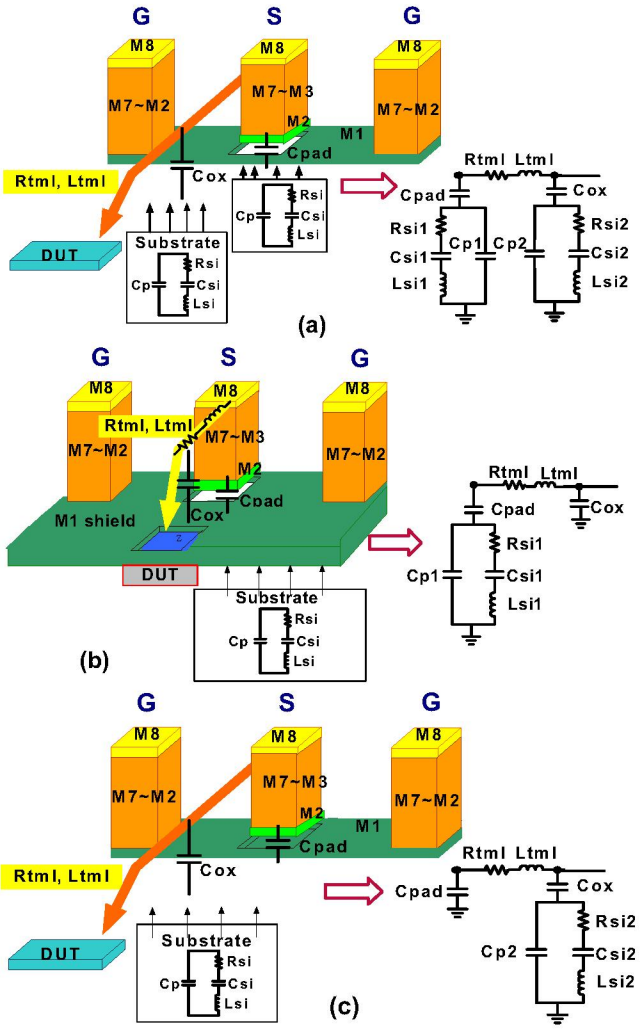

Fig.1 RF test structures adopting device under test (DUT), GSG pads, TML, and different shielding schemes (a) standard without shielding (b) TML shielding (c) pad shielding, and the corresponding equivalent circuit models under an ideal shielding condition.

To develop RF noise shielding methods in miniaturized devices for low noise RF CMOS design, two different shielding schemes were implemented using 0.13μm BEOL (Back-End-of-Line) process with 8 layers of Cu and FSG as IMD (Inter-Metal Dielectric). G-pads for grounding were constructed with stacked metals from the bottom (M1) to the top (M8). S-pads for signal supply were built from M2 to M8, i.e. stacked metals excluding M1. The preserved M1 is employed as the noise shielding plate with two different coverage areas deployed under the TML and pad, defined as TML shielding and pad shielding. Note that TML connecting DUT (device under test) to S-pad is composed of M8. Fig. 1 illustrates the 3D structures for DUT, GSG pads, TML, and the proposed shielding schemes. Fig.1(a) is a standard structure without shielding and the other two adopting TML and pad shielding are shown in Fig.1(b) and (c) respectively. Following the test structures, equivalent circuit models adapted to two shielding schemes can be easily developed based on our original lossy substrate model in Fig.1(a). For an ideal shielding, the substrate loss can be eliminated and then the substrate RLC networks (R_{Si}, C_{Si}, L_{Si}, and C_P) under the TML or pad can be removed to leave a simple capacitor, as shown in Fig.1(b) and (c).

The definition of lossy substrate model parameters and extraction method can be referred to our original work [6-7]. The inductance L_{Si} introduced in the substrate networks of our model is a key parameter facilitating accurate simulation of substrate loss and noise propagation at very high frequency [7]. The referred ED model can explain the physics underlying L_{Si}, which involves contribution of magnetic vector potential in the electric field [5]. A perfect shielding can eliminate substrate loss and remove substrate networks under the pad and TML. Then, the original lossy substrate model is reduced to a simple capacitor, such as C_{pad} and C_{ox} corresponding to pad and TML shielding. Note that C_{pad} and C_{ox} can be calculated from layout and process parameters to serve as the initial values. This simplified equivalent circuit can reduce the parameter extraction flow. The model parameters extracted in this reduced flow assuming an ideal shielding, act as an initial model for further optimization to ensure accuracy over extremely high frequency.

TABLE I
RLC model parameters of the extended lossy substrate models for four test structures with different shielding schemes

W4N6	Pad RLC model parameters						
Shielding	C_{pad} (fF)	C_{p1} (fF)	C_{si1} (fF)	L_{si1} (pH)	R_{si1} (Ω)	L_{tml} (pH)	C_c (fF)
X	60.54	84.17	234.2	10.44	230.9	46.71	1.50
TML (M1)	64.25	58.62	119.6	211.4	259.4	18.92	0.58
Pad (M1)	161.1	x	x	x	x	20.92	0.70
	C_{ox} (fF)	C_{p2} (fF)	C_{si2} (fF)	L_{si2} (pH)	R_{si2} (Ω)	R_{tml} (Ω)	
X	21.63	1.106	34.94	65	429.7	0.2	
TML (M1)	29.75	21.61	45.2	248.2	207.5	0.19	
Pad (M1)	22.31	59.66	53.53	744.7	136.9	0.199	

Table 1 summarizes a full set of model parameters extracted through an optimal fitting to the measured S-parameters up to 50 GHz. The results indicate that pad shielding can fully eliminate substrate network under the pad but TML shielding cannot. It suggests that substrate loss is dominated by coupling through the pads in the specified GSG pad topology (M2~M8), and then pad shielding enables a more effective isolation against substrate loss compared with TML shielding. Note that pad shielding leads to a dramatic increase of C_{pad} by around 2.5 times and may degrade high frequency performance due to the added parasitic capacitance. Fig. 2 presents open pad S-parameters over a broadband of 50 GHz, and a good agreement between measurement and simulation using the optimized lossy substrate models adapted to various shielding schemes. The standard structure without shielding indicates a dramatic fall-off in mag(S_{11},S_{22}) with increasing frequency, which reveals a significant substrate loss. TML shielding has very minor effect and demonstrates similar results. On the other hand, pad shielding can recover mag(S_{11},S_{22}) to near a constant independent of frequency and approaching unity, but phase(S_{11},S_{22}) toward more negative. The former one indicates an effective suppression of substrate loss and the later one

reveals an increase of capacitance consistently correlated to increase of C_{pad}.

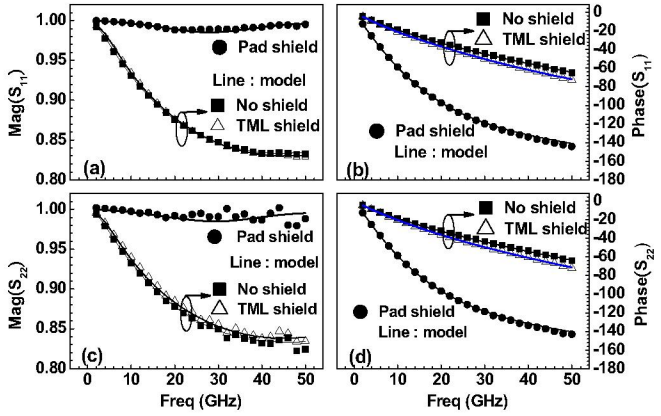

Fig.2 Open pad S parameters for three test structures with different shielding methods (no, TML and pad shielding). A comparison between measurement and simulation by extended lossy substrate models over wide frequency up to 50 GHz (a) mag(S_{11}) (b) phase(S_{11}) (c) mag(S_{22}) (d) phase(S_{22})

III. Noise Shielding Effect on High Frequency Performance

The extended lossy substrate models proven for open pads adopting specified shielding schemes were integrated with intrinsic MOSFET at gate/drain (port-1/port-2) for a two-port network circuit simulation to identify the impact on high frequency and noise characteristics [6-7]. Note that an extensive calibration has been done on the intrinsic MOSFET models in terms of V_T, mobility, velocity saturation, CLM, DIBL, overlap and fringing capacitances to realize a good match with measured I-V and C-V characteristics for 100 nm nMOS (not shown for brevity).

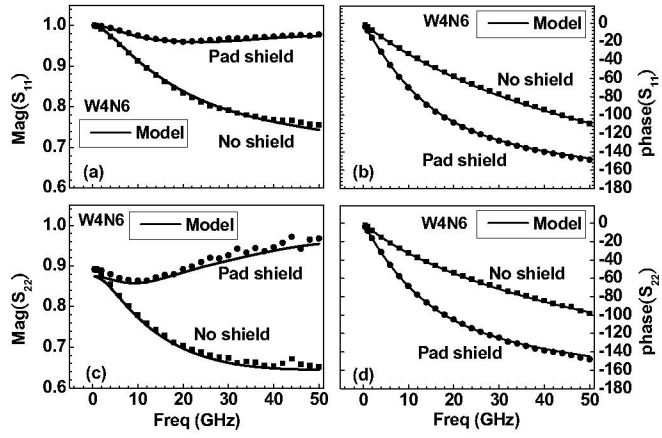

Fig. 3 100 nm nMOS (W/N=4μm/6) S parameters for two test structures (no and pad shielding). A comparison between measurement and simulation by extended lossy substrate models over wide frequency up to 50 GHz (a) mag(S_{11}) (b) phase(S_{11}) (c) mag(S_{22}) (d) phase(S_{22})

The high frequency accuracy is validated by a satisfactory fitting to the measured S-parameters up to 50 GHz, as shown in Fig.3 for a standard one without shielding and another one with pad shielding. Again, the apparent drop of mag(S_{11},S_{22}) with increasing frequency due to substrate loss, revealed by the standard structure without shielding can be recovered in devices with pad shielding. However, the increase in negative phase suggests additional parasitic capacitances and a potential impact on high frequency performance. Fig. 4 indicates the cut-off frequency f_T corresponding to three test structures and the dramatic degradation suffered by those with pad shielding. The two-port network circuit simulation using the proven lossy substrate models can consistently predict the degradation, shown in Fig. 4(a). The impact considered due to parasitic capacitances introduced from shielding plate (M1) is proven by an analytical expression of f_T, given as $g_m/2\pi(C_{gg}^2-C_{gd}^2)^{1/2}$ and a good match with that extracted from unit current gain, i.e. $|H_{21}|=1$, shown in Fig. 4(b).

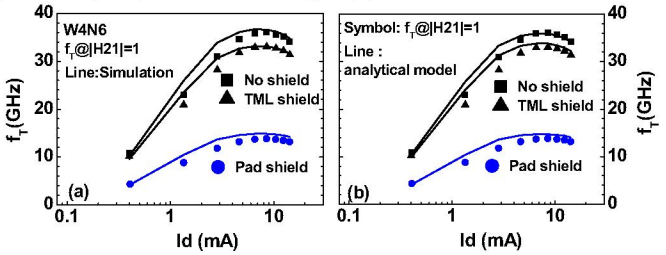

Fig. 4 100 nm nMOS (W/N=4μm/6) measured and simulated f_T for three test structures with different shielding schemes (a) f_T extracted from $|H_{21}|=1$ (b) f_T extracted at $|H_{21}|=1$ and calculated by analytical model $f_T=g_m/2\pi(C_{gg}^2-C_{gd}^2)^{1/2}$

IV. Noise Shielding Effect on RF Noise Parameters

The influence of shielding structures on RF noise is of our major focus. Four noise parameters (NF_{min}, R_n, $Re(Y_{opt})$, $Im(Y_{opt})$) were measured by ATN-NP5B under fixed V_{gs}(0.8V for max. g_m) and sweeping frequency to 18 GHz. Fig. 5 exhibits four noise parameters measured from 100 nm nMOS in two port test structure with various shielding schemes in Fig.1(a)~(c). The results indicate an effective NF_{min} suppression of around 1.8/2.05 dB at 10/18 GHz realized by pad shielding but very minor effect from TML shielding. It can be understood from shielding effect on S-parameters demonstrated in Fig.2 that substrate loss can be effectively eliminated by pad shielding but not for TML shielding. The reduction of $Re(Y_{opt})$ in Fig.5(c) makes a major contribution to NF_{min} suppression whereas R_n keeps nearly the same. The results infer an important insight that R_n is a parameter representing intrinsic device property (g_m, g_{do}, and R_g) independent of substrate loss and shielding effect. On the other hand, $Re(Y_{opt})$ closely reflects excess noises introduced from the lossy substrate and can be reduced through an effective shielding against the substrate coupling. $Im(Y_{opt})$ is one more important noise parameter, which performs an optimal matching to the source admittance at the input of DUT. The substantial increase of $Im(Y_{opt})$ (inductive mode) in test structures adopting pad shielding is realized through a tuner in ATN-NP5B to compensate for additional parasitic capacitance introduced by shielding plate. In this way, the degradation of f_T identified from DUT with shielding (Fig.4), due to added parasitic capacitance can be recovered through

an optimal admittance compensation enabled by $Im(Y_{opt})$, and then NF_{min} can be achieved corresponding to the recovered f_T and an expression of noise parameters in a noisy two-port network given by (1)-(2).

$$F = F_{min} + \frac{R_n}{G_S}|Y_S - Y_{opt}|^2 \quad (1)$$

$$F_{min} = F(Y_S = Y_{opt}),\ NF_{min} = 10 \times \log(F_{min}) \quad (2)$$

Regarding NF_{50}, the noise figure normally used in the practice of RF circuit design reveals an interesting result in shielding effect. Fig. 6 demonstrates a significant increase of NF_{50} corresponding to pad shielding that is going a direction opposite to what NF_{min} behaves. The adverse effect on NF_{50} from shielding is considered due to lack of admittance matching for compensating excess capacitances introduced by shielding plate. The proposed mechanism is supported by a consistent correlation with the degradation of f_T shown in Fig. 6(a). The dramatic drop of f_T incurred by shielding can explain the increase of NF_{50} accelerated at higher frequency. The result provides an important guideline in RF circuit design that an appropriately selected inductor is indispensable to realize compensation for parasitic capacitances, which is particularly critical for low noise design incorporating shielding schemes.

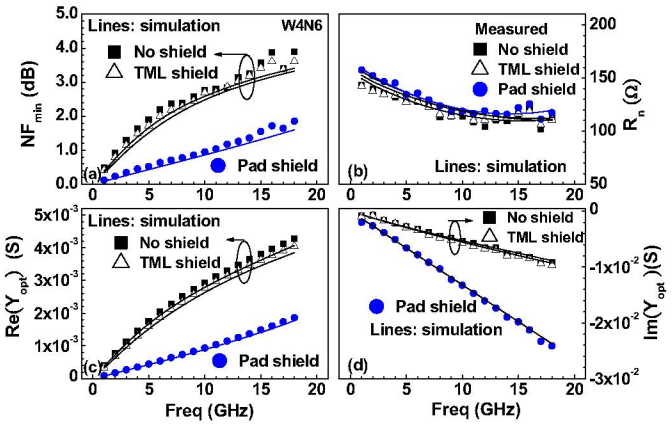

Fig. 5 100 nm nMOS (W/N=4μm/6) noise simulation and measurement for three test structures with different shielding schemes (no, TML, and pad shielding) (a) NF_{min} (b) R_n (c) $Re(Y_{opt})$ (d) $Im(Y_{opt})$

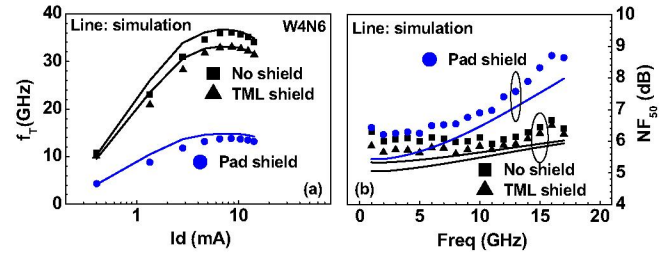

Fig. 6 100 nm nMOS (W/N=4μm/6) f_T before de-embedding and NF_{50} for three test structures with different shielding schemes (a) f_T (b) NF_{50}. Simulation (lines) can consistently predict measurement.

Note that noise simulation based on an improved thermal noise model (a replacement of default noise model in BSIM3) and the proven lossy substrate model can accurately predict the measured noise parameters. The major features incorporated in the improved noise model are short channel effects (velocity saturation, CLM, and carrier heating), substrate resistance induced potential fluctuation effect in drain current noise, and gate resistance induced excess noises in both drain and gate current noises.

V. Conclusion

RF noise shielding methods have been implemented and demonstrated an effective suppression of NF_{min} in 100 nm MOSFETs. A lossy substrate model incorporating inductive impedances in the substrate network can accurately predict substrate loss effect over extremely high frequency up to 50 GHz and the impact on noise parameters. The extended lossy substrate model adapted to noise shielding schemes proves the noise reduction due to elimination of substrate loss through the removal of substrate RLC network from the original one without shielding. The adverse effect on NF_{50} from shielding reveals an impact from the introduced excess capacitances and suggests an appropriate compensation required for RF circuit design. The proposed noise shielding methods and lossy substrate models with proven broadband accuracy for various shielding schemes can facilitate low noise RF CMOS design.

Acknowledgment

This work was supported in part by NSC under Grant NSC96-2221-E009-186. Also, the authors acknowledge the support from NDL CiC for test chip fabrication and RF Lab. for measurement.

References

[1] S. Bronckers, et al., in IEEE RFIC Symp. Proceedings, 2007, pp.753-756
[2] S. Wane, et al., in 2004 IEEE RFIC Symp. Digest, pp.179-182
[3] *J. C. Guo*, et al. in Symp. on VLSI Tech. Dig., June, Japan, 2003, p.39-40
[4] J. T. Colvin, et al. in IEEE BCTM Conference Proceeding, 1998, pp.109-112
[5] G. Manetas, et al. IEEE Trans. on Electromagnetic Compatibility, vol.49, no. pp.577-584, 2007
[6] Jyh-Chyurn Guo, et al., IEEE T-MTT, vol.54, pp.3975-3985 Nov. 2006
[7] Jyh-Chyurn Guo, et al., IEEE T-ED, vol. 53, pp.339-347, Feb. 2006
[8] J. C. Guo, et al., in 2006 RFIC Symp. Digest, pp.349-352
[9] J. C. Guo, et al. in 2007 RFIC Symp. Digest, pp.299-302