Optical and Electrical Properties of GaN-Based Light Emitting Diodes Grown on Micro- and Nano-Scale Patterned Si Substrate

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***Abstract*— We investigate the optical and electrical characteristics of the GaN-based light emitting diodes (LEDs) grown on micro- and nano-scale patterned silicon substrate (MPLEDs and NPLEDs). The transmission electron microscopy images reveal the suppression of threading dislocation density in InGaN/GaN structure on nano-pattern substrate due to nano-scale epitaxial lateral overgrowth. The plan-view and cross-section cathodo luminescence mappings show less defective and more homogeneous active quantum-well region growth on nano-porous substrates. From temperature-dependent photoluminescence (PL) and low temperature time-resolved PL measurement, NPLEDs have better carrier confinement and higher radiative recombination rate than MPLEDs. In terms of device performance, NPLEDs exhibit smaller electroluminescence peak wavelength blue shift, lower reverse leakage current and decrease in efficiency droop when compared with the MPLEDs. These results suggest the feasibility of using NPSi for the growth of high quality and power LEDs on Si substrates.**

***Index Terms*— Light emitting diodes, metal-organic chemical vapor deposition, nano-scale epitaxial lateral overgrowth, silicon substrate.**

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I. Introduction

The wide band gap GaN-based semiconductors have received enormous attention for various applications, such as short-haul optical communication, traffic and signal lights, back lights for liquid-crystal displays, and indoor/outdoor lightings. Typically, GaN-based light emitting diodes (LEDs) were grown on sapphire or SiC substrate by heteroepitaxial techniques in a metal-organic chemical vapor deposition (MOCVD) system [1]–[3]. However, the low thermal and electrical conductivities make sapphire less perfect as a substrate for the GaN epilayers, meanwhile the high price and mechanical defects hinder SiC substrate's acceptability in the LED market. Silicon has been considered as an alternative substrate material due to its low manufacturing cost, availability of large size wafers, and good thermal and electrical conductivities. Thus, many efforts have been dedicated to the realization of GaN based LEDs on Si substrates [4]–[8]. Even though good progress has been made, there are still several problems when using Si substrate for GaN epitaxial layers. The large lattice mismatch between GaN and Si (almost 17%) leads to high threading dislocation densities (TDDs) (around $10^8 - 10^{10}$ cm^{-2}) in the subsequent GaN epilayers. The other major problem is the thermal expansion coefficient difference (56%) between two materials, which induces a high tensile stress during the thermal cycling in MOCVD and often results in cracks and damages of epilayers [9]. To reduce the density of cracks and threading dislocations of GaN grown on Si, a number of approaches have been reported, such as using AlN multilayer combined with graded AlGaN layer as buffer [10], epitaxial lateral overgrowth of GaN on micro-patterned Si [11], and nano heteroepitaxial (NHE) lateral overgrowth of GaN on nanopore array Si [12], etc.. These methods effectively reduce the tensile stress and thus the crystal quality of GaN was greatly improved. Recently, our co-workers reported fabrication of GaN-based device structure on a nano-scale patterned silicon substrate [13] that shows significant improvement on reduction of TDDs, surface morphology and light emission. In the mean time, the optical and electrical properties of InGaN/GaN MQWs grown on these patterned silicon substrates have not been fully studied yet. In this paper, we examine various optical and electrical characteristics of GaN based LEDs grown on micro and nano-scale patterned

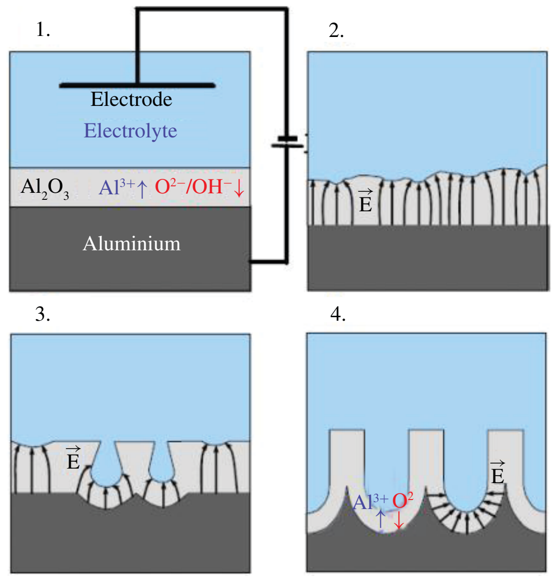


Fig. 1. Schematic diagram of pore formation at the beginning of the anodization.

Si substrates (MPLEDs and NPLEDs), and the experimental results can lead us to believe that NPLED is in general superior to its micro-scale counterpart.

II. Experiments

The micro-scale pattern Si (MPSi) substrate was prepared into 340μm $\times$ 340μm square islands on a 2-inch silicon substrate. These islands are separated by 3μm deep and 20μm wide trenches, in the $\langle 1\bar{1}0\rangle$ and $\langle 11\bar{2}\rangle$ directions, and were patterned by an STS inductively coupled plasma-reactive ion etching (ICP-RIE) system on 2-inch Si substrate. The self-ordered anodized aluminum oxide (AAO) procedures are depicted in Fig. 1. Firstly, a 500 Å thick SiO_2 film acting as the isolation layer was formed by thermal oxidation on a 2-inch Si (111) substrate. After that, 500 Å Ti and 3500 Å Al were deposited on it one by one using an AST electron-beam evaporator. The Ti improved the adhesion of the Al layer and promoted the uniformity of the porous alumina in the anodization step. The procedure of anodization can be summarized in the following four steps [13], [14]: first we deposit a non-conductive oxide layer and submerge the wafer into the electrolyte. Second, due to the inherent roughness, the electric field will locally concentrate at the high curvature points (Step 2). This local high field leads to a field-enhanced or/and temperature-enhanced dissolution of formed oxide, and thus, pores grow with the gradually dissolved alumina (Step 3). When the formation and dissolving of alumina reach an equilibrium state, a stable growth of pores can be realized, as shown in step 4.

Finally after the alumina nano-particles were formed, the oxide and then the underneath semiconductor layer can be removed by generic etching process (as shown in Fig. 2). In general, there are some parameters influencing the self-ordered anodized aluminum oxide (AAO), such as the anodic voltage, type and concentration of electrolyte, temperature, etc. [15] Among these factors, the anodic voltage is one of the most important factors for adjusting inter-pore distance. It is reported that the inter-pore distance was proportional to the anodic voltage, and could get the following relation [14],

$$2.5(\mathrm{nm/V})\ U \leq \mathrm{Dint} \leq 2.8(\mathrm{nm/V})\ U \qquad (1)$$

[16], [17] where Dint is the inter-pore distance, and U is the applied voltage.

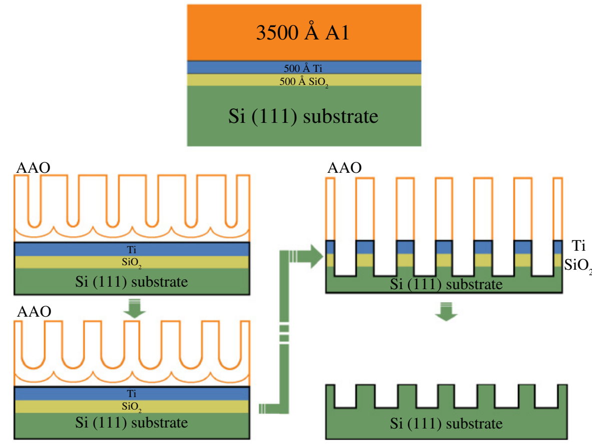


Fig. 2. Schematic diagram for preparing the porous Si substrate.

TABLE I
SUBSTRATES USED FOR GROWING GaN LAYERS

Substrate	Diameter (nm)	Spacing (nm)	Depth (μm)
A-1	200	100	1
A-2	120	150	1
A-3	120	150	0.25

The aforementioned equation (1) can served as a baseline for the process. However, in different material system, there should be one or more optimal conditions for the subsequent material quality. In this work, several designs were carried out to find out the optimized processes, and we summarize the physical characteristics in Table 1. Their outcomes of epitaxial layer quality can be visually distinguished from Fig. 3(a) to 3(c). When the size of the pore is too large, the coalescence of GaN layer can not be fully developed due to large pore diameter to mesa width ratio. If the depth of the pore is too large, the surface morphology will also be affected badly. We choose the condition in Fig. 3(c) as the final template for NPLED because it can deliver the best quality of the material. In addition to the anodic voltage and timing control, the common condition of anodization electrolyte was at 6 °C in 0.3M phosphoric acid for 30min. After anodization, self-assembled AAO nano arrays were uniformly distributed on the Si surface. By ICP etching, the AAO pattern was transferred to the Si substrate. The AAO mask was then removed by wet etching.

When all AAO steps were carried out successfully, nano-pore arrays were uniformly distributed on the entire 2-inch Si substrate with an average nano-pore diameter of 150 nm, inter-pore distance of 120 nm, and an etched depth of 250 nm. In the next step, LED structures with $In_{0.08}Ga_{0.92}N/GaN$ MQWs were grown on this nano-patterned substrate by MOCVD in

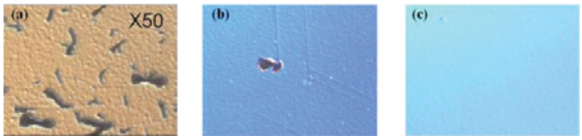


Fig. 3. Opticalmicroscope of GaN layer grown on substrate (a), (b), and (c).

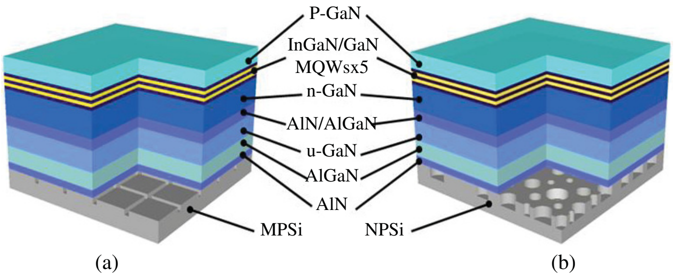


Fig. 4. Schematic of GaN-based LED structures grown on (a) MPSi and (b) NPSi.

an Aixtron 2000HT system. The epitaxial structure of the GaN-based LED overgrowth on MPSi and NPSi substrate is depicted in Fig. 4. Detailed substrate preparation and growth procedure for LED on MPSi and NPSi substrate were reported elsewhere [18], [19].

After the InGaN/GaN structures were grown, we performed standard LED lithographic process, metallization, and etch procedure in order to define device mesa and make p/n contacts of the LED layers. Once the device fabrication is finished, we engaged four different types of measurements: cathodo luminescence (CL), photoluminescence (PL), time-resolved photoluminescence (TRPL) and electroluminescence (EL). The spatially resolved CL imaging was obtained by scanning electron microscope (JEOL-7000F SEM system) with a fixed viewing scale. The temperature dependent PL measurements were done by a 325 nm He-Cd laser at 35 mW excitation power. Low temperature TRPL measurements were performed at 10 K using time-correlated single-photon counting and a pulsed GaN diode laser operating at a wavelength of 396 nm as the excitation source. In the EL measurement system, the current source is Kiethley 238, and the best measurement resolution at 1 nA injection could reach 10 fA with a accuracy of 0.3%. We can perform a serious of current-voltage measurement and data storage by Lab View human-machine control interface. Finally a generic device LIV measurement by the standard probe station and Kiethley current source will demonstrate superior power output and efficient droop in our NPLED device.

III. Results and Discussion

First step to compare these two material growth methods is to check their material quality. In order to analyze the detailed epitaxial layer quality, we used TEM to compare the cross section between two types of devices in Fig. 5. A comparison of Fig. 5(a) and 5(b) shows that the dislocation density in the NPSi sample is reduced much more than that of MPSi's. The TDDs for MPSi is estimated to be 2.5×10^{10} cm^{-2} at the bottom of the n-GaN layer, and it decreases to 4.6×10^{9} cm^{-2} at the top of the n-GaN layer and 6.2×10^{8} cm^{-2} in the p-GaN

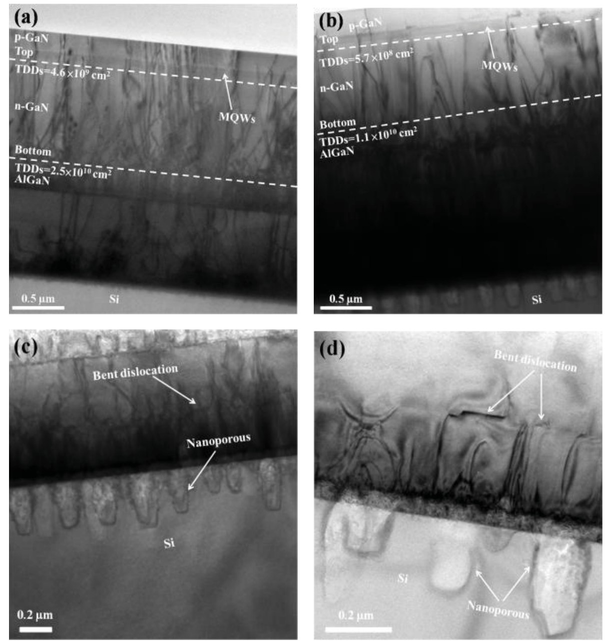


Fig. 5. TEM images of LEDs grown on (a) MPSi and (b) NPSi; (c) and (d) region of between AlGaN layer and Si substrate for NPSi using $g = (0002)$.

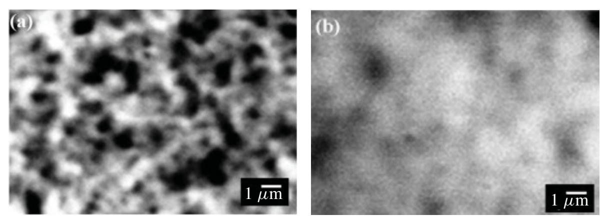
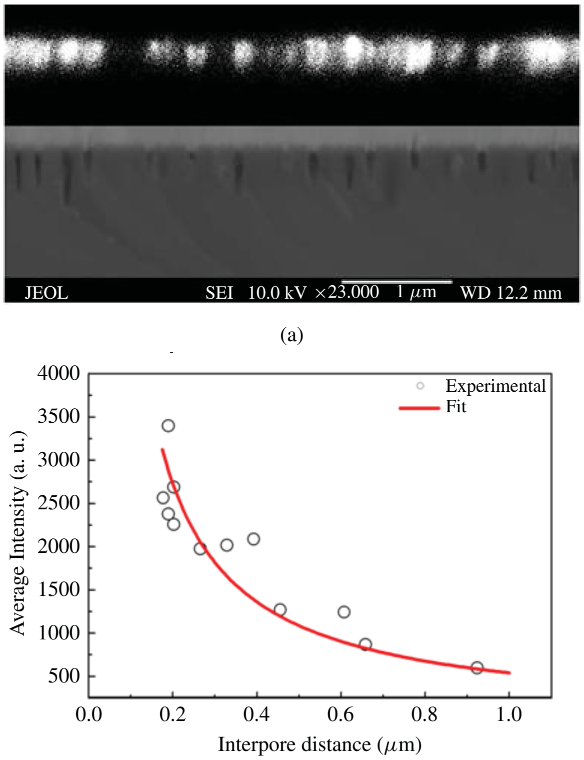


Fig. 6. Top view CL images on samples of energy for (a) micro-scale and (b) nano-scale pattered Si substrate.

region. On the other hand, for the epilayer grown on NPSi, fewer dislocations are observable within the range of view. As shown in Fig. 5(b), the TDDs at the bottom of the n-GaN layer is about 1.1×10^{10} cm^{-2}; however, the TDDs at the top of the n-GaN layer drop down to 5.7×10^{8} cm^{-2}, and it is only 8.8×10^{7} cm^{-2} in the p-GaN region. The reduction of TDDs NPSi over MPSi is about 10 times. Fig. 5(c) and 5(d) are TEM images are taken at the interface of epilayer/NPSi. As can be seen in Fig. 5(c), there are many dislocations bent and terminated in AlGaN layer or near the epilayer/NPSi interface. As a result, the density of TDDs in the subsequent quantum well region was much lower.

Next, we will examine our results by CL. CL is a very important technique when we need non-invasive assessment of crystal quality. Fig. 6(a) and 6(b) display the plan-view CL emission images with a 10 kV accelerating voltage at room temperature. At first glance, MPLED showed more "dead zone" or black spots than NPLED. These dark areas in the CL images are regions where minority carriers get consumed by dislocations due to high non radiative recombination velocity [20]. The other feature we would like to point out is that the emission intensity of MPLED is less uniform than NPLED's. This was mainly due to indium composition fluctuation and the



(b)

Fig. 7. (a) Cross section CL intensity at nano-scale patterned Si/GaN interface. (b) Average intensity between silicon holes against interpore distance.

phase separation [21], [22]. These CL images suggest that the pitch between the etched silicon holes might play an important role since the nano-patterned sample looks much better. To further investigate how the pitch of nano-patterns affects the photon emission efficiency, we cleaved through nano-porous wafers and performed the cross section CL measurement.

The upper half of Fig. 7(a) shows the cross section CL intensity of NPLEDs' quantum well region, and it is taken at the same horizontal location aligned to the nano-scale patterned Si/GaN substrate underneath (bottom half of Fig. 7(a)). We noticed that CL intensity is much stronger when etched silicon holes are closer. To quantitatively evaluate this observation, we plot the average intensity between silicon holes against interpore distances in Fig. 7(b). When the interpore distance reduced to 0.2μm (200nm) or less, the integrated luminescence intensity grows sharply. From previous research by Sugahara, et. al. [23], the CL efficiency (η) can be related to sample recombination behavior given by:

$$\eta = 1 - \left(\frac{2r_0}{L_d}\right)^2 - \frac{8}{L_d^2}\int_{r_0}^{\frac{L_d}{2}} r \exp\left(-\frac{r-r_0}{L_p}\right) dr \qquad (2)$$

where L_d is the mean dislocation distance, L is the diffusion length in InGaN, and r_0 is the radius in which non-radiative recombination consumes all carriers (the dark spot). If other material characteristics is the same and assume uniform excitation, the only factor that can affect the luminescent intensity is L_d, the mean dislocation distance. So when material has fewer defects, the efficiency is higher. From the trend of data, we can reasonably conclude that the higher density of nano-size interpore area bears less dislocation and thus tends to have strong light emission.

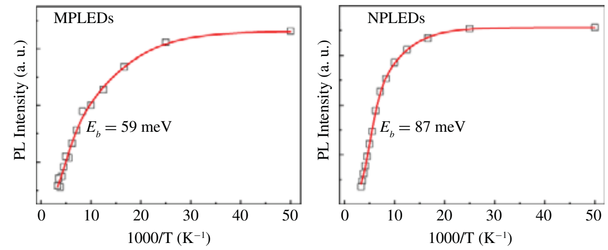


Fig. 8. (Color online.) PL intensity for (a) micro-scale and (b) nano-scale pattered Si substrate plotted as a function of 1000/T.

Just like CL can reveal the crystal quality, PL can let us find out the possible radiative recombination mechanism in the quantum well region. It has been shown that thermal quenching of PL intensity can be explained by carriers' thermal emission out of a confining potential with an activation energy correlated with the depth of the confining potential [24]. Therefore, it is expected that the deeper localization with better confinement should have larger activation energy. Fig. 8(a) and 8(b) display the temperature dependence of PL intensity fitted by Arrhenius equation as following [25]:

$$I(T) = \frac{I_0}{1 + A\exp\left(-\frac{E_a}{k_B T}\right) + B\exp\left(\frac{-E_b}{k_B T}\right)} \qquad (3)$$

where I(T) is the temperature-dependent PL intensity, I_0 is the PL intensity at 20 K, k_B is Boltzmann's constant, A and B are the rate constants, and E_a and E_b are the activation energies for two different nonradiative channels, which correspond to the low temperature and high temperature regions [26]. For high temperature region, thermal quenching can be fitted with activation energy (E_b) 59 and 87 meV for MPLEDs and NPLEDs, respectively. In particular, the activation energy for NPLEDs is 47.4 % higher than that for MPLEDs, leading to a minor overflow of carriers outside the InGaN MQW active region. The discrepancy should rise from either anisotropic distribution in the active region or mixture of thermionic emission from potential minimum to barrier. Based on above result, the PL-intensity improvement in the NPLEDs can be attributed to the stronger localization effects and better carrier confinement in $In_{0.08}Ga_{0.92}N$/GaN MQW active region [27].

Potential variation affects how easy the carrier can be confined, and the combining rate can be regarded as how fast the carriers can recombined. The information about carrier recombination rate can be obtained from decaying behavior of photoluminescence. The low temperature TRPL decay for both samples was shown in Fig. 9. Because the measurement was carried out at 10K, the influence of the nonradiative recombination process could be excluded [28]. The TRPL results can be fitted by a bi exponential decaying function: [29]

$$I(t) = I_1(0)\exp\left(-\frac{t}{\tau_1}\right) + I_2(0)\exp\left(-\frac{t}{\tau_2}\right) \qquad (4)$$

where I(t) is the PL intensity at time t; τ_1 and τ_2 represent the characteristic lifetimes of the carriers. The fast decay time

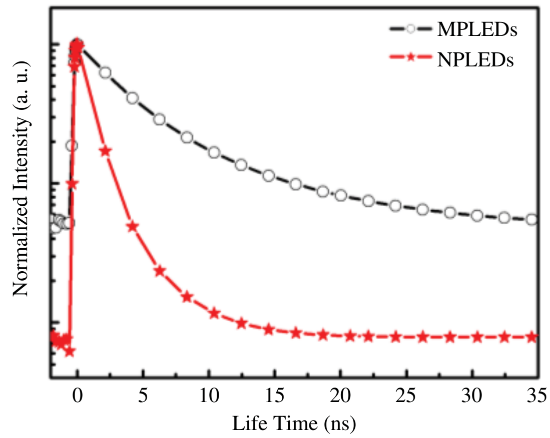


Fig. 9. Comparison of low-temperature TRPL between MPLEDs and NPLEDs.

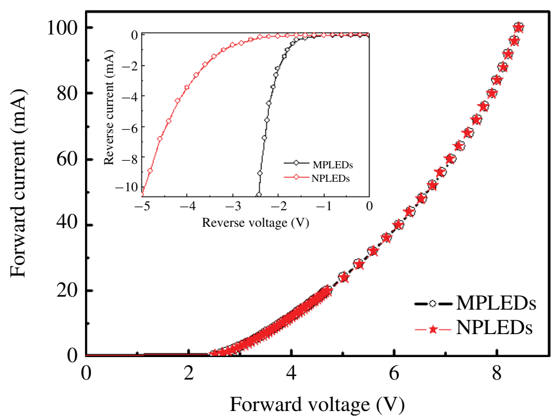


Fig. 10. Forward I–V characteristics of all fabricated LEDs, and the inset is reverse I–V characteristics of all fabricated LEDs.

constant (τ_1) usually represents the radiative recombination of excitons and the relaxation of QW excitons from free or extended states toward localized states [29], [30]. Our fitting shows $\tau_1 = 3.2$ and 1 ns for MPLEDs and NPLEDs, respectively. The slow decay time (τ_2) accounts for communication between localized states and localized excitons [29], [30]. The fitting shows $\tau_2 = 9.4$ and 3.2 ns for MPLEDs and NPLEDs, respectively. In both fast and slow constants, NPLEDs' lifetime is generally shorter than MPLEDs' at low temperature. S. Chichibu, et. al. reported the electron-hole pairs in the potential minima of QWs can be referred to as localized excitons, and the emission efficiency can still be enhanced even though the wave function overlap is weakened [31]. In the case of MPLEDs and NPLEDs, much higher radiative recombination rate observed in TRPL can be interpreted as direct evidence of stronger localized confinement in NPLEDs than MPLEDs, and also an indication of more efficient light-emitter.

The final trial of this nano-size template is to test the light emitting efficiency from the real device. LED devices with a chip size of 350 × 350 μm^2 were fabricated on both MPLEDs and NPLEDs. Fig. 10 shows the forward I-V characteristics of both samples. At 20 mA forward current, both samples exhibited diode voltages around 4.7 V. In addition, at the

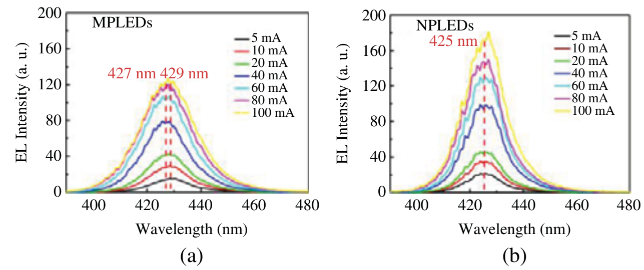


Fig. 11. EL spectra of (a) MPLEDs and (b) NPLEDs at different drive currents.

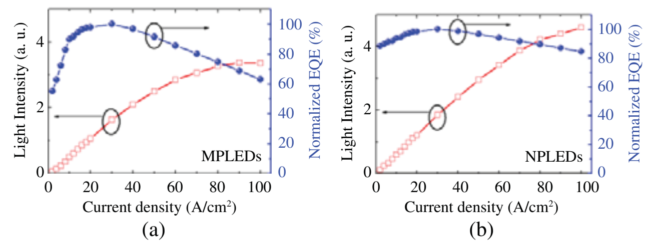


Fig. 12. Integrated EL intensity and normalized EQE as a function of forward current density for (a) MPLEDs and (b) NPLEDs, respectively.

reverse bias (shown in the insert plot of Fig. 10), the leakage current of the NPLEDs is smaller than MPLEDs. Several types of dislocations can contribute to the reverse-bias leakage current [32], and one of the most dominant type is the screw dislocation [32], [33]. The reduction of screw type dislocations can certainly help to reduce the reverse-bias current, and our measurement indicates a better crystal quality of LEDs grown on NPSi substrate, which confirms with TEM results.

Fig. 11 shows EL spectrums as a function of injection current for MPLEDs and NPLEDs. The emission peak wavelength of NPLEDs is slightly shorter than MPLEDs'. In our previous study, we performed Raman backscattering measurement at room temperature. The regular Raman shift of E_2 (High) in stress-free GaN layer is around 567.2 cm^{-1}. In this paper, the E_2 (High) shift is 565.4 cm^{-1} and 564.5 cm^{-1}, for samples on NPSi and on MPSi, respectively. The deviation of the E_2 (High) peaks from the intrinsic position is proportional to the residual tensile stress. For GaN, the E_2 (High) mode shifts linearly with stress in 2.9 cm^{-1}/GPa for biaxial stress. We can thus estimate the tensile stress in NPSi and MPSi are 0.62 GPa and 0.93 GPa, respectively. This indicates that the LEDs grown on NPSi exhibited lower strain than on MPSi. Therefore, the LEDs grown on NPSi possess a reduced QCSE. The related MPSi and NPSi Raman measurement results have been previously published by Dongmei Deng et. al. [18]. Moreover, we can see EL emission peak wavelength of MPLEDs exhibits blue shift from 429 nm to 427 nm with increasing drive current as shown in Fig. 11(a). However, we obtained almost unshifted EL peak with increasing injection current. This result indicates that the quantum confined stark effect (QCSE) does become weaker due to the strain relaxation in epitaxial layer overgrown on NPSi template [34].

Finally, Fig. 12 shows the light output intensity and normalized external quantum efficiency (EQE) as a function of forward current density for both samples. The light output-current curve of MPLEDs is linear under 20mA/cm^2. From this data, the light output of the MPLED shows an obvious soft increase of EQE, which is an indication of higher threading dislocation densities [35], and the roll-over current is much lower in MPLED. The data from NPLED, however, demonstrates good material quality with a reduced efficiency droop and much less soft increase in EQE.

However, it rolls over beyond 20mA/cm^2 with a reduced EQE. The EQE is decreased to 62% of its maximum value when the current density at 100mA/cm^2. In contrast, the NPLEDs exhibits 20% efficiency droop with increasing the injection current density to 100mA/cm^2. It can be attributed to reduced polarization field which also echoes to weaker QCSE under the circumstance of reduced strain in overgrown layers on NPSi template [36].

IV. Conclusion

In conclusion, the optical and electrical properties of LEDs grown on micro and nano-scale patterned Si substrate were investigated. We demonstrated a more homogeneous growth of InGaN/GaN active layers under this nano-scale template by plan-view and cross-section CL mapping. From temperature dependent PL and low temperature TRPL measurement, NPLEDs has better carrier confinement and higher radiative recombination rate than MPLEDs. On the actual device performance, NPLEDs exhibits smaller peak wavelength blue shift, lower reverse leakage current and decreases efficiency droop compared with the MPLEDs. The results suggest a weaker QCSE due to relaxation of strain in the epitaxial layers on nano-scale patterned substrate, which can be really useful for the next generation of large area, Si-based heteroepitaxy of GaN related optoelectronic devices.

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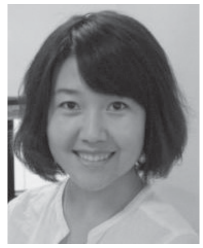

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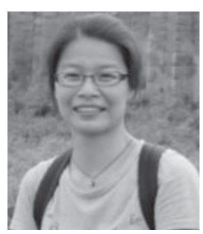

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