A Balanced Digital Phase Shifter by a Novel Switching-Mode Topology

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***Abstract*—A balanced digital phase shifter by a novel switching-mode topology is proposed. A 3-bit balanced digital phase shifter is given as an example, the working bandwidth of which is from 2.3 to 2.7 GHz. The proposed 3-bit balanced phase shifter comprises two balanced loaded-line phase shifters (90° and 45°) and six twist-line broadband 180° phase shifters. The balanced loaded-line digital phase shifter changes phases while the even- or odd-mode signal is excited. The 180° phase shifter controls the balanced signal to be even or odd mode. The commensurate transmission line filter is used as the biasing circuit.**

***Index Terms*—Balanced digital phase shifter, broadband 180° digital phase shifter, loaded-line phase shifter, switching mode, twist-line.**

I. Introduction

THE PHASE shifter is an important component in microwave systems and is widely used in many applications such as phase modulators, frequency up-converters, and phased array antenna systems. Phase shifters can be classified into analog phase shifter and digital phase shifter. The analog phase shifter generates continuous phase difference by corresponding continuous variation of the control signal, such as the voltage-controlled phase shifter, which is controlled by the varactor diode. The digital phase shifter discretizes the phase into predetermined phase states, and the user can change to different phase states by digitally controlling each phase-shifter bit.

The more bits of the digital phase shifter has, the more states of the phase the system can switch to. It is an important issue to switch to different states of the digital phase shifter accurately. There are many methods to realize the digital phase shifters. In [1]–[4], the microelectromechanical systems (MEMS) realize the switch of the phase shifter. References [5]–[7] use transistors as switches and equivalent the transistors as resistors or capacitors to realize the phase shifter. Much of the literature use p-i-n diodes to implement the digital phase shifter. The switch-path phase shifter uses the diodes to switch the signal between two different paths directly [8]–[11]. In [12] and [13], the reflective-type phase shifter is implemented by using the two biasing states of the diode. In [14] and [15], the diodes are used to switch the susceptance of the loaded-line phase shifter. Reference [16] and [17] realize the phase shifter by arranging diode switches to permit switching between low- and high-pass filters.

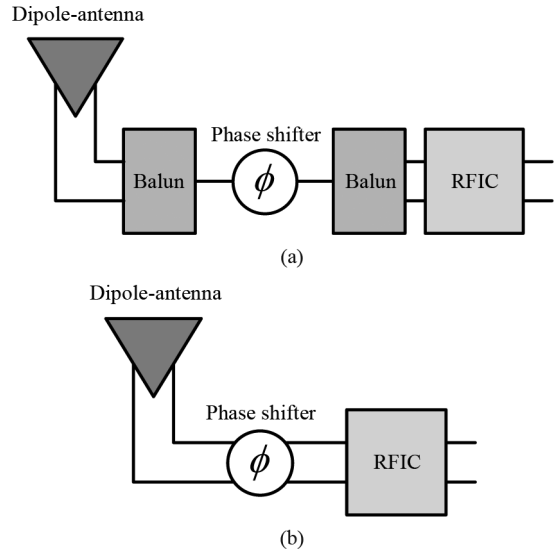

Fig. 1. Balanced system structure. (a) Single-ended phase shifter. (b) Balanced phase shifter.

A balanced circuit is important in today's microwave applications, such as antennas and RF integrated circuits (RFICs), because it has better immunity to electromagnetic (EM) interference. Due to this trend, there are more demands on balance passive circuits. Fig. 1(a) shows one element of a balanced phased-array system. For the balanced antenna and balanced RFIC, the single-ended phase shifter needs two baluns to transform the signals from balanced to single-ended and vice versa. However, a balanced phase shifter can connect the balanced antenna and balanced RFIC directly and reduce the circuit size and complexity, as shown in Fig. 1(b). There is some literature about the differential phase shifters [18], [19], but it is not suitable for the phased-array system. In [20], the 4-bit balanced active phase shifter is implemented by the vector sum method. However, the active components are unilateral, which makes it difficult to use as a reciprocal circuit in the transmit/receive (T/R) module.

In this paper, we propose a novel switching-mode topology to realize the multiple-bit balanced phase shifter. The concept of the single-bit phase shifter is shown in Fig. 2, which comprises the balanced phase-shifter element and the mode control element. The balanced phase-shifter element is with

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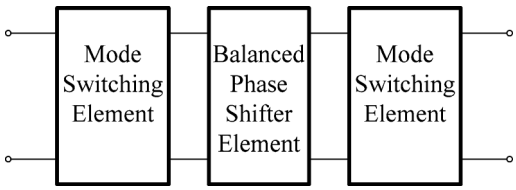

Fig. 2. Concept of single-bit balanced digital phase shifter.

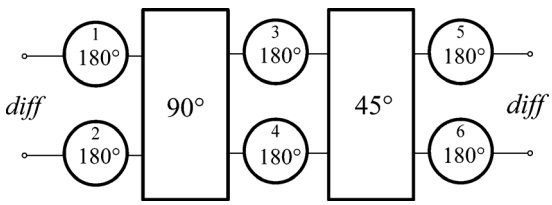

Fig. 3. 3-bit balanced digital phase shifter.

insertion phase difference between the even and odd modes. The mode switching element is used to switch the differential signal between the even and odd modes. A 3-bit balanced digital phase shifter is given as an example using the proposed concept. As shown in Fig. 3, it combines two balanced digital phase shifters and six broadband 180° digital phase shifters. The 180° digital phase shifters realize the mode switching elements. By switching between differential and common modes, the insertion phase can be switched to eight phasing states. To switch between differential and common mode accurately, we use the twist-line 180° digital phase shifter and design the commensurate line filter as a biasing circuit.

There are two benefits of the proposed circuit topology. First, the center balanced phase-shifter element in Fig. 2 is a passive circuit without control devices (p-i-n diodes in our example) that can be designed easily and accurately. Second, the only circuit including control devices is the 180° phase shifters in the mode switching element in Fig. 2 and they are identical in every phase-shifting bit.

II. Principle of Operation of the Proposed 3-bit Balanced Digital Phase Shifter

The proposed 3-bit balanced digital phase shifter is shown in Fig. 3. In Fig. 3, the 90° and 45° balanced phase shifters are operated with even- or odd-mode excitations that the insertion phase difference between even- and odd-mode signals are 90° and 45°, respectively. Now, placing six wideband 180° phase shifters between the 90° and 45° balanced phase shifters, as shown in the Fig. 3, the input signal of the 90° and 45° balanced phase shifters can be either differential or common mode by properly controlling the six 180° phase shifters. The phase of the output differential signal can then be digitally controlled with 45° steps.

Take the 45° phase-shifting state as an example. First, all of the six 180° phase shifters are set to state 0, which means 0° phase shift. When the input signal is differential, the input signal of the 90° and 45° balanced phase shifters would both be differential too. The phase of the output signal θ is the initial reference phase, as shown in Fig. 4(a).

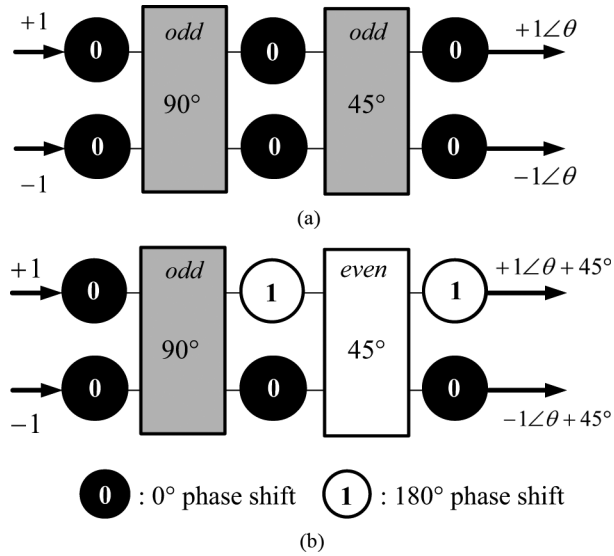

Fig. 4. Operation of the 3-bit balanced digital phase shifter. (a) Initial state. (b) State of 45°.

TABLE I
Truth Table of the 3-bit Balanced Digital Phase Shifter

	ϕ_1	ϕ_2	ϕ_3	ϕ_4	ϕ_5	ϕ_6	90°	45°
0°	0	0	0	0	0	0	Odd	Odd
45°	0	0	1	0	1	0	Odd	Even
90°	1	0	1	0	0	0	Even	Odd
135°	1	0	0	0	1	0	Even	Even
180°	0	0	0	0	1	1	Odd	Odd
225°	0	0	1	0	0	1	Odd	Even
270°	1	0	1	0	1	1	Even	Odd
315°	1	0	0	0	0	1	Even	Even

Next, change the third 180° phase shifter to state 1, which means 180° phase shift, as shown in Fig. 4(b). The input signal of the 90° phase shifter is differential mode, whereas the input signal of the 45° phase shifter is now changing from the differential mode to the common mode. The phase difference of the output signal would be 45° with respect to the initial state. The fifth 180° phase shifter is then set to state 1 to change the output signal from common mode back to the differential mode. Following the above step, the truth table of the 3-bit balanced digital phase shifter is shown in Table I. In theory, only $N+1$ 180° phase shifters are required where N is the bits number of the phase shifter. Here, for better phase and amplitude balance, we put six 180° phase shifters in our circuit. As one can see in Table I, ϕ_2 and ϕ_4 are never accessed. The working principle and the design of each circuit element in Fig. 3 are described in the following.

A. 45° Balanced Digital Phase Shifter

The 45° balanced loaded-line phase shifter is shown in Fig. 5. By controlling the input signal to be differential or common mode, the $\lambda/8$ transmission lines can be either short-circuited stubs, as shown in Fig. 5(a), or open-circuited stubs, as shown

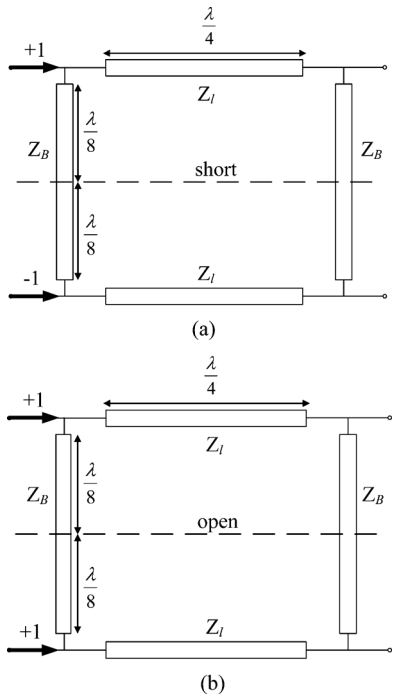

Fig. 5. 45° balanced digital loaded-line phase shifter. (a) Odd mode. (b) Even mode.

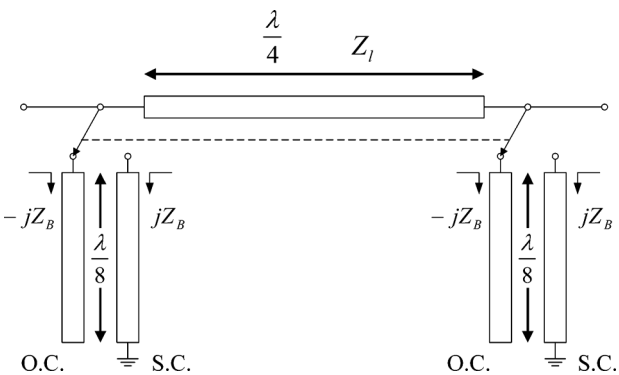

Fig. 6. Loaded-line phase shifter, where the switch is controlled by input signals as even and odd mode.

in Fig. 5(b). The equivalent half circuit of the proposed 45° balanced loaded-line phase shifter is shown in Fig. 6. The design of the loaded-line phase shifter is analyzed in [14].

A loaded transmission line and its equivalent circuit are shown in Fig. 7. There is a transmission line of electrical length θ_l and impedance Z_l connected with two switchable lumped elements of susceptance B_1 and B_2. The corresponding $ABCD$ matrix is

$$\begin{bmatrix} \mathrm{A} & \mathrm{B} \\ \mathrm{C} & \mathrm{D} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ jB_i & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_l & jZ_l \sin\theta_l \\ jY_l \sin\theta_l & \cos\theta_l \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jB_i & 1 \end{bmatrix} = \begin{bmatrix} (\cos\theta_l - B_i Z_l)\cos\theta_l & j(Z_l \sin\theta_l) \\ j(2B_i \cos\theta_l + Y_l \sin\theta_l - B_i^2 Z_l \sin\theta_l) & (\cos\theta_l - B_i Z_l) \end{bmatrix} \quad (1)$$

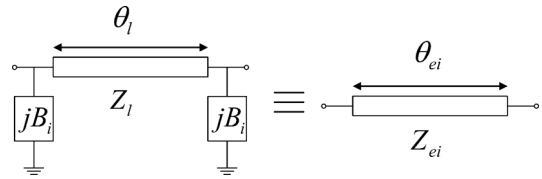

Fig. 7. Loaded transmission line connected with two susceptances and its equivalent transmission line.

TABLE II
CALCULATED VALUES OF THE 45° BALANCED DIGITAL PHASE SHIFTER

θ_l	Z_l	$\lvert B_i \rvert$	θ_{stub}	Z_{stub}
90°	45.9Ω	8.5×10^{-3}	45°	117.6Ω

where $i = 1$ or 2, which represents the two corresponding states.

The equivalent transmission line of electrical length of θ_{ei} and impedance Z_{ei} is shown in Fig. 7 with the $ABCD$ matrix of

$$\begin{bmatrix} \mathrm{A} & \mathrm{B} \\ \mathrm{C} & \mathrm{D} \end{bmatrix}_{\text{equivalent}} = \begin{bmatrix} \cos\theta_{ei} & jZ_{ei} \sin\theta_{ei} \\ jY_{ei} \sin\theta_{ei} & \cos\theta_{ei} \end{bmatrix}. \quad (2)$$

Equalizing each corresponding matrix element, we can then obtain

$$\cos\theta_{ei} = \cos\theta_l - B_i Z_l \sin\theta_l \quad (3)$$

$$Y_{ei} = Y_l \left[1 - (B_i Z_l)^2 + 2B_i Z_l \cot\theta_l\right]^{1/2}. \quad (4)$$

In our case, $B_1 = Z_B$, $B_2 = -Z_B$, and $\theta_l = 90°$, which implies $Y_{e1} = Y_{e2}$ and the two states are with good return loss. The phase difference $\Delta\phi$ of the two states can be obtained as

$$\theta_{e1} = \cos^{-1}(-Z_B Z_l) \quad (5)$$

$$\theta_{e2} = \cos^{-1}(Z_B Z_l) \quad (6)$$

$$\Delta\phi = \theta_{e2} - \theta_{e1} \quad (7)$$

where state 1 corresponds to odd mode and state 2 corresponds to even mode.

Applying (4)–(7), let $Z_e (= Y_e^{-1})$ be the port impedance of 50 Ω and $\Delta\phi = 45°$, the circuit parameters can be obtained as shown in Table II. The circuit can then be fine tuned from these initial values to have a broader bandwidth.

B. 90° Balanced Digital Phase Shifter

As the phase-shifting angle increases, the bandwidth of the above described loaded-line phase shifter decreases. To realize a 90° phase shifter with broader bandwidth, the loaded-line phase shifter with three shunt susceptances can be used. The 90° balanced phase shifter is shown in Fig. 8. The equivalent even- and odd-mode half-circuit can be presented as Fig. 9. Following the procedure in Section II-A and [14], the design equations are shown as

$$B_2 = \frac{2B_1}{(B_1 Z_0)^2 + 1} \quad (8)$$

$$\theta_{ei} = 180° + \tan^{-1}\left(\frac{2B_1 Z_0}{1 - (B_1 Z_0)^2}\right) \quad (9)$$

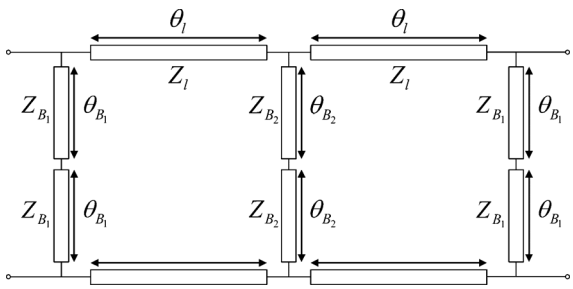

Fig. 8. 90° balanced digital phase shifter.

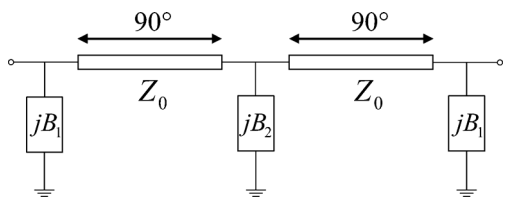

Fig. 9. Three-element loaded-line phase shifter.

TABLE III
CALCULATED VALUES OF THE 90° BALANCED DIGITAL PHASE SHIFTER

θ_0	Z_0	θ_{stub_1}	Z_{stub_1}	θ_{stub_2}	Z_{stub_2}
90°	50Ω	45°	120.7Ω	45°	71.0Ω

Fig. 10. Twist-line of balanced transmission line.

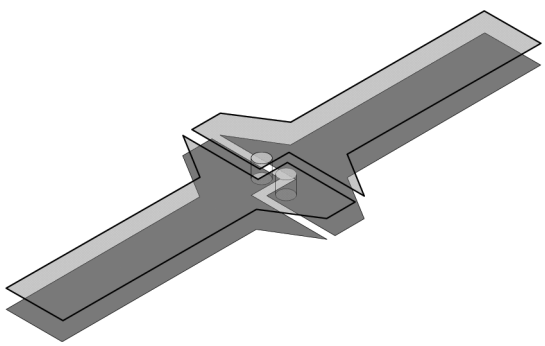

Fig. 11. Implementation of twist-line for DSPSL.

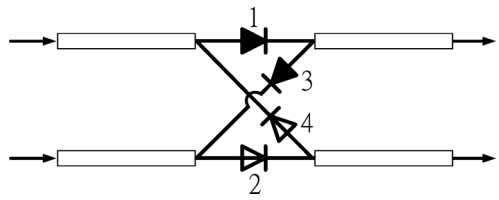

Fig. 12. Switchable twist-line with two pairs of diodes.

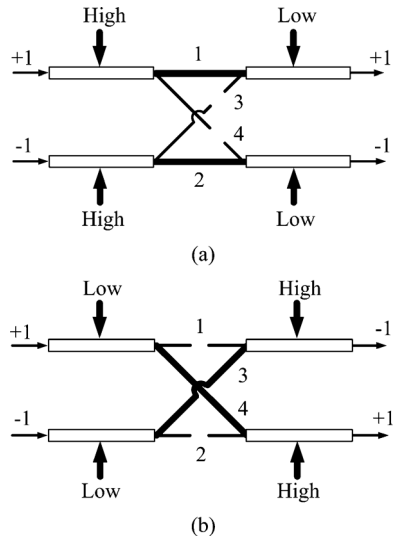

Fig. 13. Operation of the 180° digital phase shifter. (a) No 180° phase difference. (b) 180° phase difference.

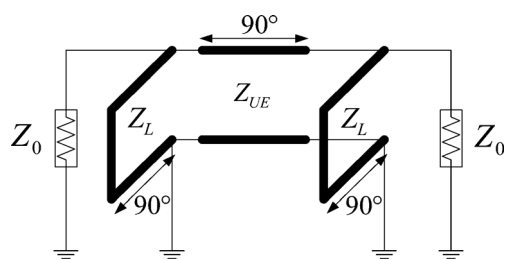

Fig. 14. Commensurate transmission-line filter.

TABLE IV
CALCULATED VALUES OF THE COMMENSURATE TRANSMISSION-LINE FILTER

Z_0	Z_{UE}	Z_L
50Ω	48.445Ω	105.175Ω

where θ_{ei}, $i = 1$, or 2 is the insertion phase of one of the two states. Since B_1 in (9) only changes the sign while changing the state, the phase difference of the even and odd mode should be

$$\Delta\phi = \theta_{e2} - \theta_{e1} = 2\tan^{-1}\left(\frac{2|B_1 Z_0|}{1-(B_1 Z_0)^2}\right). \qquad (10)$$

From(8) and (10), the element values are calculated as shown in Table III.

C. Wideband 180° Phase Shifter

The key considerations of the 180° phase shifter used here are the phase accuracy and insertion loss balance between the two states because both of these can cause mode conversion error. This means that when converting the input signal from the differential mode to the common mode through the 180° phase shifter, the output common-mode signal will be accompanied by a small amount of differential-mode signal if the above-described errors exist. The same situation occurs when converting the signal from the common mode to the differential mode. The purity of mode is important to the balanced 45° and 90° loaded-line phase shifters.

To deal with the above considerations, the twist-line phase inverter (or 180° phase shifter) is used [21], [22]. The twist-line 180° phase shifter is formed by twisting the signal and ground

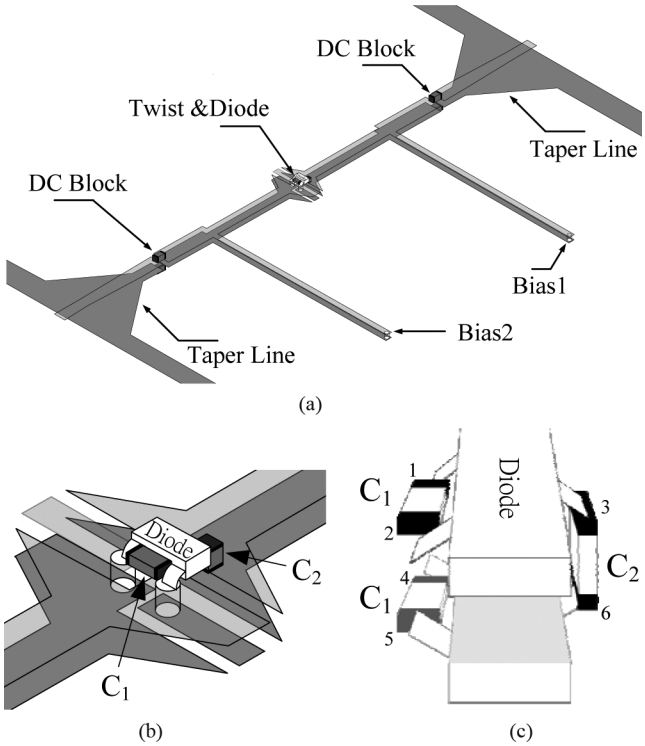

Fig. 15. Structure of the 180° digital phase shifter. (a) Total circuit. (b) Twist-line and diode. (c) Connection of diodes and capacitors.

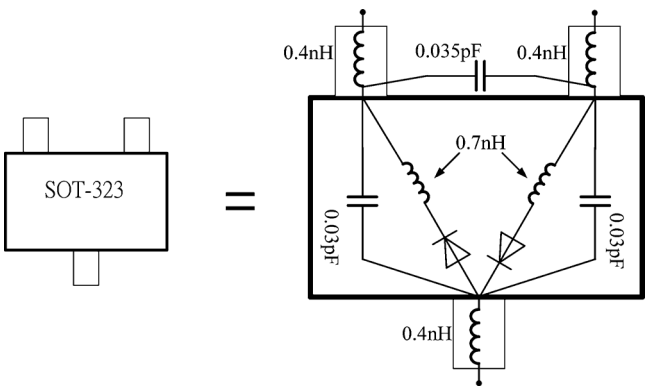

Fig. 16. Equivalent circuit of the package parasitics.

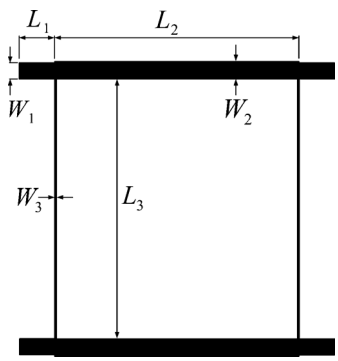

Fig. 17. Layout of the 45° balanced digital phase shifter.

TABLE V
PHYSICAL DIMENSION OF THE 45° BALANCED DIGITAL PHASE SHIFTER (IN MILLIMETERS)

W_1	L_1	W_2	L_2	W_3	L_3
1.118	2.540	1.194	17.831	0.152	19.101

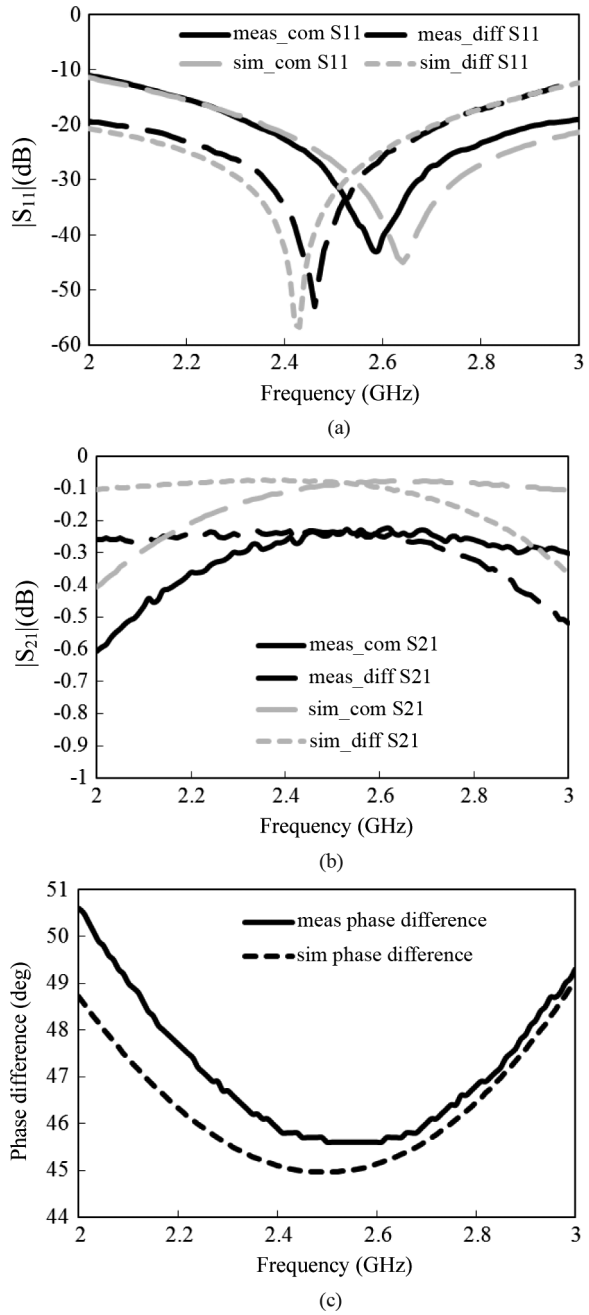

Fig. 18. Simulated and measured results of the 45° balanced digital phase shifter. (a) S_{11}. (b) S_{12}. (c) Phase difference.

of a balanced transmission line, as shown in Fig. 10. It is an ideal wideband 180° phase shifter. Fig. 11 shows the twist-line phase inverter realized by the double-sided parallel-strip lines (DSPSLs) [23], [24].

To make the twist-line switchable, a pair of series-T p-i-n diodes is placed on the twist-line portion of the circuit, as shown in Fig. 12. In Fig. 12, the two p-i-n diodes with empty filling (diodes 2 and 4) form a series-T, whereas the two with black filling (diode 1 and 3) form another series-T.

When the left side of the balanced transmission line is biased with positive voltage with respect to the right side, diodes 1 and 2 would be forward biased (as an RF short), whereas diodes 3 and 4 would be reverse biased (as an RF open). Therefore, the

TABLE VI
COMPARISON OF THE SIMULATED AND MEASURED 45° BALANCED DIGITAL PHASE SHIFTER

	Bandwidth	Insertion Loss	Maximum Phase Difference
Simulated	2.2GHz ~ 2.8GHz	0.09dB	1.5°
Measured	2.3GHz ~ 2.7GHz	0.25dB	1.5°

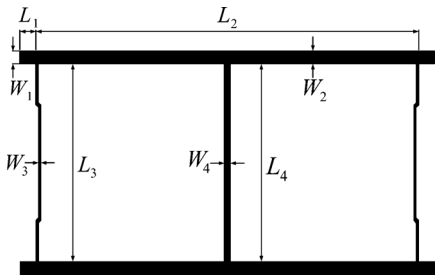

Fig. 19. Layout of the 90° balanced digital phase shifter.

TABLE VII
PHYSICAL DIMENSION OF THE 90° BALANCED DIGITAL PHASE SHIFTER (IN MILLIMETERS)

W_1	L_1	W_2	L_2	W_3	L_3	W_4	L_4
1.118	2.540	1.168	37.08	0.178	18.34	0.584	18.34

signal goes from the input to the output without twist, as shown in Fig. 13(a). Conversely, when the right side of the balanced transmission line is biased with positive voltage with respect to the left side, diodes 3 and 4 would be forward biased, whereas diodes 1 and 2 would be reverse biased. The signal going from the input to the output would be twisted, as shown in Fig. 13(b), and a 180° phase shift is obtained. The signal of each state will pass through a pair of forward-biased p-i-n diodes, which keeps the loss of two states equal.

To apply proper bias voltage to the p-i-n diodes, the commensurate line filter is used.

1) Commensurate Transmission-Line Filter: The commensurate transmission-line filter is formed by a transmission-line shunt connected with two short-circuited stubs at two ends, as shown in Fig. 14. All the transmission lines have an electrical length of 90° at center frequency f_0. With the user-defined specification, the impedance value of each transmission-line section can be synthesized exactly [25], [26]. Table IV shows the synthesized values of a commensurate line filter with a bandwidth from 2 to 3 GHz and a return loss of 30 dB.

The dc biasing circuit can be applied at the short end of the stubs. The filter is implemented by a DSPSL. The switchable twist-line is located at the center of the main line, as shown in Fig. 15(a). The switchable twist-line with four p-i-n diodes is depicted in Figs. 15(b) and 15(c), where the twist-line is cut and replaced by the p-i-n diodes. The four p-i-n diodes are realized by a pair of SOT-323 packaged series-T p-i-n diodes and soldered on the top and bottom sides of the circuit. In Fig. 15(b), only the series-T p-i-n diode on the top side of the circuit is depicted. The dc blocking capacitors of 2.2 pF are added at the

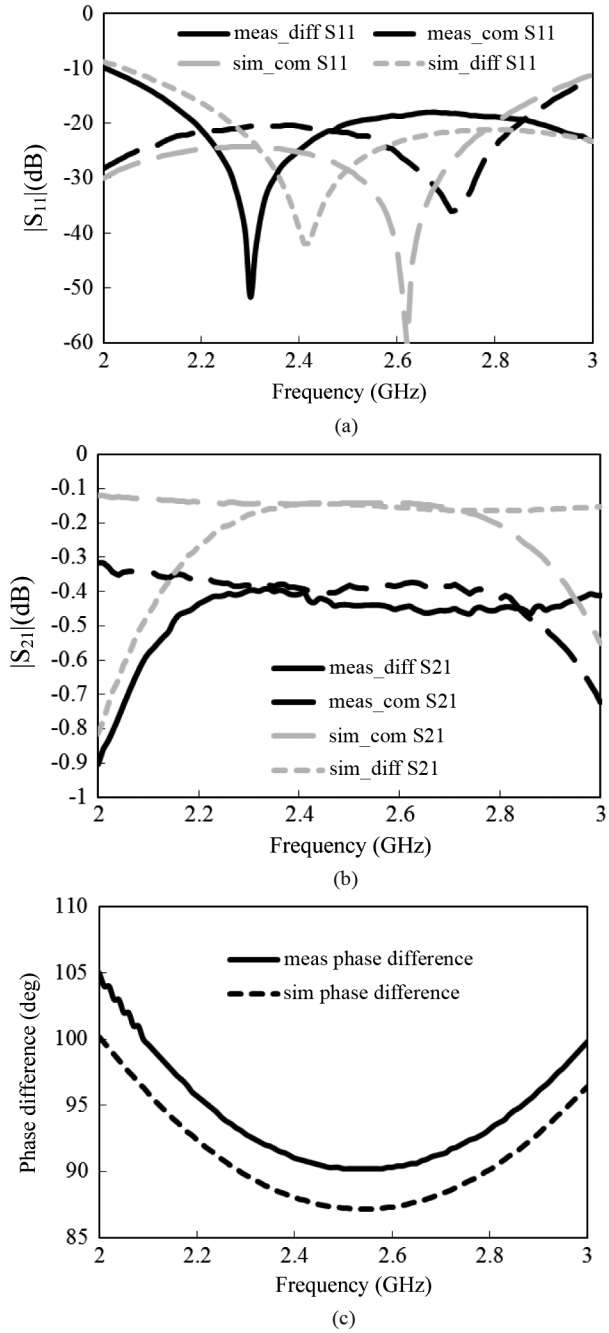

Fig. 20. Simulated and measured results of the 90° balanced digital phase shifter. (a) S_{11}. (b) S_{12}. (c) Phase difference.

TABLE VIII
COMPARISON OF THE SIMULATED AND MEASURED 90° BALANCED DIGITAL PHASE SHIFTER

	Bandwidth	Insertion Loss	Maximum Phase Difference
Simulated	2.3GHz ~ 2.7GHz	0.15dB	3°
Measured	2.3GHz ~ 2.7GHz	0.4dB	3°

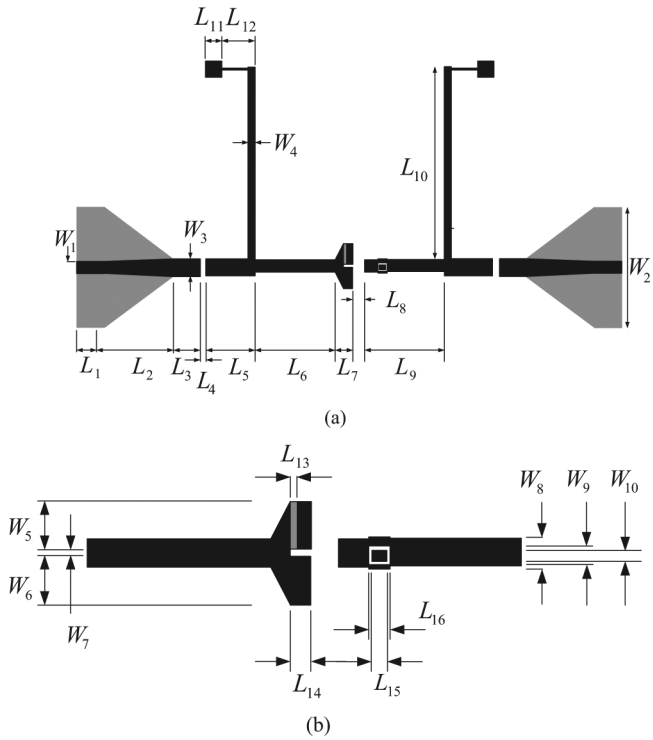

Fig. 21. Layout of the wideband 180° phase shifter.

TABLE IX
PHYSICAL DIMENSION OF THE WIDEBAND 180° DIGITAL PHASE SHIFTER IN FIG. 21 (IN MILLIMETERS)

W_1	W_2	W_3	W_4	W_5	W_6	W_7
1.118	11.28	1.575	0.559	1.981	1.981	0.229
W_8	W_9	W_{10}	L_1	L_2	L_3	L_4
1.270	0.737	0.432	2.540	6.350	2.540	0.508
L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}
4.572	7.468	1.676	1.067	7.468	17.98	1.524
L_{12}	L_{13}	L_{14}	L_{15}	L_{16}		
3.099	0.254	0.864	0.508	0.813		

input and output. The taper line transition is adopted to transform the microstrip line to a DSPSL.

There are additional parasitic inductances and capacitances caused by the SOT-323 package, as shown in Fig. 16. To compensate these parasitic effects, additional capacitors are added, as can be found in Fig. 15(b) and (c). In Fig. 15(c), there are two C_1 capacitors of 0.3 pF soldered between the two output leads of each series-T package and one C_2 capacitor of 0.7 pF connected between the input leads of the two series-T packages, which are located at different sides of the circuit board. When Bias1 in Fig. 15(a) is biased with positive voltage with respect to Bias2, node 2, 3 and node 4, 6 in Fig. 15(c) would be forward biased, and node 1, 3 and node 5, 6 would be reverse biased. The 180° digital phase shifter will operate as shown in Fig. 13(a). When Bias1 is biased with negative voltage with respect to Bias2, the 180° digital phase shifter will operate as shown in Fig. 13(b).

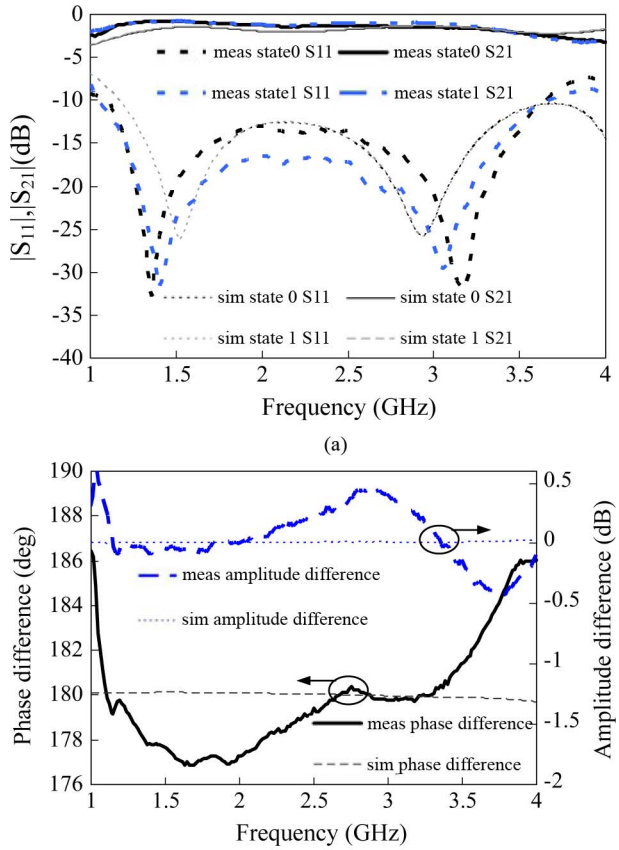

Fig. 22. Simulated and measured results of the 180° digital phase shifter. (a) Magnitude response. (b) Phase and amplitude difference.

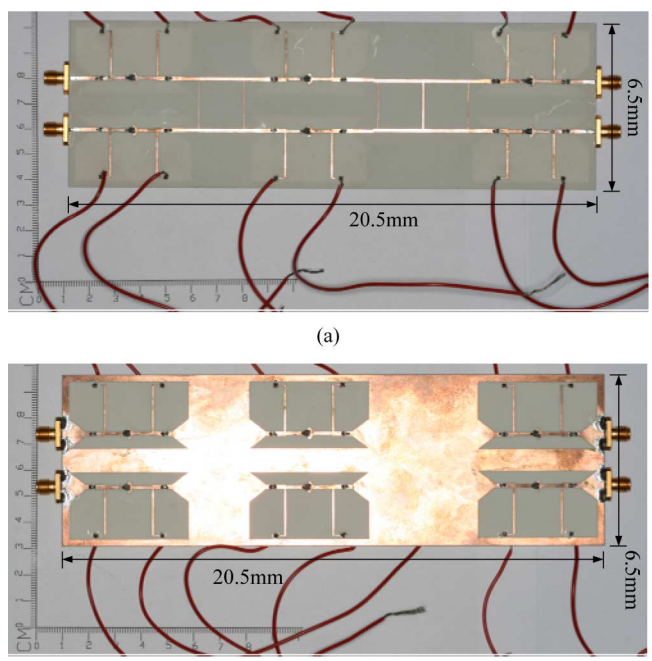

Fig. 23. Fabricated circuit of the 3-bit digital phase shifter using commensurate transmission line filter as biasing circuit. (a) Top layer. (b) Bottom layer.

III. IMPLEMENTATION AND MEASURED RESULTS

After fine tuning the circuit in a circuit simulator, all of the circuits are simulated and further fine tuned with an EM simulator.

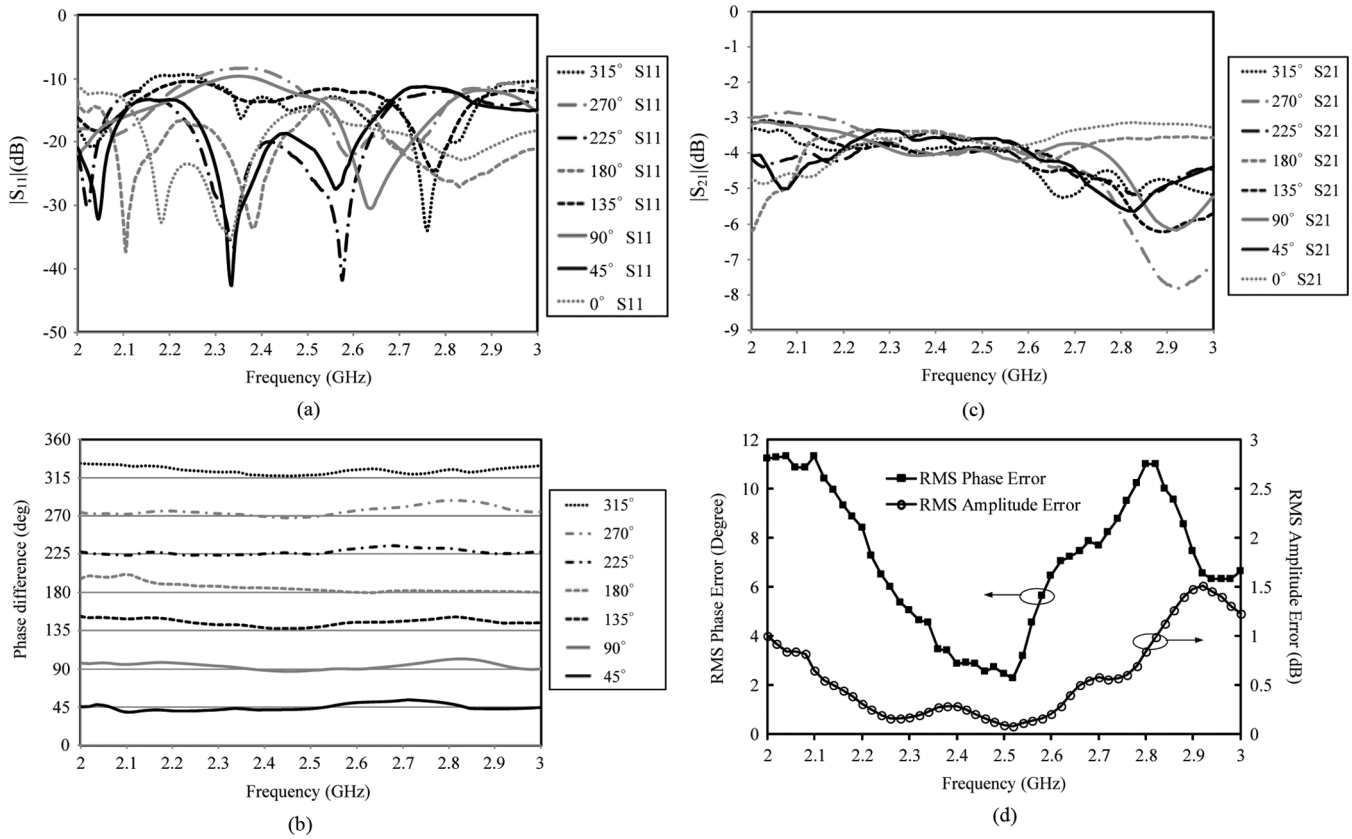

Fig. 24. Measured response of the proposed 3-bit digital phase shifter. (a) S_{11}. (b) S_{12}. (c) Phase difference of all states. (d) RMS phase and amplitude error.

The circuits are implemented by microstrip lines and DSPSLs on a Rogers RO4003 substrate with a thickness of 0.508 mm and a dielectric constant of 3.58. The p-i-n diodes are Avago HSMP-389C series-T p-i-n diodes. The capacitors are muRata GRM0335C-series.

A. 45° Balanced Digital Phase Shifter

Fig. 17 shows the layout of the 45° balanced phase shifter. The physical dimensions corresponding to Fig. 17 are listed in Table V. Fig. 18 shows the EM simulated and measured responses. The measured bandwidth is a little smaller than the simulated one and thus the measured phase difference is a little lager than the simulated one. The comparison table is shown in Table VI.

B. 90° Balanced Digital Phase Shifter

Fig. 19 shows the layout of the 90° balanced phase shifter. The dimensions corresponding to Fig. 19 are depicted in Table VII. Fig. 20 shows the EM simulated and the measured responses. The comparison table is in Table VIII.

C. Wideband 180° Digital Phase Shifter

Fig. 21 is the layout of the wideband 180° phase shifter. Fig. 21(b) shows an enlarged view of the twist-line portion of the circuit. In Fig. 21(b), there is a small island with a via-hole connected to the back side circuit, which is indicated with a dimension of L15 and W10. The island is for the compensation capacitor C_2 in Fig. 15(c). The physical dimensions corresponding to Fig. 21 are shown in Table IX.

While simulating the circuit in the EM simulator, we add internal ports at the places where the lumped capacitors and diodes should be soldered. The simulated result is extracted into the circuit simulator. The equivalent circuit of the biasing diode, lump capacitor models, and package parasitics are then co-simulated with the EM result.

Fig. 22 shows the simulated and measured responses. The simulated return loss at center frequency is degraded from 30 to 13 dB and is due to the parasitic effects of the two series-T p-i-n diodes. The measured insertion loss is about 1.5 dB. The worst case phase imbalance is about 3° and the amplitude imbalance is about 0.5 dB from 2.2 to 2.8 GHz. The simulated circuit response shows almost perfect phase and amplitude imbalance through 1.5–3.5 GHz. This might be caused by the slight layout difference of the top and bottom layers. Using the diodes to substitute the twist also causes some imbalance of the two states of the phase shifter.

D. 3-bit Balanced Digital Phase Shifter

By combining the above circuit elements, the 3-bit balanced digital phase shifter in Fig. 3 can be realized. The front-side and backside photographs of the 3-bit balanced digital phase shifter using a commensurate transmission-line filter are demonstrated in Fig. 23. The circuit size is 20.5 mm × 6.5 mm. Fig. 24(a)–(d) is the measured return loss, insertion loss, insertion phase of the circuit for each phase shifting state, and rms phase and amplitude error. The working bandwidth is from 2.3 to 2.7 GHz. The designed bandwidth of the 90° balanced phase shifter is about 2.3 ∼ 2.7 GHz, which is the narrowest bandwidth circuit

TABLE X
COMPARISON OF DIGITAL PHASE SHIFTERS

	Frequency (GHz)	Gain per bit (dB)	S_{11}	Phase error (rms)	Gain error (rms)	Area (mm^2)	Topology
[6]	11.6~12.6	0.75 to 0.875	<-17dB @11.6GHz~12.6GHz	2.6°~5.5°	0.3~0.35dB	1.88×0.915	4bit/single-ended/ active switch
[7]	9~15	-2.9 to -2.8	<-10dB @9GHz~15GHz	6°~12°	0.28~2.15dB	3.1×1.4	5bit/single-ended/ active switch
[20]	6~18	-0.53 to -0.05	<-10dB @8.5GHz~17.2GHz	2.7°~10°	0.5~1.7dB	0.75×0.6	4bit/differential/ vector sum method
[20]	15~26	-1.15 to -0.75	<-10dB @16.8GHz~26GHz	6.5°~13°	1.1~2.1dB	0.75×0.6	4bit/differential/ vector sum method
This work	2.3~2.7	-1.33 to -1.77	<-8.5dB @2.3GHz~2.7GHz	2.3°~7.9°	0.11~0.54dB	20.5×6.5	3bit/differential/ switching-mode

that limits the bandwidth of the whole circuit. The return loss is almost better than 10 dB and typical insertion loss is about 4 dB over all phasing states and frequency. The phase difference in 2.3 $\sim$ 2.7 GHz is close to 45° for each phase-shifting state. The rms phase error is less than 7.9° from 2.3 to 2.7 GHz. The rms gain error is less than 0.54 dB from 2.3 to 2.7 GHz. Table X compares the working bandwidths, gain per bit, S_{11}, phase error, gain error, area, and the topology for the published and proposed digital phase shifter.

IV. CONCLUSION

The 3-bit balanced digital phase shifter has been proposed in this paper by combining the 45° and 90° balanced digital phase shifters and six of the wideband 180° phase shifters. Each of the phase shifting state is achieved by even- or odd-mode excitation of the balanced 45° and 90° phase shifters.

Both the 45° and 90° balanced phase shifters are loaded-line phase shifter that loaded by the $\lambda/8$ open- or short-circuited stubs for even- and odd-mode half circuit, respectively. The 180° phase shifters control the excitation of the 45° and 90° balanced phase shifters to be even or odd mode. The commensurate transmission-line filter is used as the biasing circuit for the 180° digital phase shifter, which has been implemented by the DSPSL with two series-T p-i-n diodes to control the twist or nontwist of the signal. The simulated and measured results are matched well.

The circuit can be designed with more phase-shifting bits by the same principle.

There are still many works can be done in the future such as shrinking of the circuit size, reduction of the circuit losses, broaden the working bandwidth, etc. This paper, however, has well demonstrated the feasibility of the proposed switching-mode topology for a balanced digital phase shifter.

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