All-Digital Fast-Locking Pulsewidth-Control Circuit With Programmable Duty Cycle

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***Abstract*— This paper proposes an all-digital fast-locking pulsewidth-control circuit with programmable duty cycle. In comparison with prior state-of-the-art methods, our use of two delay lines and a time-to-digital detector allows the pulsewidth-control circuit to operate over a wide frequency range with fewer delay cells, while maintaining the same level of accuracy. This paper presents a new duty-cycle setting circuit that calculates the desired output duty cycle without the need for a look-up table. The circuit was fabricated under the two-stage matrix converter 0.18-μm CMOS process. Results show that the proposed circuit performs well for an input operating frequency ranging from 200 to 600 MHz, and an input duty cycle ranging from 30% to 70%. It achieves a programmable output duty cycle ranging from 31.25% to 68.75% in increments of 6.25%.**

***Index Terms*— Duty-cycle setting circuit, fast-locking, programmable duty cycle, pulsewidth-control circuit.**

I. Introduction

DOUBLE DATA RATE (DDR) technology is one solution to the need for system-on-a-chip systems capable of high-speed operations. Many systems, such as DDR-SDRAM and double-sampling analog- to-digital converter, use the rising and falling edges of the reference clock signal to sample the input signal. In high-speed systems, the clock signal often requires multistage clock buffers to drive the circuit. Variations in process, voltage, and temperature (PVT) may influence the duty cycle of the clock signal, making it difficult to calibrate the duty cycle precisely at 50%. As a result, overcoming deviations from a 50% duty cycle is an important issue in the further development of high-speed operations.

A number of pulsewidth-control loops (PWCLs) [1]–[7] have been proposed to overcome this deviation. A conventional PWCL [1] was produced using a built-in ring oscillator to produce a 50% duty-cycle reference clock. The duty cycle of the ring oscillator, however, deviated widely because of variations in PVT. In addition, the PMOS and NMOS of the pseudoinverter could limit the frequency range of the input signal. Although a low-voltage PWCL [2] is capable of operating with a shorter locking time, an accurate clock with 50% duty cycle is still required for the reference signal. The use of a single-to-differential circuit enables the low-jitter mutual-correlated PWCL [4] to escape from the limitations of the input signal's 50% duty cycle while avoiding variations in PVT. Each of these proposals [1]–[3] has the same limitations: the pseudoinverters restrict the operating frequency.

Many systems, such as ACD and digital-to-analog converter, require a reference clock with programmable duty cycle. Several approaches to achieving the programmable duty cycles have been proposed. PWCLs [8], [9] exploit analog methods to provide adjustable duty cycles. A single path PWCL [8] implements a switched charge pump to produce the programmable duty cycles. Because the circuit must wait until the delay locked loop (DLL) is locked to operate, locking time depends on the built-in DLL.

The all-digital PWCL [10] was designed to take advantage of scaling CMOS technologies. It, however, has two main drawbacks. The first is that the programmable duty cycle requires a look-up table to generate corresponding duty cycles with digital output codes. The second is that 28 reference cycles are required to be locked. Because this circuit applies serial detection methods to reduce the area and power of the D flip-flops, locking time is longer than with conventional systems.

This paper proposes a new all-digital pulsewidth-control circuit with the programmable duty cycle. Our approach provides four major benefits: 1) the use of two delay lines and a time-to-digital detector reduces the hardware required; 2) the pulsewidth-control circuit is capable of operating over a wide frequency range; 3) accuracy equal to that using previously developed circuits is achieved; and 4) an output duty cycle ranging from 31.25% to 68.75% in increments of 6.25% is achievable without the need for a look-up table, as a result of the proposed duty-cycle setting circuit. The remainder of this paper is organized as follows. Section II presents the architecture of the proposed system. Section III discusses the main building blocks. Experimental results are provided in Section IV. Conclusions are presented in Section V.

II. Proposed Circuit Architecture

A. Operation Approach

Fig. 1(a) shows the proposed all-digital pulsewidth-control circuit with the programmable duty cycle. The complete building blocks include: a one-shot circuit, a coarse pulsewidth identification circuit (CPI), a coarse delay line (CDL) and a coarse detector, a fine delay line (FDL) and a fine detector, a duty-cycle setting circuit, and a finite state machine (FSM) and control circuits. The system functions as follows. The period

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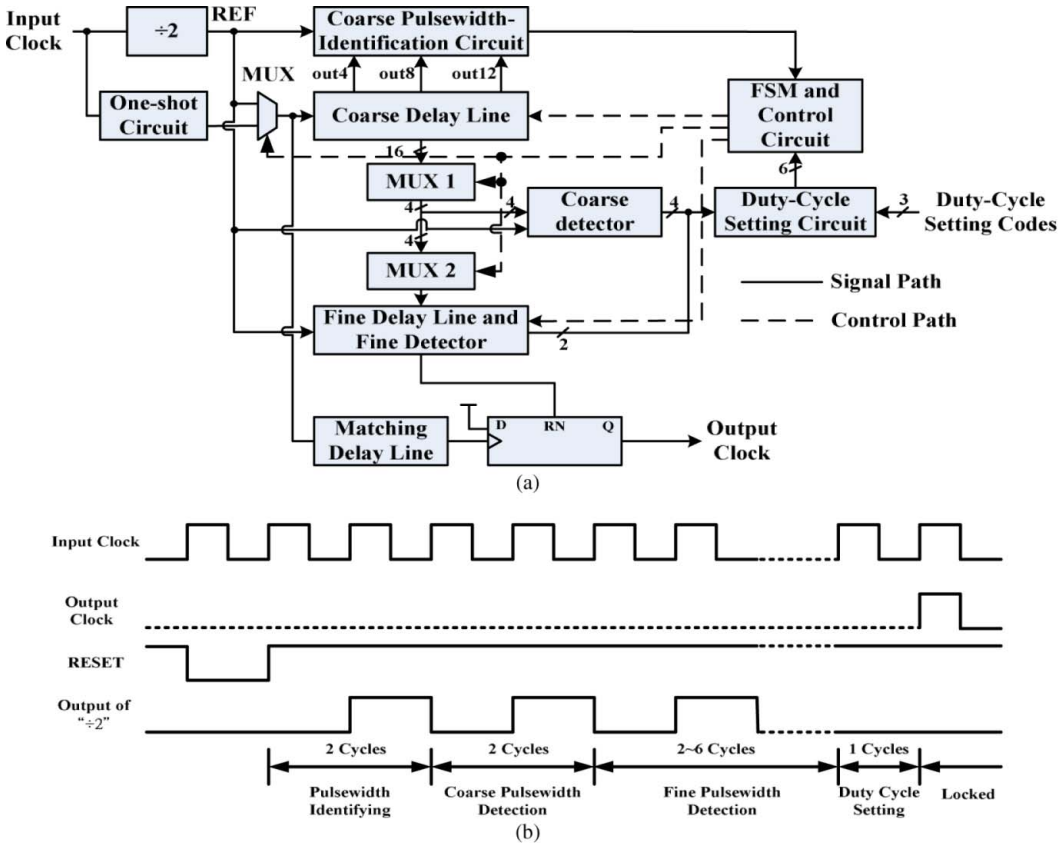

Fig. 1. (a) Proposed all-digital pulsewidth-control circuit. (b) Timing diagram of the proposed pulsewidth-control circuit.

of the input signal is determined by the two delay lines, which are then reused and controlled by the duty-cycle setting circuit to generate the final output signal with a duty cycle ranging from 31.25% to 68.75%.

In the proposed pulsewidth-control circuit, the input clock is divided by 2 to establish a reference signal [REF in Fig. 1(a)], with a duty cycle of 50%, regardless of the duty cycle of the input clock. Thus, identifying the pulsewidth of REF is equivalent to determining the period of the input clock. To ascertain the period of the input clock, we must determine the pulsewidth of REF. The one-shot circuit generates a pulse train with a frequency matching the input clock; therefore, it is used only to produce the rising edge of the output clock during the final duty-cycle setting. In the initial state, multiplexer (MUX) delivers REF to the CDL for pulsewidth detection. After the detection is complete, MUX incorporates the output of the one-shot circuit into the matching delay line (MDL) to produce the final output.

The CPI circuit is used to determine the pulsewidth of the input signal. It also detects the pulsewidth range of the divided REF to control the 16-to-4 MUX1 which, in turn, enables four output paths. The CPI circuit then turns off the unused coarse delay cells in the CDL to save power because the 16 coarse delay cells consume most of the power in the circuit, particularly under a high-speed input clock. The coarse detector proceeds to compare the four MUX1 outputs with REF to decide which of the 4-to-1 MUX2 input paths to enable. The fine detector then sequentially detects the three delay paths in the FDL to determine the delay that is closest to the REF pulsewidth. The coarse detector and fine detector operate in a manner similar to a time-to-digital converter in an all-digital phase-locked loop. After detection is complete, the same circuit may be reused to determine the final output clock.

The MUX output changes from REF to a one-shot circuit output to produce a pulse train. The pulse signal is then imported into the CDL. Because the one-shot circuit generates a signal with an equal pulsewidth regardless of the input signal frequency, the input signal's duty cycle can range from 30% to 70%. The duty-cycle setting circuit calculates the detected results of the coarse and fine detector outputs, in conjunction with the duty-cycle setting code inputs, and reuses the path of the CDL, MUX1, MUX2, and the FDL to generate the final delay signal. The output clock is generated using a D flip-flop with asynchronous reset. An MDL cancels out the extra delay caused by MUX1 and MUX2. The mismatch between MUX1, MUX2, and the MDL would certainly influence the precision of the duty cycle. The proposed circuit, however, uses a pulse, generated using a one-shot circuit that passes through the CDL and FDL to produce the desired duty cycle from the original pulse, as calculated by the duty-cycle setting circuit. Because we needed MUX1 and MUX2 to enable the corresponding outputs of CDL and FDL, we also required an MDL to compensate for the redundancy delay produced by MUX1 and MUX2. The MDL features the same structure as MUX1 and MUX2, and turns off the unused matching tri-buffers to

save power. Thus, the mismatch between MUX1, MUX2, and the MDL is nearly negligible.

The pulse-train signal that passes through the MDL triggers the D flip-flop to produce the rising edge of the output clock. The final delay signal, determined by the duty-cycle setting circuit, determines when to reset the D flip-flop to produce the falling edge of the output clock. The desired value of the duty cycle can be obtained from the duty-cycle setting circuit. There are two reasons for using D flip-flops [true single phase clock D flip-flop (TSPC DFF)], instead of the SR latches in [10]. First, the TSPC DFF operates with only one clock signal (without the need for its inverted clock). Thus, no clock skew exists and even higher clock frequencies can be achieved. This also means that the setup time and hold time can be much smaller; therefore, the width of the trigger pulse and reset pulse can be smaller than the pulses of the S and R inputs. This enables a higher operating frequency. Second, an SR latch cannot work if input pulse R overlaps pulse S, but a TSPC DFF can operate in this situation. Thus, using D flip-flops facilitates the implementation of clocks with a small or large duty cycle at high frequencies than those afforded by SR latches.

The timing diagram is shown in Fig. 1(b). The proposed circuit requires two cycles to identify the pulsewidth, two cycles for coarse detection, and one cycle for the duty-cycle setting circuit to calculate the final results. These are the same for every detection. The only difference for each detection is the time required for fine detection since the FDL and fine detection use a serial structure. It requires two to six cycles for fine detection. Thus, the total operating time of the circuit is 7–11 cycles, depending on the process of fine detection. These operations are performed digitally; therefore, this approach is easily applicable to other advanced processes. Detailed descriptions of the circuit blocks are discussed below.

B. Design Flow Chart

A flow chart of the FSM and the operations of the control circuit in each state are shown in Fig. 2. When the circuit is initially reset, the control circuit initiates all D flip-flops. Subsequently, the FSM changes to the coarse pulsewidth identification state. The MUX enables the REF to enter the CDL and the CPI circuit detects the pulsewidth range of the REF. Following detection, the control circuit enables the four outputs of the CDL into the coarse detector according to the detection results of the CPI circuit. The control circuit also turns off the unused coarse delay cells to save power, with consideration of the fact that the coarse delay cells are the main source of power consumption, especially under the high-speed operations. The FSM subsequently changes to the coarse detection state, and the coarse detector then compares four outputs from the MUX1 with the REF. Following detection, MUX2 enables one path from MUX1 into the FDL according to the detection results of the coarse detector. When the FSM switches to fine detection state, the control circuit enables each path from the MUX2 to perform detection of greater precision sequentially if the detection is not finished. After the duty-cycle setting circuit calculates the final results, the FSM changes to the output generation state. Thus, the MUX allows

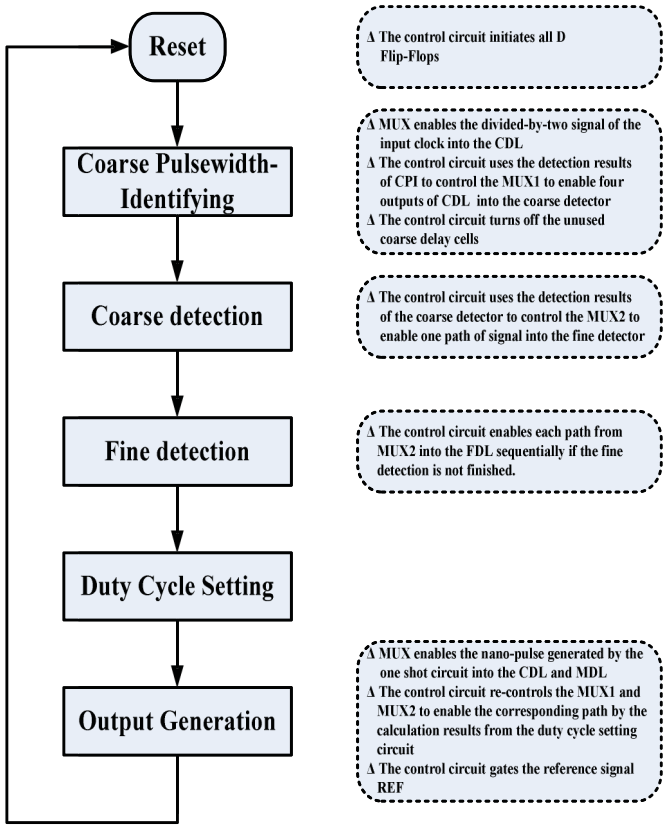

Fig. 2. Flow chart of the FSM and the operations of the control circuit.

the pulse generated by the one-shot circuit into the CDL and MDL to produce the output clock. The control circuit also re-controls MUX1 and MUX2 to enable the corresponding path to produce the desired duty cycle according to the results calculated from the duty-cycle setting circuit. The control circuit simultaneously gates the REF to save power because the REF is not used for output generation. The output clock continues generating until the next reset signal.

III. Main Building Blocks

A. CPI Circuit

The CPI circuit is used to determine the pulsewidth of REF, which is equal to the period of the input signal. The CPI circuit and an example of a timing diagram are presented in Fig. 3(a) and (b), respectively. The divided signal REF is sent to both the CPI circuit and the CDL. The CPI circuit also receives three output signals (Out4, Out8, and Out12) from the CDL. The three signals divide the CDL into four parts, each of which has four coarse delay cells, as shown in Fig. 4. The pulses of Out4, Out8, and Out12 trigger three D flip-flops, respectively. The pulsewidth codes F1, F2, F3, F4, and FC_FINISH are initially set to {10000}. Assume that the input pulsewidth is between 8 coarse delays and 12 coarse delays, as shown in Fig. 3(b). The Out4 delay signal triggers a corresponding D flip-flop. The pulsewidth code F1 falls low and F2 rises high. Because the input pulsewidth is larger than eight coarse delay cells, Out8 also triggers a D flip-flop. The pulsewidth code F2 falls low and F3 rises high. When REF falls low, the FSM changes to

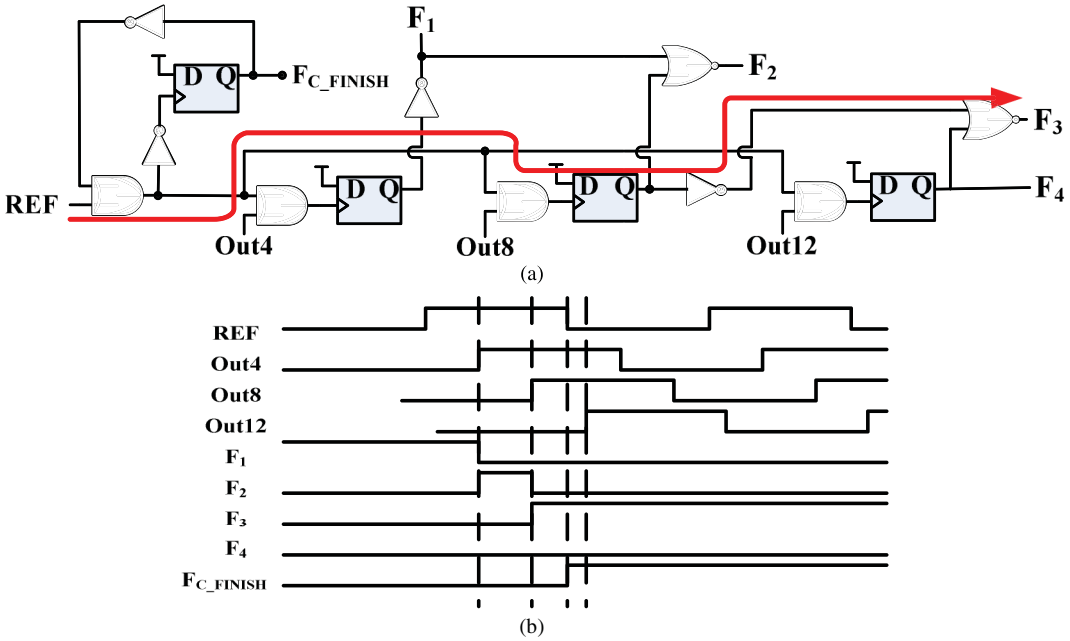

Fig. 3. (a) CPI circuit. (b) One example of the time diagram of the CPI circuit.

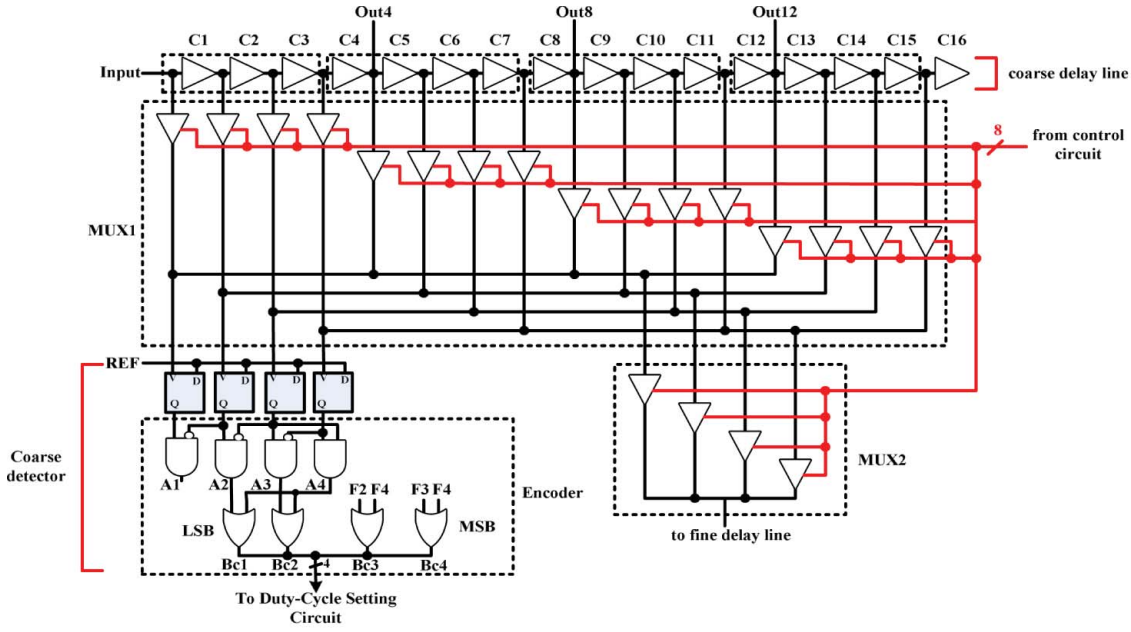

Fig. 4. Block diagram of the CDL and coarse detector.

the following state and FC_FINISH is set to high to complete the detection. Therefore, Out12 does not trigger the final D flip-flop and F3 and F4 do not change their states. Because the clock of each D flip-flop is gated, when the detection is completed, the CPI circuit blocks the REF to save the results of the D flip-flops and reduce dynamic power. Without a CPI circuit, the coarse detector would require 16 D flip-flops for detection; with the CPI circuit, the coarse delay circuit only requires one quarter of the number of D flip-flops, thereby greatly reducing costs and power usage. Finally, pulsewidth codes F4 to F1 are set to {0100}, and then sent to the FSM and the control circuit to control the CDL and MUX1.

The CPI circuit in the proposed pulsewidth-control circuit has two main functions. First, it reduces the number of detectors required in the CDL. This circuit has a smaller area cost and lower decoder complexity than those of conventional coarse detectors. Second, when the detection of the input signal is finished, the CDL, MUX1, MUX2, and FDL are reused to generate the falling edge of the output signal. If the pulsewidth-control circuit operated at a high frequency and all of the coarse delay cells of the CDL were turned on, the CDL would require a great deal of power. The CPI circuit turns off unused coarse delay cells to save power. For example, when the period of the input signal is less than $8\tau_c$ (eight coarse cell

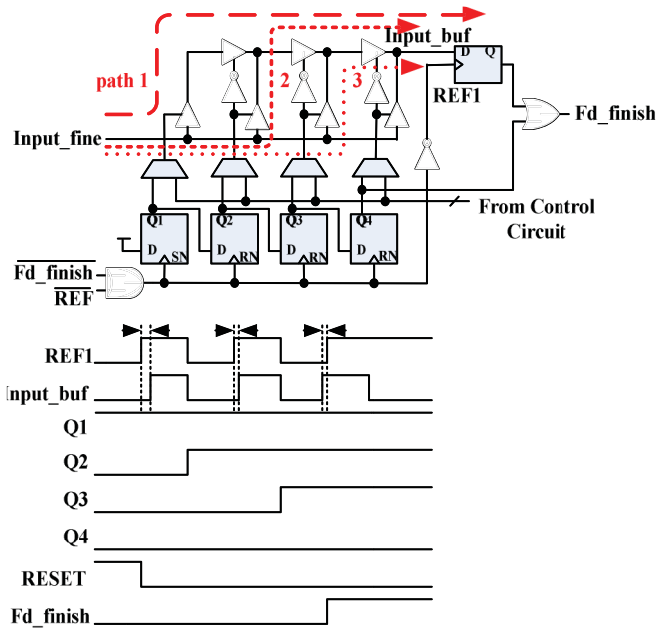

Fig. 5. FDL, fine detector, and one example of the timing diagram.

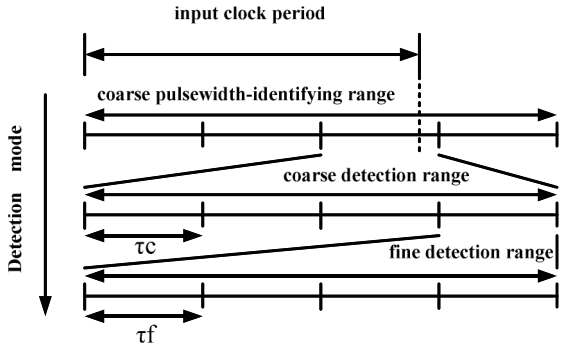

Fig. 6. Pulsewidth detection of each mode.

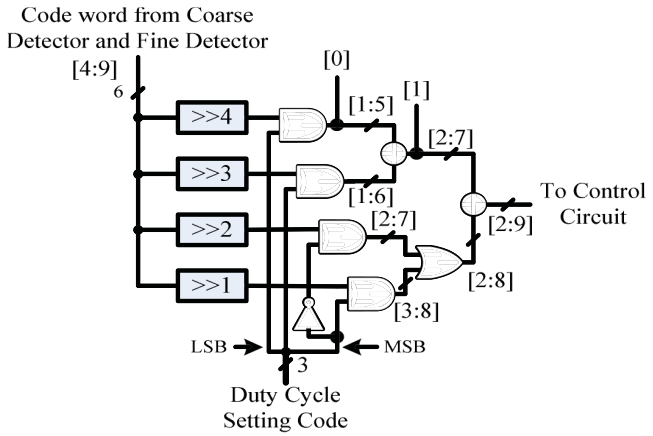

Fig. 7. Proposed duty-cycle setting circuit.

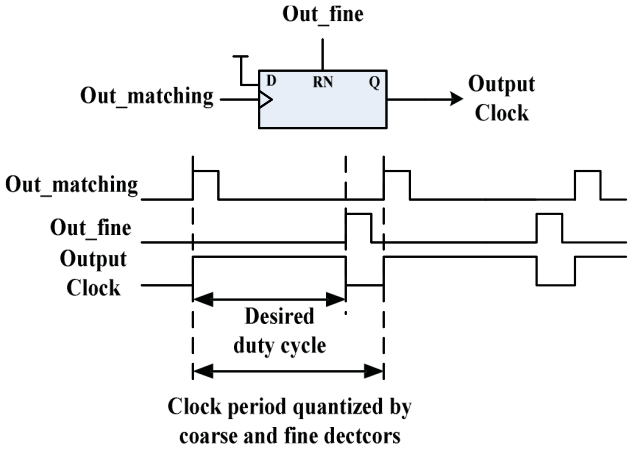

Fig. 8. Output clock generator.

delay), coarse delay cells C9 to C16 remain unused, allowing the CPI circuit to turn them off to save power.

B. CDL and Coarse Detector

Fig. 4 presents the CDL and coarse detector. The CDL comprises 15 tri-state delay cells, C1 to C15, and one matching delay cell, C16, where each cell has a delay of τ_c. The CDL is divided into four groups: C1 to C3, C4 to C7, C8 to C11, and C12 to C15. MUX1 selects one signal (Input, Out4, Out8, or Out12), and sends it to the coarse detector and MUX2. MUX1 also selects another signal (Out1, Out5, Out9, or Out13), and sends it to the coarse detector and MUX2, as well. The same selection also applies to (Out2, Out6, Out10, and Out14) and (Out3, Out7, Out11, and Out15). If the pulsewidth of the input signal REF is greater than $8\tau_c$ and smaller than $12\tau_c$, the CPI circuit detects it, generates codes F4 to F1 of {0100}, and directs MUX1 to enable the four outputs (Out8 to Out11) of delay cells C8 to C11. Because C12 to C15 delay cells are not used, the CPI circuit turns them off to save power. The coarse detector compares the delays of Out8, Out9, Out10, and Out11 with REF to convert the pulsewidth of the input signal into digital code. A thermometer-to-binary encoder then converts the digital code from the coarse detector and CPI circuit into binary code. If the pulsewidth falls between Out11 and Out12, the coarse detector codes A4 to A1 as {1000}, and the pulsewidth codes F4 to F1 from CPI are coded as {0100}. The final output binary code of the coarse detector, Bc4 to Bc1, equates to {1011}, which is equal to the number of coarse delay cells closest to the REF pulsewidth. After detection is complete, the control circuit determines which of the MUX2 paths to enable and pass to the fine delay block for detection of greater precision.

C. FDL and Fine Detector

Fig. 5 presents the FDL and fine detector. The FDL comprises three tri-state delay cells. Each cell has a delay τ_f, which, in our design, is equal to one-quarter of τ_c. In the structure of conventional detectors, each delay cell is connected to a D flip-flop for phase detection, a subsequent delay cell, and an output buffer. This structure is similar to that of the coarse detector. The advantage of the conventional structure is that only one clock cycle is required to complete detection. The disadvantage is that it increases the loading to each of the delay cells, which may increase the intrinsic delay

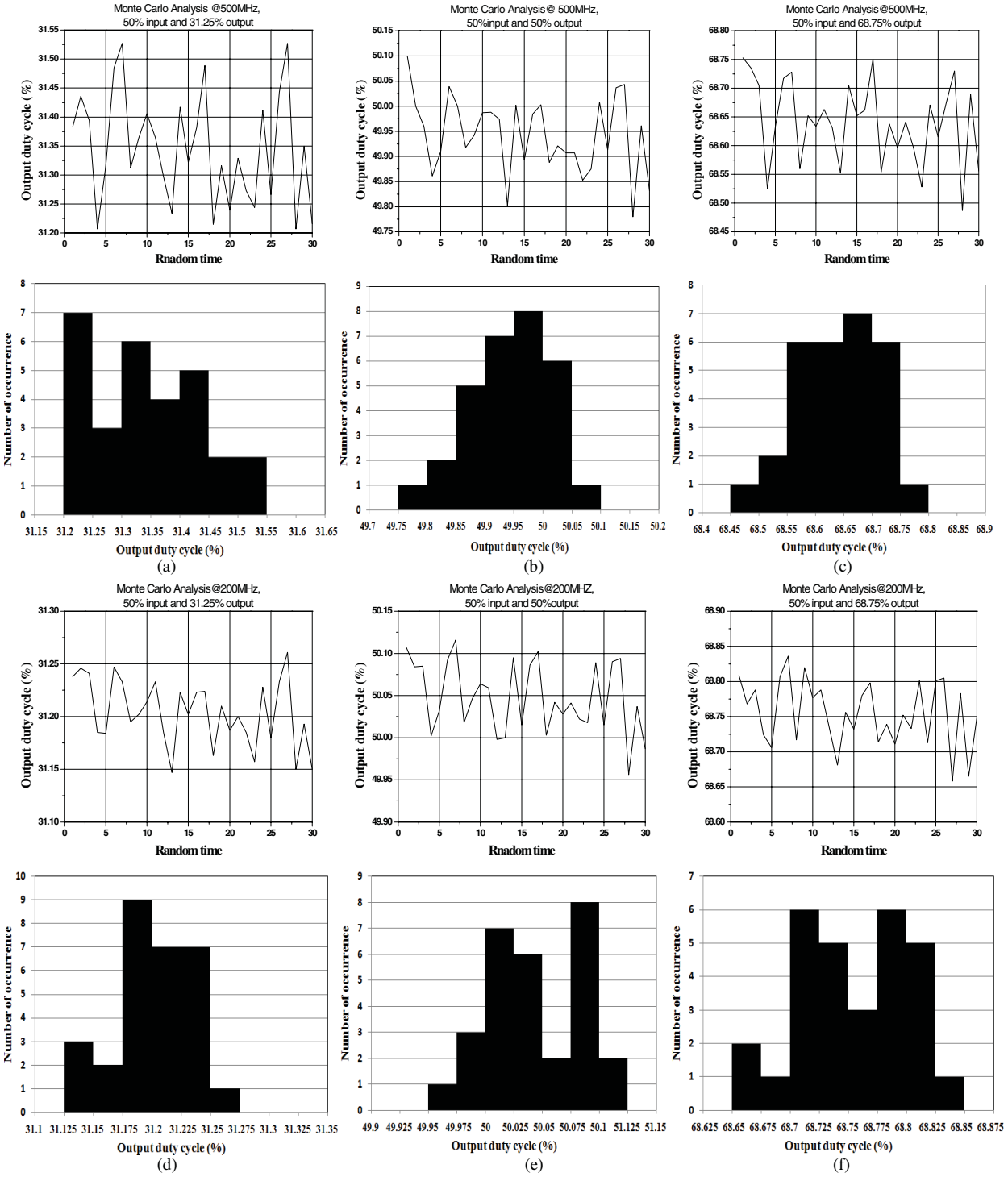

Fig. 9. Monte Carlo simulation results for CLKin duty cycle = 50%. (a) Frequency = 500 MHz, CLKout duty cycle = 31.25%, and $\sigma = 0.09587\%$. (b) Frequency = 500 MHz, CLKout duty cycle = 50%, and $\sigma = 0.07585\%$. (c) Frequency = 500 MHz, CLKout duty cycle = 68.75%, and $\sigma = 0.07253\%$. (d) Frequency = 200 MHz, CLKout duty cycle = 31.25%, and $\sigma = 0.03178\%$. (e) Frequency = 200 MHz, CLKout duty cycle = 50%, and $\sigma = 0.04229\%$. (f) Frequency = 200 MHz, CLKout duty cycle = 68.75%, and $\sigma = 0.04703\%$.

time of each delay cell. To improve the time resolution of the FDL, we employed a serial structure to perform fine detection. Unlike a parallel structure, a serial structure enables a decrease in the fan out of the delay cells because phase detection need to be performed only on the last delay cell, instead on each of them. Because the signal, Input_fine, is derived from the CDL, the phase difference between Input_fine and REF is smaller than the delay time of one coarse delay cell; that is, the phase difference between Input_buf and REF is smaller than $4\tau_f$. The use of only three delay cells enables the FDL to decrease detection time and improve time resolution.

In our example (Fig. 5), the initial values of Q4 to Q1 are set to $\{0001\}$. The input signal from the CDL first travels through path 1. The signal has been delayed by $3\tau_f$, compared

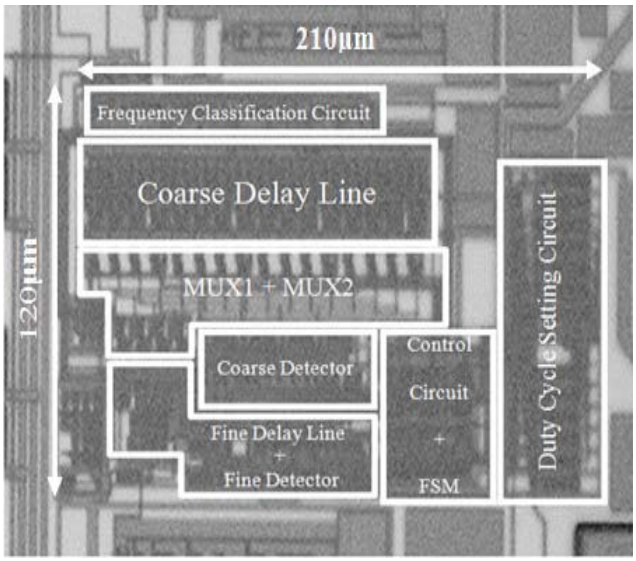

Fig. 10. Die micrograph.

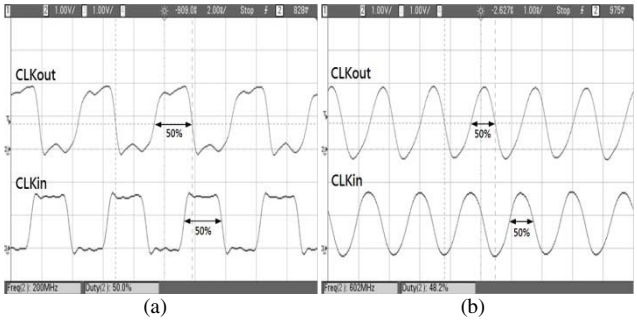

Fig. 11. CLKin duty cycle = 50%, CLKout duty cycle = 50%. (a) Frequency = 200 MHz. (b) Frequency = 600 MHz.

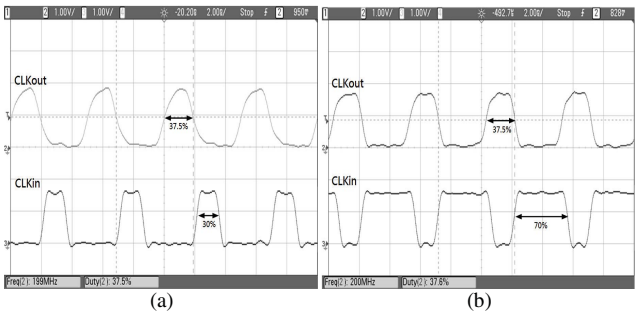

Fig. 12. Frequency = 200 MHz, CLKout duty cycle = 37.5%. (a) CLKin duty cycle = 30%. (b) CLKin duty cycle = 70%.

with REF1. Reference signal, REF1, is a replica of REF. It is used to determine whether the Input_buf is leading or lagging. If REF1 does not trigger the D flip-flop, this is an indication that Input_buf lags REF1. In other words, the pulsewidth of REF (the input clock period) is $3\tau_f$ smaller than the detected results of the CPI circuit and the CDL. The sequential detection of the pulsewidth of the input signal in each mode is shown in Fig. 6. Following the detection of path 1, the fine detector enables the comparison of path 2 of the delay line and REF1 to be repeated. If Input_buf still lags REF1, the fine detector continues on to path 3. If REF1 triggers

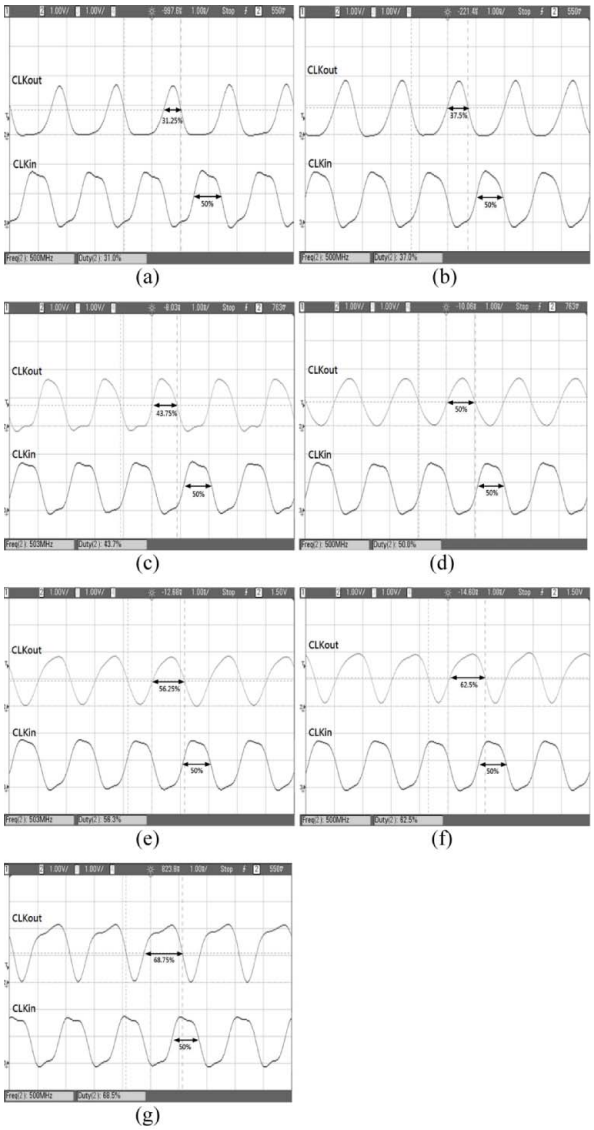

Fig. 13. Frequency = 500 MHz, CLKin duty cycle = 50%. (a) CLKout duty cycle = 31.25%. (b) CLKout duty cycle = 37.5%. (c) CLKout duty cycle = 43.75%. (d) CLKout duty cycle = 50%. (e) CLKout duty cycle = 56.25%. (f) CLKout duty cycle = 62.5%. (g) CLKout duty cycle = 68.75%.

the D flip-flop in this state, it means that Input_buf leads REF1. The pulsewidth of REF is τ_f larger than the detection results of the CPI circuit and the CDL, but $2\tau_f$ smaller than them. Once the detection is complete, FSM changes to the following state and passes the results to the duty-cycle setting circuit. In this case, Input_buf leads REF1 when path 3 is enabled and Q4 to Q1 = {0111}, such that the final output codes Bf2 to Bf1 of the fine detector become {01}, which is equal to the number of fine delay cells closest to the pulsewidth of REF, after being converted by the thermometer-to-binary encoder. If Input_buf still lags REF1 after paths 1–3 are all enabled, Q4 to Q1 = {1111}, and the final output codes Bf2 to Bf1 become {00}.

The proposed circuit requires two to six cycles for fine detection. If the comparison signal REF1 lags Input_buf when the control circuit enables path 1, the detection will be performed using only two cycles. If the REF1 leads Input_buf

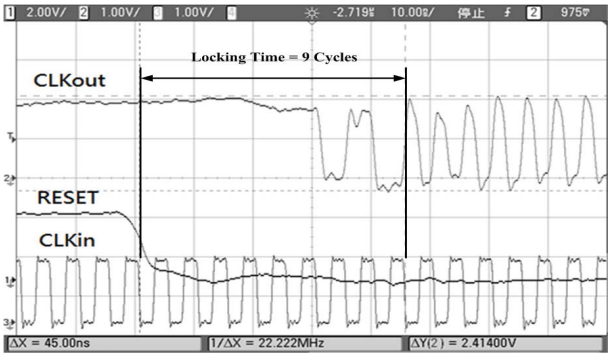

Fig. 14. Locking time of the output clock at 200 MHz.

TABLE I
DUTY CYCLE SETTING CODES

Duty cycle (%)	Duty-cycle setting code (acd)	Duty cycle (fractional number)	
31.25	001	$\frac{5}{16}$	$\frac{1}{16}+\frac{1}{4}$
37.50	010	$\frac{6}{16}$	$\frac{1}{8}+\frac{1}{4}$
43.75	011	$\frac{7}{16}$	$\frac{1}{16}+\frac{1}{8}+\frac{1}{4}$
50	100	$\frac{8}{16}$	$\frac{1}{2}$
56.25	101	$\frac{9}{16}$	$\frac{1}{16}+\frac{1}{2}$
62.50	110	$\frac{10}{16}$	$\frac{1}{8}+\frac{1}{2}$
68.75	111	$\frac{11}{16}$	$\frac{1}{16}+\frac{1}{8}+\frac{1}{2}$

when path1 is enabled, the control circuit will disable path 1 and enable path 2 to continue the detection. If REF1 lags Input_buf when path 2 is enabled, the detection will be performed in four cycles. If REF1 leads Input_buf when paths 1 and 2 are enabled sequentially, detection will require six cycles. The proposed circuit requires two cycles to identify the pulsewidth, two cycles for coarse detection, and one cycle for the duty-cycle setting circuit to calculate the final results. Thus, the total operating time of the circuit is 7–11 cycles, depending on the process of fine detection.

D. Duty-Cycle Setting Circuit

Fig. 7 shows the proposed duty-cycle setting circuit. The detected results of the coarse detector and fine detector are converted to a 6-bit binary code (bits [4:9]) by the thermometer-to-binary encoder. The binary code is then sent to the duty-cycle setting circuit, which calculates the corresponding results based on the duty-cycle setting codes provided by the programmer. Because the detected digital code corresponds to the period of the input signal, an output clock with the desired duty cycle can be implemented by sending the pulse with the delay (the percentage of which corresponds to that of the input period), to reset the D flip-flop of the output clock generator (see Fig. 8). For example, because the detected digital codes correspond to a 100% duty cycle, a 50% duty-cycle output clock can be implemented by dividing the detected digital codes by 2. The newly calculated results from the duty-cycle setting circuit can be used to resume control of MUX1 and MUX2 and enable the corresponding path to generate the output clock. Note that 25%, 12.5%, and 6.25% duty cycles can be achieved by dividing the detected digital codes by 4, 8, and 16, respectively. According to the output codes of the coarse and fine detectors, the input signal period is quantified as {Bc4 Bc3 Bc2 Bc1 Bf2 Bf1}. Using the duty-cycle setting codes {abcd}, the duty cycle of the output clock can be set to

$$\begin{aligned} &a\times Bc4Bc3Bc2Bc1Bf2.Bf1(50\%)\\ &\quad +b\times Bc4Bc3Bc2Bc1.Bf2Bf1(25\%)\\ &\quad +c\times Bc4Bc3Bc2.Bc1Bf2Bf1(12.5\%)\\ &\quad +d\times Bc4Bc3.Bc2Bc1Bf2Bf1(6.25\%)\\ &\quad (a,b,c,d=0 \text{ or } 1). \end{aligned}$$

If the output duty cycle is set from ((5/16)(31.25%)) to ((11/16)(68.75%)) in steps of ((1/16)(6.25%)), (1/2), and (1/4) do not appear concurrently. Therefore, b can be set to $\bar{a}$, such that the duty-cycle setting codes can be reduced to {acd}. For example, if the input signal period is 010000 ($4\tau_c$), and the output duty cycle is set to 31.25% ((1/16) + (1/4)), based on Table I, the results from the dutycycle setting circuit become

$$\begin{aligned} &0\times 01000.0+1\times 0100.00+0\times 010.000+1\times 01.0000\\ &=101.0000\equiv(1\tau_c+1\tau_f). \end{aligned}$$

The pulse train produced by the one-shot circuit triggers the D flip-flop with an asynchronous reset to generate the rising edge of the output clock, as shown in Fig. 8. The control circuit uses the results of the duty-cycle setting codes to determine which MUX1 and MUX2 paths should be enabled. The pulse train then passes through two delay lines and resets the D flip-flop of the output clock generator to generate the falling edge. This operation is repeated to produce the final output clock. In the example, the desired output with a 31.25% duty cycle can be achieved by delaying the pulse train from the one-shot circuit using one coarse delay cell and one fine delay cell to reset the D flip-flop of the output clock generator. The implementation of the duty-cycle setting circuit uses shift registers to express the division of the code: one shift corresponds to (1/2), two shifts correspond to (1/4), and so on. Because bits [4:9] corresponds to an integer of fine delay cells, bits [0:3] represents the decimal number of a fine delay cell. Bits [0] and [1] would not influence the operation of the overall circuit; therefore, they are both overlooked during this calculation. As a result, we require only a 6-bit adder and a 7-bit adder, as shown in the Fig. 7. The duty-cycle setting circuit then adds the codes to generate the final results using full adders controlled by the setting codes. In our design, because (1/2) and (1/4) do not appear concurrently (as shown in Table I), hardware cost can be reduced by having two codes share an addition operation. For example, if we want to produce a duty cycle of 68.75%, the duty-cycle setting code is set to {111}. The AND gates provide the code represented by 6.25%, 12.5%, and 50%. Following two addition operations, the desired duty cycle corresponding to 6.25% + 12.5% + 50% = 68.75% can be calculated using the duty-cycle setting codes.

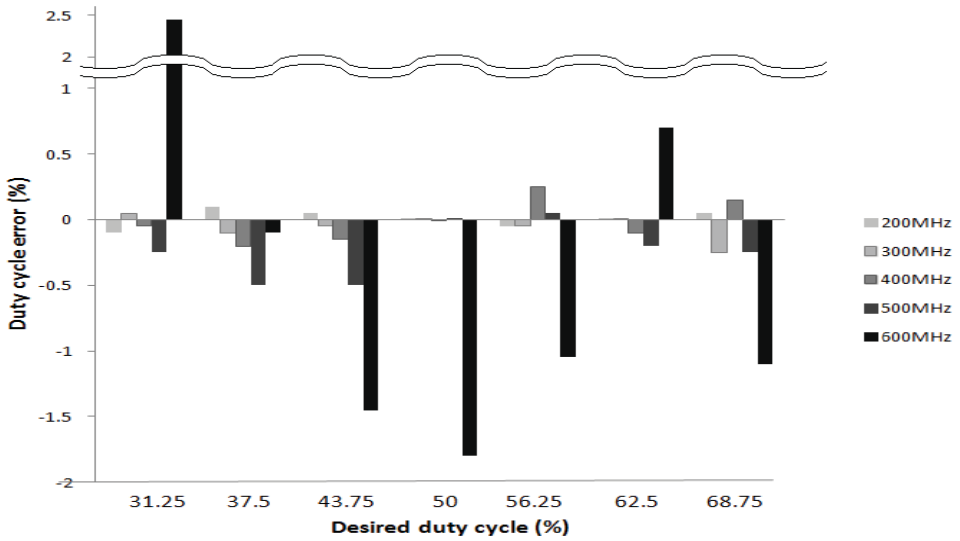

Fig. 15. Measured errors with respect to different output duty cycles from 200 to 600 MHz.

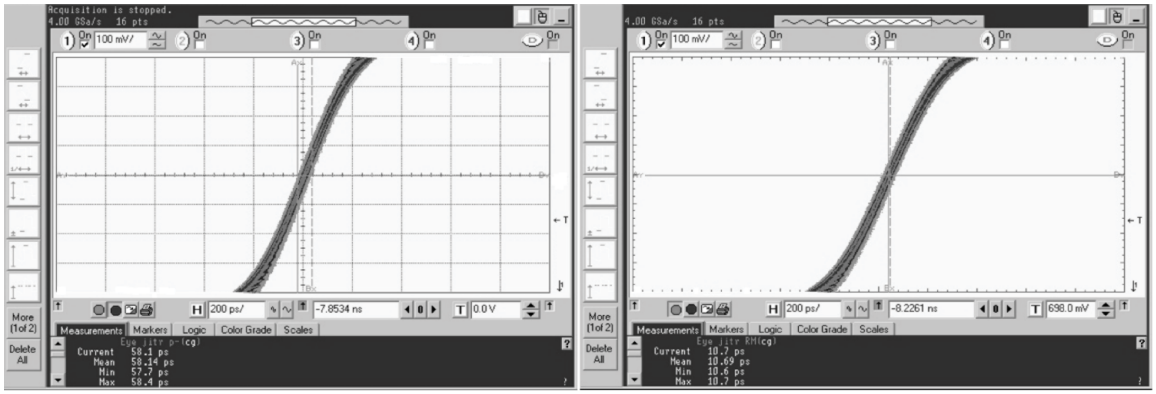

Fig. 16. Measured jitter of the output clock at 600 MHz.

IV. Simulation and Experimental Results

A. Monte Carlo Analysis

Monte Carlo analysis of the proposed circuit has been performed using two-stage matrix converter (TSMC) 0.18-μm Monte Carlo statistical model. Because the CDL, FDL, and output generator are sensitive to the size variation of the MOS transistors, we add variation on the sizes of MOS transistors according to the technical documents provided by TSMC for the reliability test. The number of Monte Carlo iterations is 30, and the simulation results are shown in Fig. 9. We use 50% duty cycles of 200 and 500 MHz input clocks to produce 31.25%, 50%, and 68.75% duty cycles of output clocks. Based on the simulation results shown below, the duty cycle errors are smaller than 0.3% for 500 MHz input clock and smaller than 0.15% for 200 MHz input clock, which can prove the validity of the propose circuit.

B. Experimental Results

The proposed circuit was fabricated using the 0.18-μm TSMC 1P6M CMOS process. Fig. 10 presents a die micrograph of the proposed circuit. The core die area is 210 μm $\times$ 120 μm = 0.0252 mm^2. The supply voltage is 1.8 V and the operating frequency ranges from 200 to 600 MHz. Fig. 11 shows the output clock at a 50% duty cycle with operating frequencies of 200 and 600 MHz, when the input clock has a 50% duty cycle. Fig. 12 shows the output clock at a 37.5%

TABLE II
Performance Summary of the Presented Pulsewidth-Control Circuit

Technology	TSMC 0.18-μm 1P6M CMOS
Power supply	1.8 V
Operation range	200–600 MHz
Input duty cycle (%)	30–70
Output duty cycle (%)	31.25–68.75 at 6.25%
Locking time	7–11 cycles
Peak-to-peak jitter	58.14 ps at 600 MHz
Rms jitter	10.69 ps at 600 MHz
Power consumption	5.49 mW at 600 MHz
Core area	0.0252 mm^2

TABLE III
PERFORMANCE COMPARISON WITH OTHER WORKS

	JSSC04 [4]	JSSC05 [8]	JSSC06 [10]	JSSC08 [9]	TVLSI11 [7]	This paper
Control method	Analog	Analog	Digital	Analog	Analog	Digital
Process	0.35-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	0.18-μm CMOS	0.35-μm CMOS	0.18-μm CMOS
Operation range	300–900 MHz	1–1.27 GHz	400–600 MHz	1 MHz to 1.3 GHz	70–500 MHz	200–600 MHz
Input duty cycle	N/A	N/A	30%–70%	30%–70%	5%–95%	30%–70%
Output duty cycle	50%	35%–70%	30%–70% at 10%	30%–70% at 5%	50%	31.25%–68.75% at 600 MHz
Locking time	3 μs (simulation)	N/A	28 cycles	$<$ 600 ns	NA	7–11 cycles
Need look-up table	NO	NO	YES	NO	NO	NO
Power (mW)	2.45 mW at 1 GHz (simulation)	150 mW	20 mW at 500 MHz	4.8 mW at 1.3 GHz	23 mW at 500 MHz	5.49 mW at 600 MHz
Core area (mm^2)	0.02	0.129	0.682	0.057	0.275	0.0252

duty cycle with two 200 MHz input clocks, one with a 30% duty cycle, and one with a 70% duty cycle. The proposed all-digital pulsewidth-control circuit works well with various input clock duty cycles. Fig. 13 demonstrates the output waveforms of duty cycles ranging from 31.25% to 68.25% in increments of 6.25% at 500 MHz. Our results indicate that the proposed duty cycle setting circuit can operate correctly across a range of frequencies and generate correct outputs for the corresponding duty cycles. Fig. 14 demonstrates that the proposed all-digital pulsewidth-control circuit is capable of achieving rapid locking only after 7–11 cycles. We adopted the structure of an inverter chain in the output driver of the proposed circuit by increasing the size of the inverter at each stage by a factor of two to three to drive the parasitic loads of the bonding pads and the output measurement equipment. Although the inverter chain is used to drive the loading, when the signal first arrives in the inverter chain, the parasitic inductance of the bonding wire influences the stability of the output clock for several clock cycles. The output clock stabilizes afterwards. The same phenomenon appears in [6]. In Fig. 15, the measured duty-cycle error with respect to various output duty cycles (ranging from 200 to 600 MHz) is less than $\pm$2.5%. Jitter measurements are provided in Fig. 16. Here, the peak-to-peak jitter is 58.14 ps and the rms jitter is 10.69 ps, with a 46 ps peak-to-peak jitter of the source clock. Power consumption at 600 MHz is 5.49 mW. The performance summary and comparison are provided in Tables II and III, respectively. As shown in Table III, the proposed circuit has a small core area and simultaneously achieves fast locking within 7–11 clock cycles.

V. CONCLUSION

This paper presented a fast-locking all-digital pulsewidth-control circuit with programmable duty cycle. The proposed approach using two delay lines and two detectors is capable of reducing hardware costs, compared with previous solutions, while achieving an equal degree of accuracy. We proposed a new duty-cycle setting circuit to produce output duty cycles from 31.25% to 68.75% in increments of 6.25% without the need for a look-up table. The operating frequency of this circuit ranges from 200 to 600 MHz with an input cycle range from 30% to 70%. The circuit was fabricated using the TSMC 0.18-μm CMOS process, has a core area of only 0.0252 mm^2, and provides fast locking (within 7–11 cycles).

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