Study Trapped Charge Distribution in P-Channel Silicon–Oxide–Nitride–Oxide–Silicon Memory Device Using Dynamic Programming Scheme

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Study Trapped Charge Distribution in P-Channel Silicon–Oxide–Nitride–Oxide–Silicon Memory Device Using Dynamic Programming Scheme

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In this study, we precisely investigate the charge distribution in SiN layer by dynamic programming of channel hot hole induced hot electron injection (CHHIHE) in p-channel silicon–oxide–nitride–oxide–silicon (SONOS) memory device. In the dynamic programming scheme, gate voltage is increased as a staircase with fixed step amplitude, which can prohibits the injection of holes in SiN layer. Three-dimensional device simulation is calibrated and is compared with the measured programming characteristics. It is found, for the first time, that the hot electron injection point quickly traverses from drain to source side synchronizing to the expansion of charged area in SiN layer. As a result, the injected charges quickly spread over on the almost whole channel area uniformly during a short programming period, which will afford large tolerance against lateral trapped charge diffusion by baking.

1. Introduction

Conventionally, many studies have been done for the charge distribution in SiN layer during programming in n-channel silicon–oxide–nitride–oxide–silicon (SONOS) devices,[1–4] using several methods,[5–12] such as comparison between sub-threshold and gate induced drain leakage (GIDL) characteristics,[1,6,7] studying V_t difference between forward and reverse read.[4,11,12] These studies have revealed that injected charges were locally concentrated near to drain side until SiN trapped states are fully occupied by trapped charge. After that the trapped charges are extended to the source side,[4] gradually. On the other hands, recently, in order to achieve high performance and highly reliable embedded Flash memory, lots of interests have been focused on p-channel SONOS memory devices.[13–15] Especially, three superior characteristics of p-channel Flash memory (low voltage operation, high speed programming, and low power consumption) have been emphasized.[16,17] In order to achieve hot electron injection in SiN layer, low gate voltage setting is required and makes it possible to attain low voltage operation at the gate. Next, hot electron injection efficiency in p-channel devices can be higher than that in n-channel devices,[18,19] which results in high speed programming and low power consumption. Furthermore, channel electron tunneling erase operation in p-channel device does not produce hot hole injection because of the larger hole barrier height,[19] as long as applied erasing voltage is lower so as not to generate hole injection from substrate. Therefore, hot-hole-free operation scheme in p-channel device further reinforces the reliability.[19] Additionally, dynamic programming scheme with gate voltage staircase pulses has been proposed[15] to achieve higher programming efficiency and low bit-line bias operation. By adopting dynamic programming scheme, memory cell can perform better writing efficiency and suffer less oxide degradation than the constant programming scheme[15] (i.e., apply a fixed voltage on gate), due to the suppression of hot hole injection. However, the trapped charge distribution induced by channel hot hole induced hot electron injection (CHHIHE) in p-channel SONOS device has not been explored yet. In this paper, trapped charge distribution as a function of programming time is studied. At first, experimental forward and reverse current–voltage (I–V) characteristics are calibrated to fit the parameters of numerical three-dimensional device simulations. Next, we investigate the dependence on the programming time of trapped charge distribution with various pulse width and number of pulses for p-channel SONOS device by comparing experimental programming characteristics and simulated I–V characteristics. Following the introduction, Sect. 2 introduces the device structure, bias setting and methodology for studying the electrical characteristic induced by localized charge in p-channel SONOS device. In Sect. 3, the spatial charge distribution of the localized trapped charge is shown.

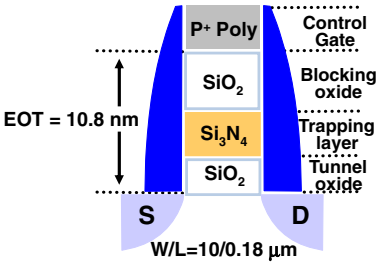


Fig. 1. (Color online) Schematic SONOS device structure used for experiments. The channel length, channel width and EOT of the ONO layer are 0.18 μm, 10 μm, and 10.8 nm, respectively.

2. Device Structure, Bias Setting, and Methodology

Schematic p-channel SONOS device structure under analysis is presented in Fig. 1. The channel length, channel width and equivalent oxide thickness (EOT) of the ONO layer are 0.18 μm, 10 μm, and 10.8 nm, respectively. Figure 2(a) shows the programming window of ΔV_{tR} [i.e., the difference between V_t in reverse read (RR) and the initial state V_t] and ΔV_{tRF} (i.e., the reverse to forward V_t difference). In order to simplify the simulation methodology, we consider an idealized non-uniform distribution, represented by a step function, so that the trapped charge density (T_D) is assumed to have only two possible values in two different regions.

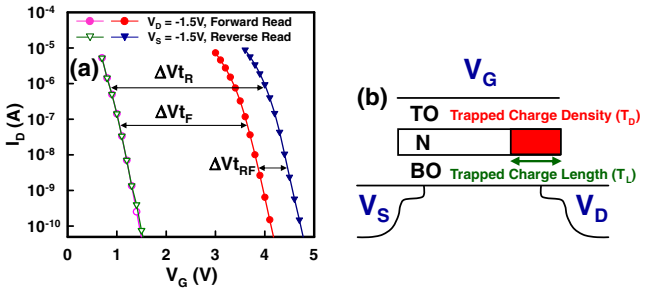


Fig. 2. (Color online) (a) ΔV_{tR} and ΔV_{tF} is the programming window in reverse and forward read condition. ΔV_{tRF} is the reverse to forward V_t difference. (b) The trapped charge density (T_D) and the effective trapped charged length (T_L) are extracted.

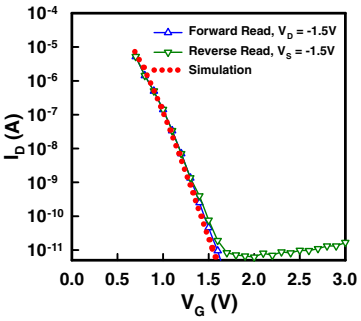
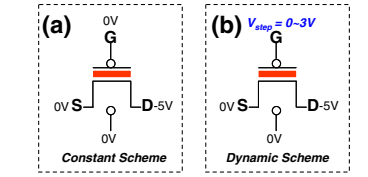
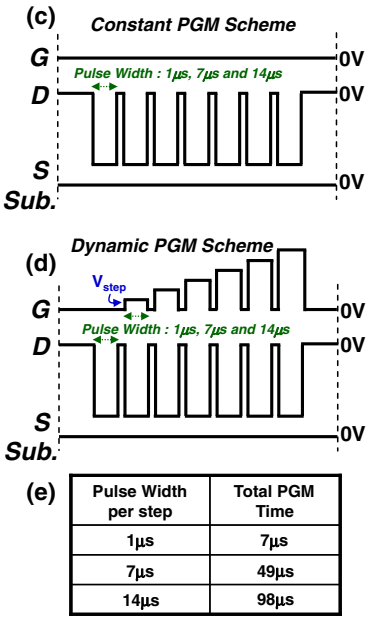


Fig. 4. (Color online) Comparison of the measured and simulated I–V curves in forward and reverse read to verify the initial state condition.





(e)

Pulse Width per step	Total PGM Time
1μs	7μs
7μs	49μs
14μs	98μs

Fig. 3. (Color online) (a, b) Bias setting of constant and dynamic programming scheme. (c, d) Programming waveforms of constant and dynamic programming scheme with various pulses width used in this work. (e) The total programming time with various pulse widths per step.

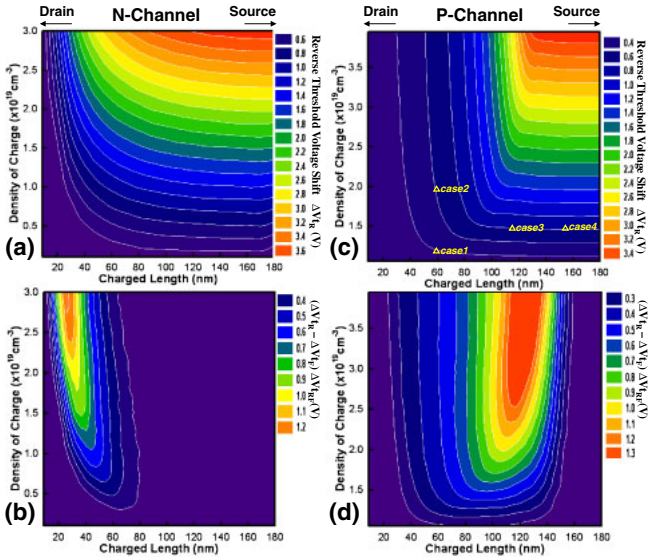


Fig. 5. (Color online) N- and P-channel contour plots of (a) and (c) ΔV_{tR} and (b) and (d) ΔV_{tRF} as a function of the effective trapped charge region and the density of charge.

Then, T_D and the effective trapped charge length (T_L) are extracted, as shown in Fig. 2(b). Figures 3(a) and 3(b) show the bias setting of constant and dynamic programming scheme. Figures 3(c) and 3(d) show the programming waveforms of two schemes with various pulse widths. The increment gate voltage step up pulse is used with seven steps as shown in Figs. 3(c) and 3(d), where three kinds of pulse widths (1, 7, and 14 μs) are examined. Figure 3(e) shows the total programming time with various pulse widths per step.

3. Simulation and Experimental Results

Initial state before programming is prepared by electron tunnel erasing and electrons are uniformly distributed (9.5×10^{18} cm^{-3}) in SiN layer, as shown in Fig. 4. Next, simulated n-channel contour plot of ΔV_{tR} and ΔV_{tRF} as a function of T_L and T_D are exhibited in Figs. 5(a) and 5(b). On the other hands, the simulated p-channel plots are shown in Figs. 5(c) and 5(d). In the case of n-channel device, charges in SiN layer locally concentrate near to drain side to get ΔV_{tRF} more than 1 V, as shown in Fig. 5(b). However, in the case of p-channel device, charges in SiN layer need to be extended into source side to get ΔV_{tRF} more than 1 V, as shown in Fig. 5(d). This difference comes from the formation of local inversion layer in the p-channel device when electrons are injected in SiN layer. Figures 6(a) and 6(b) are simulated channel surface potential associated with the cases 1–4 as marked in Fig. 5(c), where different T_L and T_D are placed. The equivalent value of ΔV_{tR} is observed between case 1 and case 2 or between case 3 and case 4. In comparison of case 1 and case 2, the maximum potential barrier heights are the same even though they have the different T_D. On the other hand, in comparison of case 3 and case 4, the potential barrier heights also are the same in spite of the different T_L. Figure 7 shows the comparison of program transients of the constant and dynamic programming schemes with various pulse width (a) 1, (b) 7, and

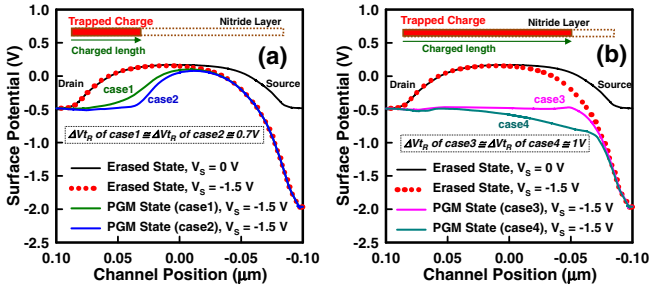


Fig. 6. (Color online) Simulated channel surface potential correspond with [cases 1–4 as marked in Fig. 5(c)].

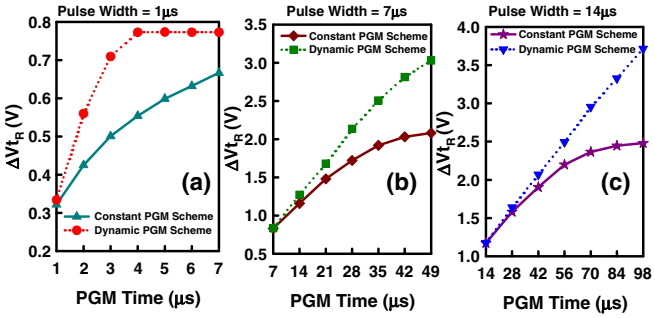


Fig. 7. (Color online) Comparison of program transients of the constant and dynamic programming schemes at various pulse width (a) 1, (b) 7, and (c) 14 μs respectively.

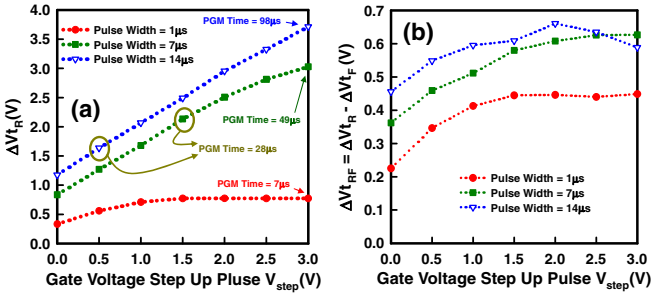


Fig. 8. (Color online) Measured dynamic programming characteristics. (a) Reverse threshold voltage shift and (b) reverse-forward threshold voltage shift versus gate voltage step.

(c) 14 μs, respectively. Dynamic programming scheme has higher programming efficiency than constant programming scheme, where programming efficiency is defined by V_t shift divided by program time, as shown in Fig. 7. Figures 8(a) and 8(b) show the measured ΔV_{tR} and ΔV_{tRF} as a function of gate voltage step up pulse. As shown in Fig. 8(a), pulse width 7 and 14 μs exhibit different V_{th} shift at the same programming time. It indicates that pulse width 7 μs have the best programming efficiency. Figures 9(a) and 9(b) show ΔV_{tR} versus ΔV_{tF} (the difference between V_t in forward read and the initial state V_t) and $\Delta V_{tF}/\Delta V_{tR}$ as a function of programming time for the analysis of charge uniformity. After programming time longer, ΔV_{tR} vs ΔV_{tF} curves approach the line ($\Delta V_{tR} = \Delta V_{tF}$) in both of pulses width 7 and 14 μs. It means that the charges are getting uniformly distributed in SiN layer as program step number increased.

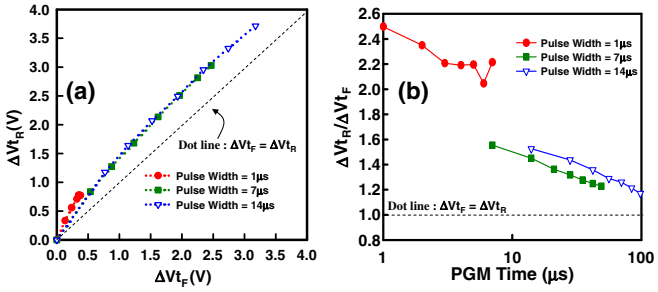


Fig. 9. (Color online) (a) ΔV_{tF} versus ΔV_{tR} and (b) $\Delta V_{tF}/\Delta V_{tR}$ as a function of programming time for the analysis of charge uniformity resulting from various pulse widths, such as 1, 7, and 14 μs respectively.

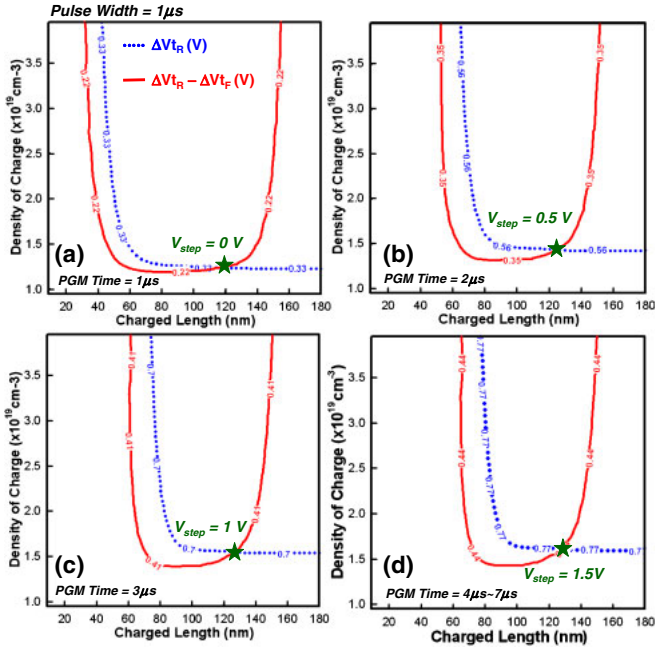


Fig. 10. (Color online) Extract T_L and T_D using contour plot (see Fig. 5) of the cross point between ΔV_{tR} and ΔV_{tRF} with various V condition: (a) 0, (b) 0.5, (c) 1, and (d) 1.5 V.

Cross point of the contour plots between ΔV_{tR} and ΔV_{tRF} show the value of T_D and T_L, as shown in Figs. 10(a)–10(d), where 1 μs pulse width is used. Programming time dependence of T_D and T_L from first ($V_{step} = 0$ V) to fourth ($V_{step} = 1.5$ V) pulses are represented in series from Figs. 10(a) to 10(d). The saturation of the value of ΔV_{tR} and ΔV_{tRF} appears at V_{step} equal to 1.5 V (see Fig. 8), which result in the saturation of the extension of T_D and T_L. Figure 11 shows the simulated trapped charge evolution curve dependent on program step number, coupled to the measured results. In the case of 1 μs pulse width, T_L will extend to SiN layer by applying seven program steps even though it exhibits lower T_D and programming speed (see Fig. 7). Between two pulses width (7 and 14 μs), T_L and T_D have the same trajectory, even though they have the different programming speed. Consequently, it is shown that the trapped charge smoothly extends into the SiN layer in seven program steps. The Electric field associated with different T_L during programming period is shown in Fig. 12. The

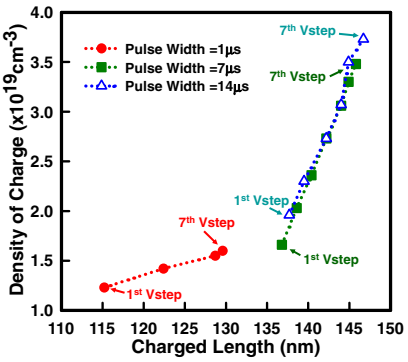


Fig. 11. (Color online) Simulated trapped charge evolution curve depends on program step number using dynamic programming scheme.

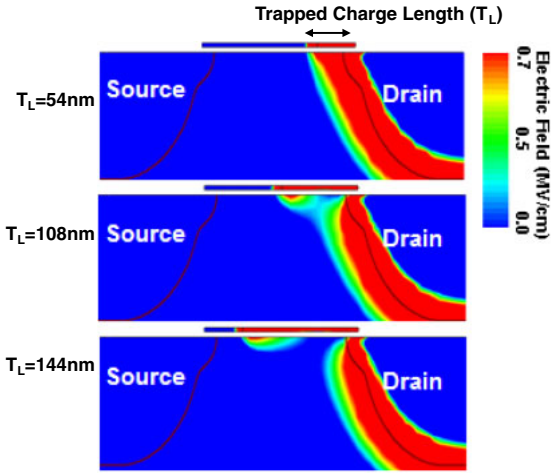


Fig. 12. (Color online) Electric field associated with different T_L during programming period.

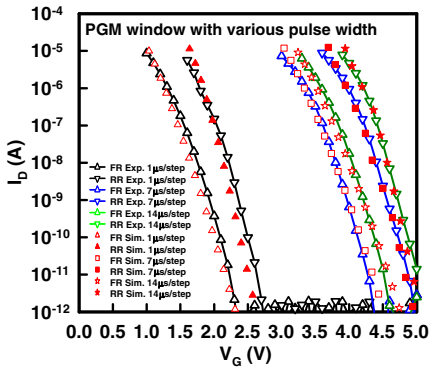


Fig. 13. (Color online) Measured and simulated programming window in forward and reverse read with various pulse widths.

accumulated trapped charges in SiN layer and the pinches-off point below the channel will move from drain side toward source side. Figure 13 shows the measured and simulated programming window in forward and reverse read with various pulse widths. The measured and simulated I–V curves show good agreements. In n-channel device, the V_t is sensitive to T_L. However, in p-channel device, the charge almost uniformly distributed into SiN and the V_t is insensitive to T_L. Consequently, by using FN erase plus CHHIHE programming, uniform charge transfer between the substrate and trapping layer is executed, which will ensure the robust program and erase operation.

4. Conclusions

In this paper, we have quantitatively traced the evolutionary trapped charge distribution induced by various dynamic pulse times in p-channel SONOS device. During a short dynamic programming period, the trapped charges quickly extend into the SiN layer of the whole p-channel based on our result. On the other hand, the channel length self-modulation can reduce the programming stress of gate oxide. This study provides a comprehensive understanding and design guidelines for p-channel SONOS devices.

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