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2013 Jpn. J. Appl. Phys. 52 04CC18

(http://iopscience.iop.org/1347-4065/52/4S/04CC18)

Japanese Journal of Applied Physics **52** (2013) 04CC18 **REGULAR PAPER**
http://dx.doi.org/**10.7567/JJAP.52.04CC18**

A New Methodology for Probing the Electrical Properties of Heavily Phosphorous-Doped Polycrystalline Silicon Nanowires

Horng-Chih Lin[1,2*], Zer-Ming Lin[1], and Tiao-Yuan Huang[1]

[1]*Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan*
[2]*National Nano Device Laboratories, Hsinchu 300, Taiwan*
E-mail: hclin@faculty.nctu.edu.tw

Received September 21, 2012; accepted December 15, 2012; published online March 21, 2013

In this study, we proposed a new methodology for probing the electrical properties of heavily doped polycrystalline silicon (poly-Si) nanowires (NWs), including active doping concentration, mobility, and interface fixed charge density. Implementation of this procedure is based on the modulation of the device operation of a gate-all-around (GAA) junctionless (J-less) transistor from the gated resistor mode to the ungated one. The extracted carrier concentration in the NW is found to be much lower than that of Hall measurements, while a negative fixed charge density is identified with the procedure. Dopant segregation at the oxide interface is postulated to be closely related to these observations.

1. Introduction

Recently, junctionless (J-less) transistors, which have a degenerately doped channel with a doping type identical to that of the source/drain (S/D), have been proposed as an alternative candidate in the manufacturing of extremely scaled metal–oxide–semiconductor (MOS) devices,[1,2] as well as three-dimensional (3D) stacked NAND Flash memory.[3] Such a scheme is not only free from the difficulty in forming shallow and uniform S/D junctions but also shows much reduced parasitic series resistance.[1,2] This is especially important for the 3D architectural Flash memory schemes[3,4] whose S/D doping process is difficult to accomplish with the implant technique. An additional unique feature of the 3D memory structure is the utilization of a polycrystalline silicon (poly-Si) layer as the channel material. In this regard, a novel implantation-free gate-all-around (GAA) poly-Si nanowire (NW) J-less transistor has recently been developed by our group.[5] In this architecture, the complexity of the process could be greatly simplified because the implantation is skipped by employing a heavily in situ phosphorous-doped S/D and channel simultaneously formed by low-pressure chemical vapor deposition (LPCVD), making it very attractive for 3D electronics integration. To optimize the device performance, assessment of the values of active doping concentration and mobility of the in situ doped poly-Si NW is essential. Conventional techniques such as Hall measurement, four-probe technique, and secondary ion mass spectrometry (SIMS) have been widely adopted to characterize the doping properties of poly-Si films.[6–8] However, these methods may not be appropriate for the poly-Si NW structure, as they do not take into account the effects drawn by the surface of the NW and dopant segregation.[9] In one of the previous works,[10] the active doping concentration of in situ phosphorous-doped Si NWs was studied. However, the value of mobility used in the analysis for extracting the carrier concentration was approximated by the result of the Hall measurement, leading one to question the accuracy of the analysis. In this work, we propose a new methodology to extract major parameters, such as the active doping concentration and mobility of the NW channel as well as the fixed-charge density of NWs, based on the concept of the switching in device operation characteristics between gated- and ungated-resistor behaviors of J-less transistors.

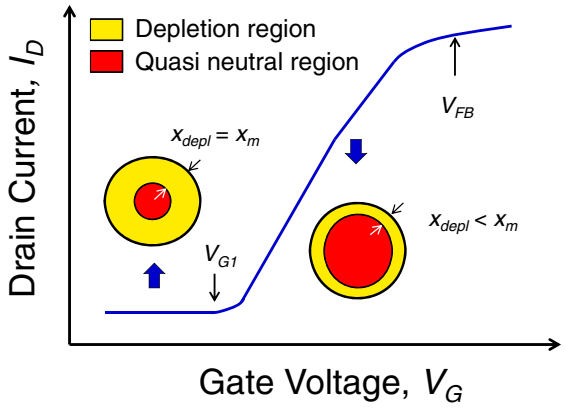

Fig. 1. (Color online) Schematic illustration of the transfer characteristics of a GAA J-less transistor with a rather thick round NW channel. The device is normally on due to the high channel doping and the drain current starts to decrease as the gate voltage decreases from V_{FB} due to the formation of a surface depletion layer with a width of X_{depl}. However, the current will reach a lower bound as X_{depl} reaches a maximum value X_m.

The remaining part of this paper is organized as follows: In Sect. 2, we present the impact of NW cross-sectional area on the device characteristics and discuss the operation of the J-less devices, including the interesting leaky characteristics of the NW devices with a rather large cross-sectional area. Then, a theoretical model is detailed in Sect. 3 to establish the relations among different parameters. In Sect. 4, the above theoretical background is verified with experimental results. A method for determining the gate voltages corresponding to the switching of transport behaviors is also presented. Results of the major parameters extracted by the developed procedure are further discussed. Finally, Sect. 5 summarizes the major contributions and observations of this work.

2. Impact of the Cross-sectional Area of Nanowires

Figure 1 schematically shows the transfer curve of a GAA n-channel J-less transistor. For simplicity, the cross section of the NW channel is assumed to be round, with a sufficiently large diameter so that it will not be fully depleted

even if a highly negative gate voltage is applied (see discussion later). Certainly, the operation of the device is quite different from that of conventional inversion mode transistors considering the channel doping, which is very high and of the same type as that of the source and drain. Such a feature is structurally similar to the accumulation-mode (AM) devices.[11–14] However, although bearing some resemblance to the AM device at first glance, the J-less device is actually quite different in terms of the operation characteristics. Specifically, conventional AM transistors usually adopt a channel doping concentration (e.g., 4×10^{16} and $5 \times 10^{17}\,\mathrm{cm}^{-3}$)[11,12] far lower than that of the S/D region, albeit with the same doping type. So, as the device is turned on, the drain current (I_D) conduction takes place in an accumulation layer (carrier concentration typically $\geqq 10^{19}\,\mathrm{cm}^{-3} \gg$ channel doping) formed in the channel surface near the oxide interface. In contrast, the channel doping concentration of J-less devices is typically about or higher than $1 \times 10^{19}\,\mathrm{cm}^{-3}$,[1,2] making the operation distinctly different from those of conventional AM and inversion-mode (IM) devices. This can be understood from Fig. 1 in which the flat-band voltage (V_{FB}) corresponds to a point in the transfer curve in the regime of the on-state operation.[15] As the gate voltage (V_G) decreases from V_{FB}, a surface depletion region starts to form in the NW channel, so the NW can be roughly divided into the surface depletion and quasi neutral regions, as shown in Fig. 1. Note that, because of the high carrier concentration in the quasi neutral region, the current conduction of the J-less devices is mainly through the channel body rather than being confined to a region near the oxide interface, in strong contrast to that of the AM devices.

As V_G further decreases, the depletion region is widened and thus leads to a reduction in I_D owing to the shrinkage of the effective conduction area (i.e., the quasi neutral region) of the channel. This implies that the off-state current of the J-less devices is strongly dependent on the cross-sectional feature size of the NW channel. Specifically, if the NW size is not small enough to allow full depletion of the NW by the highly negative gate bias, the lower bound of the leakage current will be set by the component conducting through the quasi neutral region remaining in the core of the NW channel, as shown in Fig. 1. Another fact that should be noted is that the voltage drop in the depletion region of a heavily doped semiconductor is limited by its band gap.[16] For heavily doped Si, the band gap is about 1 eV.[17] This means that the width of the depletion region (X_{depl}) has an upper limit. As a result, a rather thick NW channel will not be fully depleted even under a highly negative gate bias, and the quasi neutral region remaining in the middle of the channel continues to allow current to conduct through. This occurs as V_G reduces to a specific value denoted as V_{G1} in Fig. 1, where X_{depl} reaches its maximum (X_m). In the regime $V_G < V_{G1}$, the quasi neutral region becomes "ungated" since its cross-sectional area is basically no longer affected by the gate bias. As a result, the leakage current remains constant in this regime, as shown in Fig. 1. To effectively shut down the conduction when the device is off, the quasi neutral region in the channel core should be eliminated. This explains why a J-less device demands its channel to be ultrathin or tiny to acquire a high on/off current ratio in operation.[1,2,5] Nonetheless, the methodology developed in this work shows that useful information is still contained in the leakage characteristics of J-less devices with a rather thick channel body.

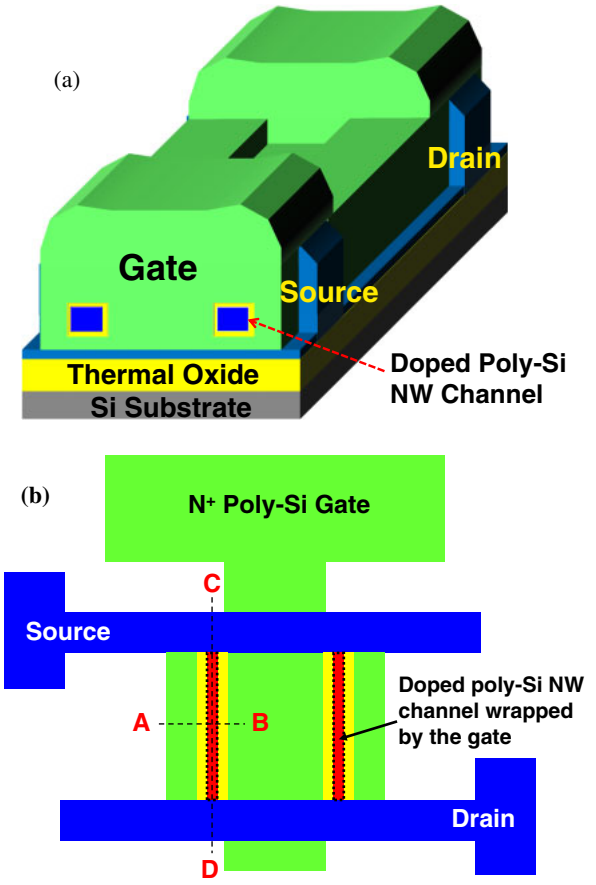

Fig. 2. (Color online) (a) Stereo and (b) top views of the fabricated GAA J-less poly-Si NW transistor. In the top view, the NW channels wrapped by the gate are intentionally shown.

To confirm the aforementioned inferences, we characterize the GAA J-less transistors with in situ phosphorous-doped poly-Si NW channels of different cross-sectional areas. The 3D schematic structure and top view of the fabricated GAA J-less transistors are shown in Figs. 2(a) and 2(b), respectively. As can be seen in the figures, a pair of n^+ poly-Si NW channels is gated with an n^+ poly-Si gate thus normally-on device characteristics are expected. The fabrication flow of the characterized devices is described in Ref. 5. In this work, two types of device with different cross-sectional NW dimensions were fabricated and characterized. Figure 3 shows the cross-sectional scanning electron microscopy (SEM) image of one of them, denoted as Device A, which has a rectangular-shaped cross section with an area of $70 \times 27\,\mathrm{nm}^2$. Figure 4(a) compares the transfer characteristics of Device A with those of a device (denoted as Device B) characterized in the previous work[5] with a much smaller cross-sectional area of approximately $23 \times 12\,\mathrm{nm}^2$. The strong impact drawn by the NW size can be clearly seen in Fig. 4(a). Device A shows very leaky characteristics and unapparent switching behavior. In contrast, sharply off characteristics are observed for Device B, and the minimum I_D of the transfer curves in the off-state regime is comparable to or lower than the

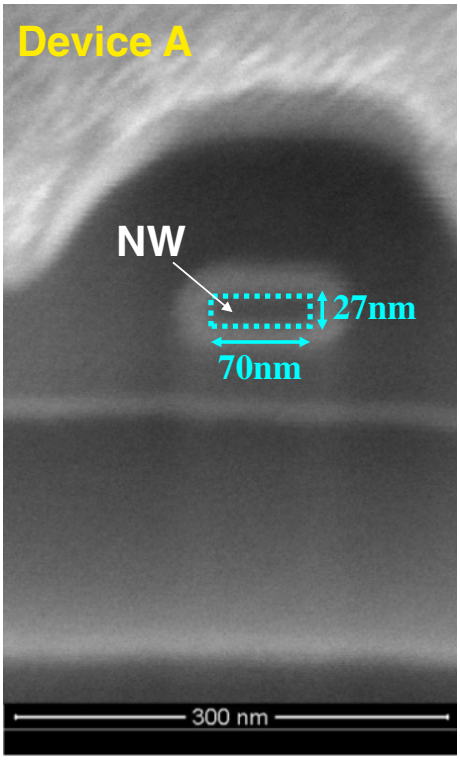

Fig. 3. (Color online) Cross-sectional SEM image of Device A along line AB shown in Fig. 2(b). This device has a rectangular-shaped cross section with an area of $70 \times 27\,\mathrm{nm}^2$.

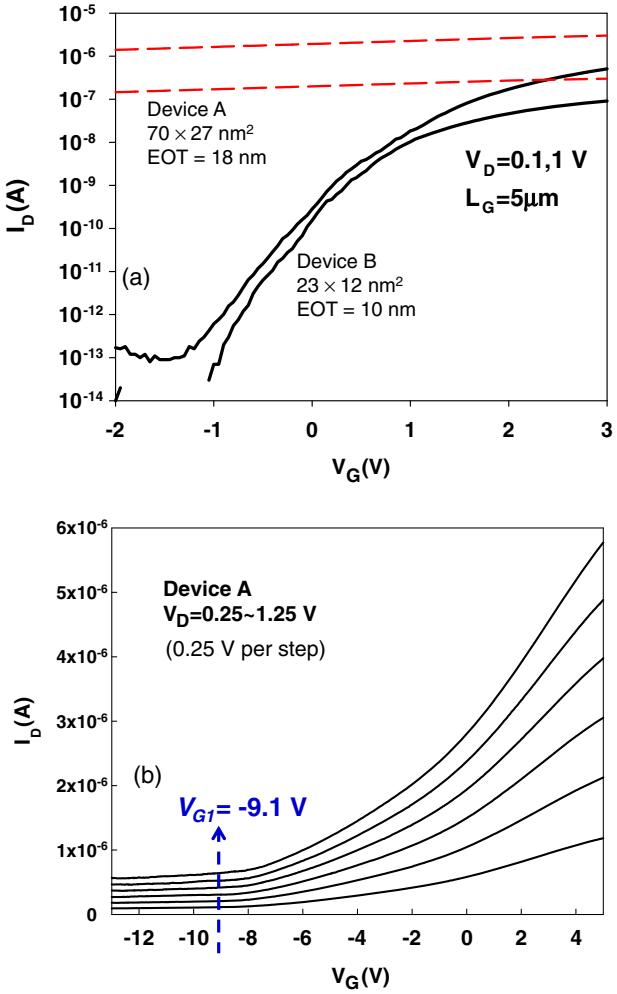

Fig. 4. (Color online) (a) I_D–V_G characteristics of Devices A and B. Device B has a much smaller cross-sectional area of around $23 \times 12\,\mathrm{nm}^2$.[5] (b) Transfer characteristics of Device A measured at various V_D values. The device behaves like an ungated resistor when V_G is smaller than $-9.1\,\mathrm{V}$.

sensitivity ($\sim 10^{-13}\,\mathrm{A}$) of the measurement system. Such a finding is reasonable considering the fact that the tiny NW size of Device B allows the effective depletion of the whole channels and thus the complete shut-down of the current conduction when the device is off.[1,2]

To confirm the existence of the ungated region in the operation of the device with sufficiently large NWs, the I_D–V_G characteristics of Device A, measured in a highly negative V_G regime at V_D ranging from 0.25–1.25 V are shown in Fig. 4(b). In the figure, as expected, two distinct regions can be identified and divided by V_G at $-9.1\,\mathrm{V}$, which is denoted as V_{G1} in Fig. 1. (Precise determination of V_{G1} is given in Sect. 4.) As V_G is smaller than $-9.1\,\mathrm{V}$, I_D is essentially independent of V_G and linearly proportional to V_D. These features indicate that the conduction is resistor-like and no longer governed by the applied gate bias.

Although Device A with wider poly-Si NW channels could not be turned off effectively, its transfer characteristics are cleverly analyzed to acquire the active doping concentration and mobility of the in situ phosphorous-doped poly-Si NWs. Details about the methodology including theoretical analysis and experimental verification are elaborated in the next sections.

3. Theoretical Background

The cross-sectional view of the device along line A–B shown in Fig. 2(b) is plotted in Fig. 5, where H, W, EOT, and n denote the height, width, effective oxide thickness, and active doping (or carrier) concentration of the heavily phosphorous-doped poly-Si NW channel, respectively. As has been pointed out in the discussion of Fig. 1, a surface depletion region exists as V_G is smaller than V_{FB}. Owing to the rather thick structure and the heavy channel doping, the investigated Device A is partially depleted during off-state operation and the maximum depletion width X_m is expected to be much smaller than both H and W. This allows us to use the 1D Poisson's equation to calculate the electric potential in the depletion region at a position far from the corners shown in Fig. 5. The 1D Poisson's equation along the x-direction [Fig. 2(b)] is expressed as

$$\frac{d^2\Phi(x)}{dx^2} = \frac{-qn}{\varepsilon_{Si}}, \tag{1}$$

where Φ is the electric potential, ε_{Si} is the dielectric constant of silicon, and q is the electric charge. In Fig. 5, $x = 0$ corresponds to the interface between the top gate oxide and the NW channel. The two boundary conditions applied for solving Eq. (1) are listed below:

$$E(x = X_{depl}) = 0, \tag{2}$$

$$\Phi(x = X_{depl}) = 0, \tag{3}$$

where $E(x = X_{depl})$ and $\Phi(x = X_{depl})$ are the electric field and electric potential, respectively, at the edge of the depletion region. Here, we assume that the applied V_D is

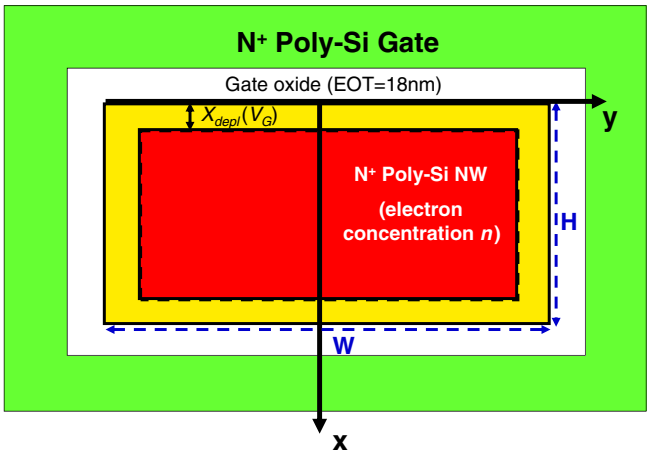

Fig. 5. (Color online) Schematic illustration of the cross-sectional structure of the GAA J-less transistor when $V_G < V_{FB}$ along line AB shown in Fig. 2(b).

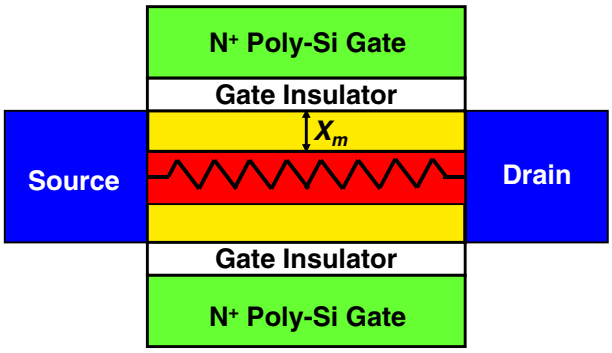

Fig. 6. (Color online) Schematic illustration of the cross-sectional structure of the GAA J-less transistor when $V_G < V_{G1}$ along line CD shown in Fig. 2(b).

small, so its impact on the potential and electric field is negligible. By applying the two boundary conditions to solve Eq. (1), the solution of electric potential can be expressed as

$$\Phi(x) = \frac{qnX_{\mathrm{depl}}}{\varepsilon_{\mathrm{Si}}}x - \frac{qn(x^2 + {X_{\mathrm{depl}}}^2)}{2\varepsilon_{\mathrm{Si}}}, \quad 0 < x \le X_{\mathrm{depl}}. \quad (4)$$

To turn off an n-channel J-less transistor, the gate bias is decreased to increase X_{depl} and thus decreases the area of the quasi neutral region in the NW core available for current conduction. As mentioned above, X_{depl} is limited by the maximum voltage drop in the NW, which is close to the band gap of Si.[16] The maximum depletion width, X_{m}, and the gate voltage as X_{m} is reached, V_{G1}, can be expressed as follows:[17]

$$X_{\mathrm{m}} = \sqrt{2\varepsilon_{\mathrm{Si}}\frac{E_{\mathrm{g}}/2 + kT/q\ln(n/n_{\mathrm{i}})}{qn}}, \quad (5)$$

$$V_{\mathrm{G1}} = V_{\mathrm{FB}} - \frac{qnX_{\mathrm{m}}}{C_{\mathrm{ox}}} - \frac{E_{\mathrm{g}}}{2} + \frac{kT}{q}\ln\left(\frac{n}{n_{\mathrm{i}}}\right), \quad (6)$$

$$V_{\mathrm{FB}} = \frac{E_{\mathrm{g}}}{2} - \frac{kT}{q}\ln\left(\frac{n}{n_{\mathrm{i}}}\right) - \frac{Q_{\mathrm{fix}}}{C_{\mathrm{ox}}}, \quad (7)$$

where Q_{fix}, C_{ox}, n_{i}, E_{g}, and kT/q are the fixed charges at the oxide/channel interface, gate oxide capacitance per unit area, intrinsic carrier concentration, silicon band gap, and thermal energy at room temperature, respectively. As V_{G} is more negative than V_{G1}, X_{m} is reached and retained. In other words, the device operation changes from a gated resistor (as $V_{\mathrm{G}} > V_{\mathrm{G1}}$) to an ungated one (as $V_{\mathrm{G}} < V_{\mathrm{G1}}$) in which the current flow is conducted through the quasi-neutral core region with a conduction area not affected by the gate bias. Figure 6 shows the cross section along the C–D cutline (i.e., along the source-to-drain direction) in Fig. 2(b) showing the situation as X_{m} is reached. For a long-channel device operated at a low V_{D}, X_{m} should be quite uniform across the channel and, from Fig. 5, the area for the leakage current of the ungated resistor to conduct can be approximated as $H \times W - 2(H + W)X_{\mathrm{m}} + 4{X_{\mathrm{m}}}^2$. Thus, the resistance of the ungated resistor, R, can be expressed with the following form:

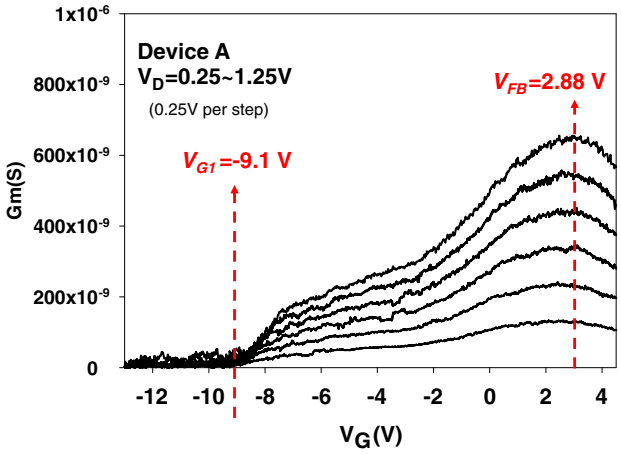

Fig. 7. (Color online) G_{m} versus V_{G} for Device A measured at various V_{D} values. V_{G1} and V_{FB} can be precisely determined from the plots.

$$R = \frac{V_{\mathrm{D}}}{I_{\mathrm{D}}} = \frac{L}{nq\mu(H \times W - 2(H + W)X_{\mathrm{m}} + 4{X_{\mathrm{m}}}^2)}, \quad (8)$$

where μ is the effective mobility. R can be obtained from the information contained in the ungated operation regime, i.e., $V_{\mathrm{G}} < V_{\mathrm{G1}}$.

4. Experimental Verification and Discussion

In Fig. 4(b), more precise determination of V_{G1} could be achieved by plotting the transconductance (G_{m}) as a function of V_{G}, and the results are shown in Fig. 7. Since G_{m} is the differentiation of I_{D} to V_{G}, it should suddenly drop to zero when the conduction of the device transfers from gated- to ungated-resistor behavior. This transition indeed occurs in the figure, and V_{G1} can be extracted as the gate voltage when G_{m} drops to zero, which is -9.1 V in this case. Moreover, V_{FB} can also be determined as the gate voltage corresponding to the G_{m} peaks in Fig. 7. The major reason is as follows. As mentioned above, the depletion region exists as V_{G} is smaller than V_{FB}, and contributes to the additional equivalent oxide thickness (EOT_{depl}) of the gate dielectric:[16]

$$EOT_{\mathrm{depl}} = \frac{X_{\mathrm{depl}}\varepsilon_{\mathrm{SiO_2}}}{\varepsilon_{\mathrm{Si}}}. \quad (9)$$

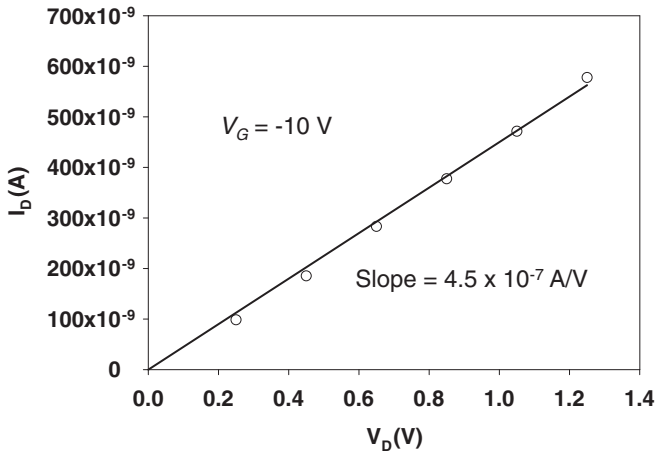

Fig. 8. I_D extracted from Fig. 4(b) at $V_G = -10$ V as a function of V_D.

The additional EOT contributed by X_{depl} decreases with increasing V_G, one of the two major reasons responsible for the increase in G_m as $V_G < V_{FB}$. The other reason is the increase in the conduction area of the quasi neutral region. When V_{FB} is reached, the two mechanisms quench. The further increase in I_D when V_G is larger than V_{FB} is due to the conduction through the surface accumulation layer and the conduction has a much weaker dependence on V_G as compared with the aforementioned two mechanisms. Therefore, the peak of G_m is resulted at V_{FB}. From Fig. 7, it is seen that the V_G corresponding to G_m peaks shows a very weak dependence on the applied V_D, and the corresponding V_G (2.88 V) is determined to be V_{FB}. With this value, a negative fixed charge density (Q_{fix}) of -3.25×10^{12} cm^{-2} can be extracted from Eq. (7). Next, the active doping concentration (n) of the doped poly-Si NW can be extracted to be 1.18×10^{19} cm^{-3} by substituting the V_{G1} and V_{FB} values into Eq. (6).

To extract R and μ, I_D in Fig. 4(b) measured at $V_G = -10$ V is re-plotted and shown as a function of V_D in Fig. 8. In this figure, it can be seen that the current is proportional to the drain voltage and its slope, which is equal to $1/R$, is 4.5×10^{-7} A/V. On the basis of this result and Eq. (8), the mobility of the doped poly-Si NW of Device A is determined to be 52.5 cm^2 V^{-1} s^{-1}. Note that, on the basis of the extracted n value, the estimated X_m is around 10 nm, which is much smaller than W (= 70 nm) and H (= 27 nm) of the NW and supports the assumption made for the derivation of Eq. (8).

Table I lists the measured results from SIMS, Hall measurements, and the proposed methodology. Both SIMS and Hall measurements were performed on a 400-nm-thick blanket film. Note that the carrier concentration measured from Hall measurements is smaller than the dopant concentration obtained from the SIMS analysis, indicating the occurrence of dopant precipitation and segregation. More importantly, the carrier concentration is further reduced in the NW sample. One possible explanation for this observation is the segregation of phosphorous atoms to the oxide interface from the poly-Si NW.[9,18] A reduction in the concentration of phosphorous in the Si material may also explain the increase in the effective carrier mobility of the NW sample as compared with the Hall mobility.

Table I. Results of SIMS, Hall measurements, and the proposed methodology.

	SIMS	Hall	This work
Test structure	Blanket thin film[a)]	Blanket thin film[a)]	NW J-less transistor
Dopant or carrier concentration (cm^{-3})	10^{20}	7×10^{19}	1.18×10^{19}
Mobility (cm^2 V^{-1} s^{-1})	—	42.7	52.5

a) 400 nm thick.

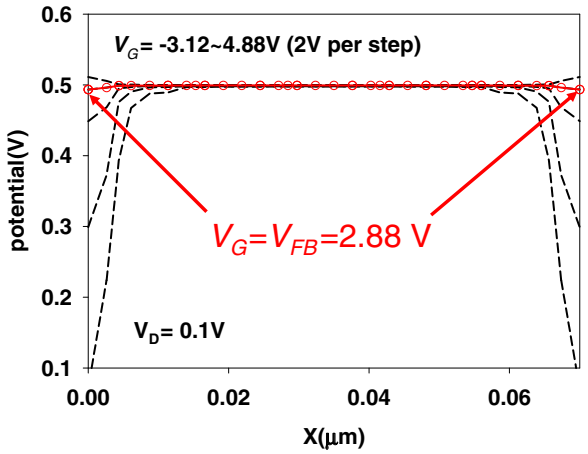

Fig. 9. (Color online) Simulated electric potential distributions in the middle of the NW along the y-axis at $V_D = 0.1$ V and various V_G values. The result shown for $V_G = 2.88$ V confirms the flat-band condition.

To further verify the accuracy of the methodology proposed in Fig. 7 for determining V_{FB}, we simulate the electric potential across the middle of the NW along the y-direction (see Fig. 5) under various gate bias conditions with a TCAD tool.[19] In the simulation, the n and Q_{fix} extracted from the above procedure are taken into account and the results are shown in Fig. 9. It can be seen that the electric potential is almost flat at $V_G = 2.88$ V, confirming the feature of flat-band condition. Note that the negative value of Q_{fix} is reported for the first time. Certainly, its origin needs more efforts to be unveiled, but the aforementioned segregation of phosphorous to the oxide interface should play an essential role in such a finding. Finally, although the NW material studied in this study is polycrystalline in nature, there should be no doubt about the applicability of this scheme to monocrystalline NWs.

5. Conclusions

A simple procedure without a complicated or expensive measurement setup is proposed in this study to extract the major electrical properties of in situ phosphorous-doped poly-Si NWs, including the effective active doping concentration, mobility, and interface fixed charge density. The principles of this methodology rely on the operation of a GAA J-less transistor with rather thick NW cross-sectional dimensions. Such a device exhibits an ungated operation behavior when gate bias is sufficiently negative, i.e., $V_G \leqq V_{G1}$, which is clearly observed in the practical measurements. Moreover, the gate voltage corresponding to V_{G1} and V_{FB} can be precisely determined from the G_m-vs-V_G plots.

Mobility could also be determined from the characteristics of the GAA J-less transistor operated in the ungated-resistor region. The extracted carrier concentration is significantly lower than that obtained from Hall measurements performed on blanket thin films. Segregation of phosphorous at the gate oxide/NW interface is postulated to be the major reason for the observed disparity. We have also identified the presence of negative fixed charges at the oxide interface, which is likely related to the dopant segregation as well.

Acknowledgments

The authors would like to thank the National Nano Device Laboratories (NDL) and the Nano Facility Center of the NCTU for assistance in device fabrication. This work was supported in part by the Ministry of Education in Taiwan under the ATU Program, and the National Science Council under contract No. NSC 99-2221-E-009-172 and No. NSC 99-2221-E-009-167-MY3.

1) C. W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J. P. Colinge: Solid-State Electron. **54** (2010) 97.
2) J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy: Nat. Nanotechnol. **5** (2010) 225.
3) H. T. Lue, T. H. Hsu, Y. H. Hsiao, S. P. Hong, M. T. Wu, F. H. Hsu, N. Z. Lien, S. Y. Wang, J. Y. Hsieh, L. W. Yang, T. Yang, K. C. Chen, K. Y. Hsieh, and C. Y. Lu: Symp. VLSI Technology Dig. Tech. Pap., 2010, p. 131.
4) R. Katsumata, M. Kito, Y. Fukuzumi, M. Kido, H. Tanaka, Y. Komori, M. Ishiduki, J. Matsunami, T. Fujiwara, Y. Nagata, L. Zhang, Y. Iwata, R. Kirisawa, H. Aochi, and A. Nitayama: Symp. VLSI Technology Dig. Tech. Pap., 2009, p. 136.
5) C. J. Su, T. I. Tsai, Y. L. Liou, Z. M. Lin, H. C. Lin, and T. S. Chao: IEEE Electron Device Lett. **32** (2011) 521.
6) J. Y. W. Seto: J. Appl. Phys. **46** (1975) 5247.
7) N. D. Arora, J. R. Hauser, and D. J. Roulston: IEEE Trans. Electron Devices **29** (1982) 292.
8) G. Masetti, M. Severi, and S. Solmi: IEEE Trans. Electron Devices **30** (1983) 764.
9) R. D. Chang and J. R. Tsai: J. Appl. Phys. **103** (2008) 053517.
10) H. Schmid, M. T. Björk, J. Knoch, and H. Riel: Nano Lett. **9** (2009) 173.
11) W. Cheng, A. Teramoto, M. Hirayama, S. Sugawa, and T. Ohmi: Jpn. J. Appl. Phys. **45** (2006) 3110.
12) A. Terao, D. Flandre, E. Lora-Tomayo, and F. Van der Wiele: IEEE Electron Device Lett. **12** (1991) 682.
13) A. L. P. Rotondaro, U. K. Magnusson, C. Claeys, D. Flandre, A. Terao, and J.-P. Colinge: IEEE Trans. Electron Devices **40** (1993) 727.
14) Z. M. Lin, H. C. Lin, and T. Y. Huang: Jpn. J. Appl. Phys. **51** (2012) 064301.
15) J. P. Colinge: Silicon Nanoelectronics Workshop, 2011, p. 69.
16) K. F. Schuegraf, C. C. King, and C. Hu: Symp. VLSI Technology Dig. Tech. Pap., 1992, p. 18.
17) Y. Taur and T. H. Ning: *Fundamentals of Modern VLSI Devices* (Cambridge University Press, Cambridge, U.K., 2009) 2nd ed., p. 91.
18) R. D. Chang, C. C. Ma, and J. R. Tsai: Semicond. Sci. Technol. **28** (2010) 1158.
19) DESSIS software manual (Synopsis International, 2004).