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Low Operation Voltage InGaZnO Thin Film Transistors with $LaAlO_3$ Gate Dielectric Incorporation

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In this paper, we report low operation voltage indium gallium zinc oxide (IGZO) thin film transistors (TFTs) incorporating a high-κ lanthanum aluminum oxide ($LaAlO_3$) as gate dielectric. Good TFT characteristics were achieved simultaneously, including a small subthreshold swing (*SS*) of 98 mV/dec, a low threshold voltage (V_t) of 0.29 V, a good on-off-state drive current ratio (I_{on}/I_{off}) of 1.1×10^5, and field effect mobility (μ_{FE}) of 5.4 $cm^2/V \cdot sec$. These good performances are related to the high gate capacitance density and small equivalent oxide thickness (EOT) provided by the high-κ $LaAlO_3$ dielectric. Moreover, the effects of oxygen partial pressure during IGZO deposition process on the device characteristics were investigated. The small *SS* and low V_t allow the devices to be used at operation voltage as low as 1.5 V, which shows the great potential for future high speed and low power applications.
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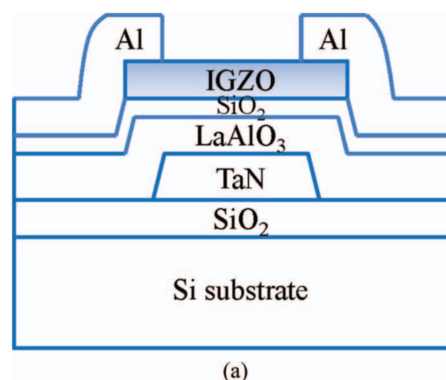
With the rapid development of active-matrix flat panel displays (AMFPDs), thin film transistor (TFT) technologies have been widely used for display applications. However, the traditional Si TFTs using amorphous silicon and poly-crystalline silicon as active channel layer face difficulties due to physical drawback properties.[1–3] Recently, the new TFTs with transparent oxide semiconductors have attracted much attention as potential candidates, due to their unique optical and electrical advantages as compared to conventional Si TFTs, such as high mobility, low cost, excellent uniformity, and good transparency to visible light.[4–25] Particularly, indium gallium zinc oxide (IGZO) TFT[7–25] with superior stability and performance is one of the most promising candidates and has been widely studied. Moreover, the IGZO TFTs can be processed with very low thermal budget and used in emerging flexible display applications.

With the above merits of IGZO film, the IGZO TFT devices are being considered for a variety of applications, such as low-cost large-area displays, RFIDs and wearable electronics.[7,8] For high-speed display circuits, it requires TFTs to operate at low voltages and high drive currents with low threshold voltage (V_t) and small subthreshold swing (*SS*), which make low operation voltage TFTs very favorable for efficiency improvement and environment energy conservation. To address these concerns, incorporating high-κ gate dielectric into TFT provides an alternative solution to achieve these goals.[26–28] In this paper, we report a low operation voltage IGZO TFT by introducing a high-κ lanthanum aluminum oxide ($LaAlO_3$)[28–30] as gate dielectric. Due to the higher κ-value (∼23) of $LaAlO_3$ dielectric as compared to that of SiO_2 (∼3.9), the gate capacitance density increases, which lowers the V_t and improves the gate leakage current. Besides, the $LaAlO_3$ dielectric has good reliability of low bias temperature instability among high-κ devices. The $LaAlO_3$ TFTs showed a small *SS* of 98 mV/dec, a low V_t of 0.29 V, good on-off-state drive current ratio (I_{on}/I_{off}) of 1.1×10^5, and field effect mobility (μ_{FE}) of 5.4 $cm^2/V \cdot sec$ at the operation voltage as low as 1.5 V. Furthermore, the influences of oxygen partial pressure during IGZO film deposition process on the device characteristics were investigated, since IGZO has electrons as majority carriers, which is mainly affected by the oxygen vacancies.[31] The present results demonstrate that IGZO TFTs with high-κ $LaAlO_3$ as gate dielectric has great promise in future high speed and low power applications.

Experimental

Figure 1a and 1b show the schematic cross-sectional structure and microscopic image of the IGZO TFT device, respectively. The channel width (*W*) and length (*L*) of the TFTs were 500 μm and 50 μm, respectively. Bottom-gate top-contact IGZO TFTs were fabricated on an insulated SiO_2/Si substrate through a four-shadow-mask process flow. Firstly, a 50 nm TaN was deposited by physical vapor deposition (PVD) and patterned as gate (G) electrode. Next, a 30 nm $LaAlO_3$ and a 10 nm SiO_2 were deposited by PVD as gate dielectrics, followed by a 400°C O_2 annealing to improve the gate oxide quality. Sequentially, a 40 nm IGZO was formed as active channel layer by dc reactive sputtering using an IGZO target with a power of 80 W and an oxygen partial pressure of $P_{O2} = 50\%$ in Ar and O_2 mixed gas ambient under a working pressure of 7.6 mTorr at room temperature. Here, oxygen partial pressure of P_{O2} (%) is defined as the mixing ratio of O_2 / (O_2 + Ar). Finally, Al source (S)/drain (D) electrodes of 300 nm



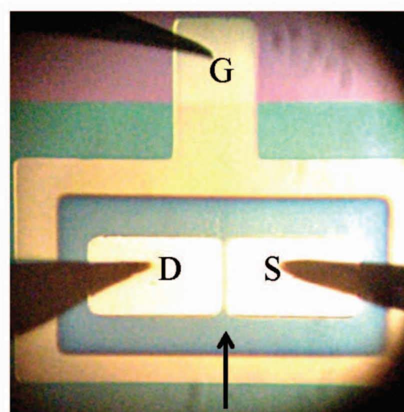


Figure 1. (a) Schematic cross-sectional structure and (b) microscopic image of the IGZO TFT device with $LaAlO_3$ gate dielectric incorporation.

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were deposited, followed by sintering at 300°C in N_2 ambient to reduce the contact resistance. The control samples of IGZO/$LaAlO_3$ TFT without SiO_2 layer insertion were fabricated for comparison. To further evaluate the effects of oxygen partial pressure during IGZO deposition on the device characteristics, the TFT devices with P_{O2} of 33% and 0% in IGZO deposition were also fabricated. The metal-insulator-metal (MIM) capacitors were also fabricated to investigate gate dielectric. The TFT devices were characterized by current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements using HP4156C semiconductor parameter analyzer.

Results and Discussion

Figure 2a and 2b show the *C-V* and *J-V* characteristics of the TaN/$LaAlO_3$/Al and TaN/$LaAlO_3$/SiO_2/Al gate capacitors on the same substrate, respectively. The high capacitance density of ~0.62 μF/cm^2 and ~0.23 μF/cm^2 was measured for the TaN/$LaAlO_3$/Al and TaN/$LaAlO_3$/SiO_2/Al MIM capacitors, respectively. It indicates an equivalent oxide thickness (EOT) of ~5.5 nm and ~15 nm for single $LaAlO_3$ and bilayer $LaAlO_3$/SiO_2 gate dielectrics, respectively, giving a high κ-value of ~21–23 in the $LaAlO_3$ dielectric. Such large gate capacitance density can give the advantages of lowering the operation voltage, increasing the transistor drive current, and improving the I_{on}/I_{off}. Besides, the large gate leakage of 6.9×10^{-6} A/cm^2 at −2 V bias was significantly decreased to 1.5×10^{-7} A/cm^2 after the insertion of SiO_2 layer. This SiO_2 layer evaporated at room temperature without sputtering plasma damage can effectively reduce interface state near the IGZO active channel layer.[23,24]

The output I_d-V_d characteristics of the IGZO/SiO_2/$LaAlO_3$ TFT when P_{O2} = 50% are shown in Figure 3a. An enhancement-mode behavior with good saturation characteristics was well observed even under an operation voltage as low as 1.5 V, which could enable energy saving for low power application. Figure 3b displays the transfer I_d-V_g characteristics of the IGZO/$LaAlO_3$ and IGZO/SiO_2/$LaAlO_3$ TFTs when P_{O2} = 50% for a V_d of 0.4 V, along with the $I_d^{1/2}$ versus V_g plot. For the TFT device characteristics, V_t can be determined from the linear $I_d^{1/2}$-V_g curve and I_{on}/I_{off} can be obtained from the I_d-V_g curve. Besides, μ_{FE} can be extracted from a gradual channel approximation in the linear region using the equation:[32]

$$\mu_{FE} = \partial I_d/\partial V_g \cdot L/(W \cdot V_d \cdot C_g), \quad [1]$$

where I_d, V_d, V_g, L, W, and C_g are the drain current, drain voltage, gate voltage, channel length, channel width, and gate insulator capacitance per unit area, respectively. For the IGZO/$LaAlO_3$ TFT device, it shows a V_t of 0.41 V and a low operation voltage of 1.5 V, but suffers a low I_{on}/I_{off} of 1.4×10^3, a small μ_{FE} of 1.3 cm^2/V · sec and a large *SS* of 390 mV/dec. In contrast, the IGZO/SiO_2/$LaAlO_3$ TFT device exhibits a much larger μ_{FE} of 5.4 cm^2/V · sec and a higher I_{on}/I_{off} of 1.1×10^5 due to small gate leakage current, with a V_t of 0.29 V. Besides, a much smaller *SS* of 98 mV/dec is achieved in the IGZO/SiO_2/$LaAlO_3$ TFT device and closed to the theoretical minimum value of 60 mV/dec at room temperature, indicating the device can be switched on fast at very low operation voltage. These good performances can be attributed to the insertion of SiO_2 layer, which is necessary for stable operation of TFT devices.[23,24,33] By introducing smooth SiO_2 layer insertion, the high-κ surface can be passivated and the interface trap issue can be effectively reduced, thus the performances can be improved, as reported in the literatures.[23,24]

To further investigate the influences of oxygen partial pressure during IGZO deposition process, the IGZO/SiO_2/$LaAlO_3$ TFT device characteristics with the IGZO active channel layers deposited at different oxygen partial pressure (P_{O2} = 0% and P_{O2} = 33%) were

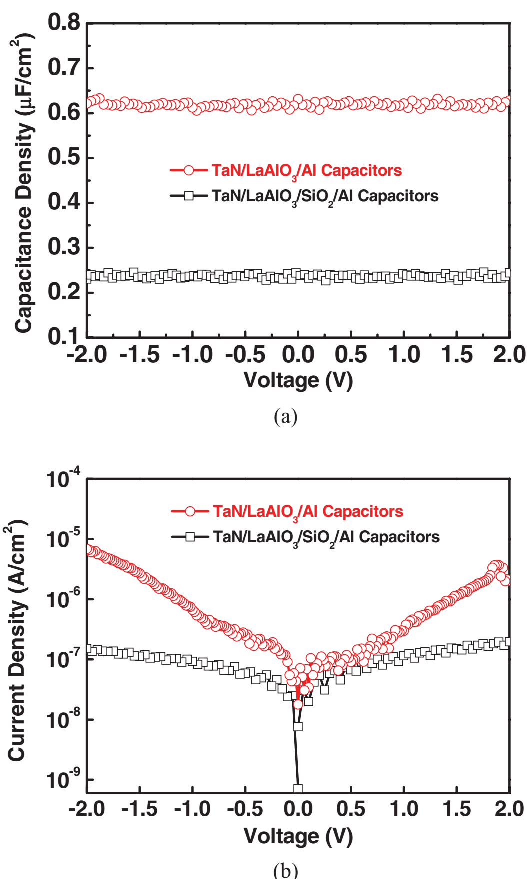
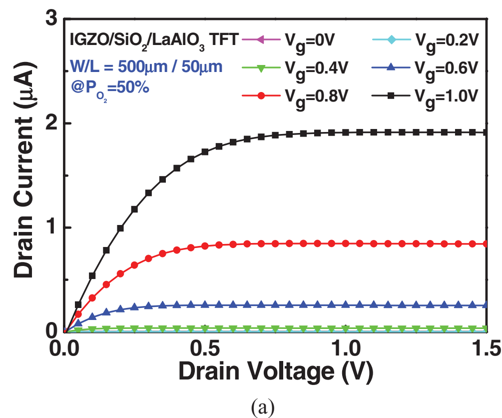


Figure 2. (a) *C-V* and (b) *J-V* characteristics of the TaN/$LaAlO_3$/Al and TaN/$LaAlO_3$/SiO_2/Al gate capacitors fabricated on the same substrate.



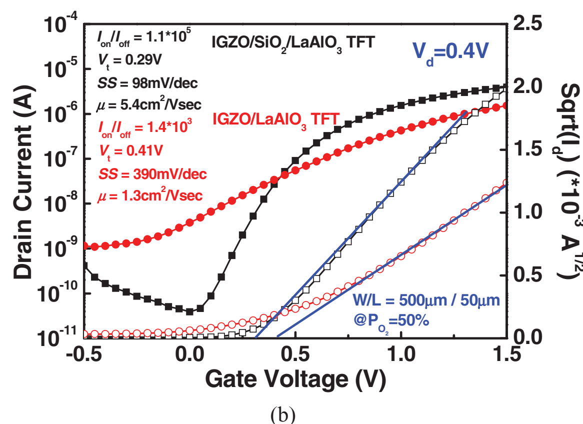


Figure 3. (a) Output I_d-V_d characteristics and (b) transfer I_d-V_g characteristics of the IGZO/$LaAlO_3$ and IGZO/SiO_2/$LaAlO_3$ TFTs when P_{O2} = 50%.

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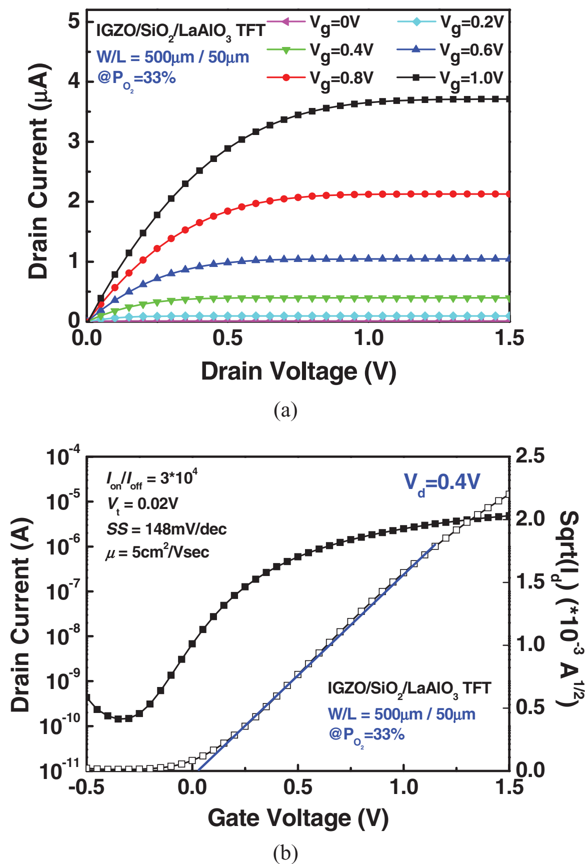

Figure 4. (a) Output I_d-V_d characteristics and (b) transfer I_d-V_g characteristics of the IGZO/SiO_2/$LaAlO_3$ TFT when $P_{O2} = 33\%$.

compared to the characteristics of TFT device when $P_{O2} = 50\%$. It is well-known that the carrier concentration and the mobility of sputtered IGZO film can be controlling by the mixing ratio of sputtering gases during deposition process.[25] Defects created by the ion bombardments and incorporation of sputtering ions act as scattering centers or charge traps for the carriers, and thus degrade the electrical device performances.[17] For the $P_{O2} = 0\%$ TFT device, it behaved with failed transistor characteristics with large leakage current (not shown). For the $P_{O2} = 33\%$ TFT device, the output I_d-V_d and transfer I_d-V_g characteristics are shown in Figure 4a and 4b, respectively. As compared to the TFT device when $P_{O2} = 50\%$, the $P_{O2} = 33\%$ TFT device exhibits degraded performances, including a much lower I_{on}/I_{off} of 3×10^4 and a smaller μ_{FE} of 5 $cm^2/V \cdot sec$, and a much larger *SS* of 148 mV/dec with a V_t of 0.02 V. It can be attributed to the oxygen partial pressure when depositing the IGZO film as the active channel layer. Since the IGZO film has electrons as majority carriers, which is mainly affected by the oxygen vacancies during deposition process.[31] When the IGZO film is deposited at low $P_{O2} = 0\%$, the oxygen is not supplied sufficiently, causing the increase of oxygen vacancies, which may act as shallow donors.[34] In this case, the active IGZO film would have a relatively high carrier density and behave with conducting property. This may be one of the reasons why the TFT using IGZO film when $P_{O2} = 0\%$ exhibited failed transistor characteristics with large leakage current. However, with the increase of P_{O2} when depositing the IGZO film, the amount of the oxygen vacancies decrease, leading to the decrease of carrier density, and thus the IGZO electrical property may change from conducting to insulating via semiconducting. It agrees with the improved TFT device characteristics when increasing the P_{O2} from 0% to 50% during the active IGZO channel layer deposition process.

Conclusions

In conclusion, incorporating a high-κ $LaAlO_3$ as gate dielectric, the IGZO TFTs show a small *SS* of 98 mV/dec, a low V_t of 0.29 V, a good I_{on}/I_{off} of 1.1×10^5, and an acceptable μ_{FE} of 5.4 $cm^2/V \cdot sec$ at operation voltage as low as 1.5 V. These good performances were related to the high gate capacitance density and small EOT by introducing the high-κ $LaAlO_3$ dielectric. Furthermore, with relatively high oxygen partial pressure during IGZO deposition process, the TFT device characteristics could be improved due to the low oxygen vacancy formation. The present results show that these low operation voltage IGZO TFTs with high-κ $LaAlO_3$ as gate dielectric have high potential for future high speed and low power applications.

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