Interleaved Current Sensorless Control for Multiphase Boost-Type Switch-Mode Rectifier With Phase-Shedding Operation

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Abstract—**Multiphase boost-type switch-mode rectifiers (SMRs) are often used to improve the efficiency of ac–dc conversion. In particular, the light-load efficiency can be increased by turning off some phases (i.e., phase-shedding operation). To keep the number of feedback signals fixed regardless of the topology phase number N, the interleaved current sensorless control (ICSC) with consideration of the phase-shedding operation is proposed in this paper. In ICSC, no current sensing is needed, and only input and output voltages are sensed. To demonstrate the proposed ICSC, a two-phase boost-type SMR is established for test, and the proposed ICSC is implemented in a field-programmable-gate-array-based system. The provided simulation and experimental results show good performance of the proposed ICSC.**

Index Terms—**Interleaved control, phase-shedding operation.**

I. INTRODUCTION

THE QUALIFIED ac/dc conversion must meet the functions of input current shaping and output voltage regulation. The boost-type switch-mode rectifier (SMR), including a diode rectifier and a boost converter, is often used to perform the qualified ac/dc conversion [1]–[3]. In addition, the multiloop control with the inner current loop and the outer voltage loop is often used to generate a switching signal in boost-type SMR. However, multiloop control needs to sense three signals: current signal and input and output voltage signals.

Recently, to reduce the number of feedback signals, many voltage sensorless controls (VSCs) [4]–[7] and current sensorless controls (CSCs) [8]–[10] for boost-type SMR have been proposed in the literature. The summary of feedback signals for sensorless controls is tabulated in Table I. It is clear that fewer feedback signals were used in sensorless control except the one in [9] due to the additional dc load current sensing.

Compared to the conventional boost-type SMRs, the multiphase SMRs with an interleaved control scheme possess smaller current ripples and higher efficiency.

To meet efficiency requirements, more and more multiphase boost-type SMRs were used in fuel-cell power-generation systems [11], plug-in electric vehicles [12], and photovoltaic applications [13]. Therefore, more and more research has focused on multiphase boost-type SMRs.

The design of multiphase boost-type SMRs can be found in [13]–[15]. The interleaved phase shifter in variable-frequency pulsewidth modulation and the reduction technique of common-mode electromagnetic interference in the multiphase boost-type SMRs had been proposed in [16] and in [17], respectively. The results in [18]–[21] show that the light-load system efficiency can also be significantly improved by shutting down some boost cells (i.e., phase-shedding operation).

The conventional multiloop control for boost-type SMR can be modified and extended to control an N-phase boost-type SMR by sensing all N inductor currents. Thus, the total number of the sensed signals is $(N + 2)$. With the increasing of the topology phase number N, the complexity of the control configuration would also increase. Therefore, sensorless control applied to the N-phase boost-type SMR is important to simplify the controller design. However, no sensorless control was used for N-phase boost-type SMR in the publication.

After studying the sensorless controls for boost-type SMR in [4]–[10], it is found that all sensorless controls can be extended for the N-phase boost-type SMRs. From the number of feedback signals listed in Table I, it is noted that, for the case of extending VSC, the number of total sensed signals is $N + 1$, and this number also increases with the topology phase number N. However, for the case of extending CSC, the required number of sensing signals is fixed to two, regardless of the phase number N. It means that the case of extending CSC to N-phase boost-type SMR is better than the case of extending VSC.

By observing the three CSC methods in Table I, the voltage follower control in [8] is simple, but it suffers from the large current harmonics. The method in [9] senses an additional load current signal instead of the input current signal. Therefore, the aforementioned two methods are not suitable to be extended for the control of N-phase boost-type SMR.

The CSC in [10] is used to develop the proposed interleaved CSC (ICSC) which is the first sensorless control for N-phase boost-type SMRs. In particular, the proposed ICSC also considers phase-shedding operation and improves the voltage transient response during phase-shedding operation.

TABLE I
SUMMARY OF FEEDBACK SIGNALS FOR VARIOUS CONTROLS [4]–[10]

|	Multi-loop Control	Voltage Sensorless Control (VSC)				Current Sensorless Control (CSC)		
		[4]	[5]	[6]	[7]	[8]	[9]	[10]
Feedback Input Voltage Signal	√	√					√	√
Feedback Output Voltage Signal	√		√	√		√	√	√
Feedback Current Signal	√	√	√	√	√			
Number of feedback signals for boost-type SMR	3	2	2	2	1	1	3*	2
Number of total feedback signals for N-phase boost-type SMR	$N+2$	$N+1$	$N+1$	$N+1$	N	1	3	2

* additional dc load current sensing
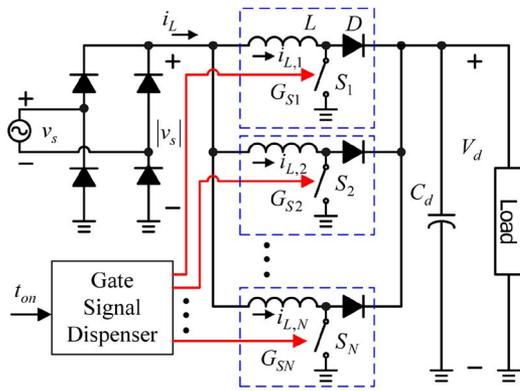
Fig. 1. Topology of an N-phase boost-type SMR.

This paper is organized as follows. Initially, the gate signal dispenser (GSD) is studied, and the average model of the N-phase boost-type SMR with phase-shedding operation is developed. Based on the developed model, ICSC is proposed. The analysis shows that the sinusoidal current waveform can be automatically generated by the proposed ICSC and the input current amplitude is independent of the active-phase number n. Finally, some simulated and experimental results are provided to show the performances of the proposed ICSC.

II. N-PHASE BOOST-TYPE SMR

Fig. 1 shows the topology of an N-phase boost-type SMR, where integer N is the topology phase number ($N > 1$). It consists of a diode bridge rectifier, N boost converters with the identical inductors L, and the identical diodes D. It is noted that, in the digital control of the power electronic system, the turn-on time t_{on} is given before the beginning of each switching period T_s. Thus, by the GSD, all the gate signals $G_{S1}, G_{S2}, \ldots, G_{SN}$ corresponding to the controllable switches $S_1, S_2, \ldots, S_N$ are generated from the same turn-on time signal t_{on}.

To model the behavior of the N-phase boost-type SMR, some assumptions are initially made: 1) All switches are assumed to operate at a fixed period T_s much smaller than the line period T, and thus, the input voltage v_s over one switching

period can be seen as a constant, and 2) a bulk capacitor C_d is connected to the output dc voltage, and thus, the output voltage is assumed to be equal to its average value V_d. Therefore, the steady-state output voltage is assumed to be equal to the voltage command $V_d = V_d^*$.

According to KCL, the total inductor current i_L is the sum of individual inductor currents

$$i_L = \sum_{k=1}^{N} i_{L,k}. \tag{1}$$

When the input voltage $v_s(t) = V_{sp} \sin(2\pi t/T) = V_{sp} \sin(\omega t)$ is positive, the total inductor current i_L is equal to the input current i_s, and the current i_L is equal to the negative input current $-i_s$ when the input voltage v_s turns to negative. Then, the input current can be represented in terms of the total inductor current i_L

$$i_s(t) = \text{sign}(v_s(t)) i_L(t) = \text{sign}(\sin \omega t) i_L(t) \tag{2}$$

where $\text{sign}(\bullet)$ is the sign operator and

$$\text{sign}(X) = \begin{cases} +1, & \text{when } X \geq 0 \\ -1, & \text{when } X < 0. \end{cases} \tag{3}$$

To let all gate signals have the same turn-on time signal t_{on} and the duty ratio d, a GSD is proposed. It follows that all the duty ratios $d_1, d_2, \ldots, d_N$ of gate signals are equal to each other

$$d_1 = d_2 = \cdots = d_N = \frac{t_{on}}{T_s} = d \tag{4}$$

where d_k is the duty ratio of boost converter #k.

A. GSD

At first, every switching period T_s can be divided into N identical subperiods $T_s' = T_s/N$. When the given turn-on time t_{on} is within the range $(M-1)T_s' < t_{on} \leq MT_s'$ ($1 \leq$ integer $M \leq N$), the given turn-on time t_{on} can be seen as the sum of two terms t_{on}' and $(M-1)T_s'$

$$t_{on} = t_{on}' + (M-1)T_s' \tag{5}$$

where t'_{on} can be seen as a partial turn-on time in the subperiod T'_s. Every gate signal with the same turn-on time t_{on} can be seen as the combinations of the following:

1) $(M-1)$ "turning-on" subperiods between $sp\#1$ and $sp\#(M-1)$;
2) one "partial-on" subperiod $sp\#M$ with partial turn-on time t'_{on};
3) $(N-M)$ "turning-off" subperiods between $sp\#(M+1)$ and $sp\#N$ subperiods.

The dispensing rules of the aforementioned subperiod series for the gate signal G_{S1} of boost converter #1 are obtained by the series

$$G_{S1}(t) = \{sp\#1, sp\#2, \ldots, sp\#(N-1), sp\#N\}. \quad (6)$$

Then, the gate signal G_{S2} of converter #2 is obtained from the shift-left operation of the gate signal G_{S1} by one subperiod, and it can be expressed as

$$G_{S2}(t) = \{sp\#2, \ldots, sp\#(N-1), sp\#N, sp\#1, \}. \quad (7)$$

Moreover, the gate signal G_{Sk} ($1 \leq$ integer $k \leq N$) of the boost converter $\#k$ is obtained from the shift-left operation of the gate signal G_{S1} by $(k-1)$ subperiod

$$G_{Sk}(t) = \{sp\#k, sp\#(k+1), \ldots, sp\#N,$$
$$sp\#1, \ldots, sp\#(k-1)\}. \quad (8)$$

According to the aforementioned GSD rules, the illustrated gate signals and the resulting inductor currents for $T'_s < t_{\text{on}} \leq 2T'_s$ ($M = 2$) and $(N-2)T'_s < t_{\text{on}} \leq (N-1)T'_s$ ($M = N-1$) are illustrated in Fig. 2(a) and (b), respectively.

For the case of $M = 2$ in Fig. 2(a), all the gate signals can be seen as a combination of one "turning-on" subperiod, one "partial-on" subperiod, and $(N-2)$ "turning-off" subperiods. The signal G_{S2} can be obtained by the shift-left operation of G_{S1} by one subperiod.

For the case of $M = N-1$ in Fig. 2(b), all the gate signals can be seen as a combination of $(N-2)$ "turning-on" subperiods, one "partial-on" subperiod, and one "turning-off" subperiod. The signal G_{SN} can be obtained by the shift-left operation of G_{S1} by N subperiods.

The inductor currents and the total current are also plotted in Fig. 2 for comparison. It is clear that the total current ripple $I_{\text{rip},N}$ is much smaller than the individual inductor current ripple.

B. Maximum Current Ripple

According to Fig. 2(a), there are always one "turning-on" switch, one "partial-on" switch with partial-on time $t'_{\text{on}} = t_{\text{on}} - T'_s$, and $(N-2)$ "turning-off" switches at each subperiod T'_s when $T'_s < t_{\text{on}} \leq 2T'_s$.

Similarly, when $(N-2)T'_s < t_{\text{on}} \leq (N-1)T'_s$, there are always $(N-2)$ "turning-on" switches, one "partial-on" switch with partial turn-on time $t'_{\text{on}} = t_{\text{on}} - (N-2)T'_s$, and one "turning-off" switch at each subperiod, as shown in Fig. 2(b).
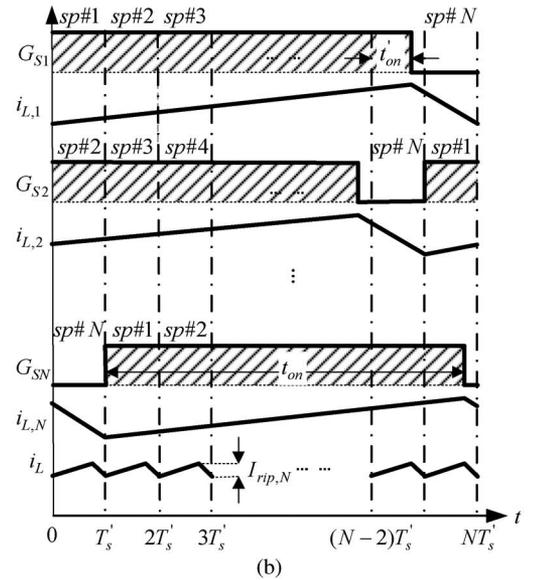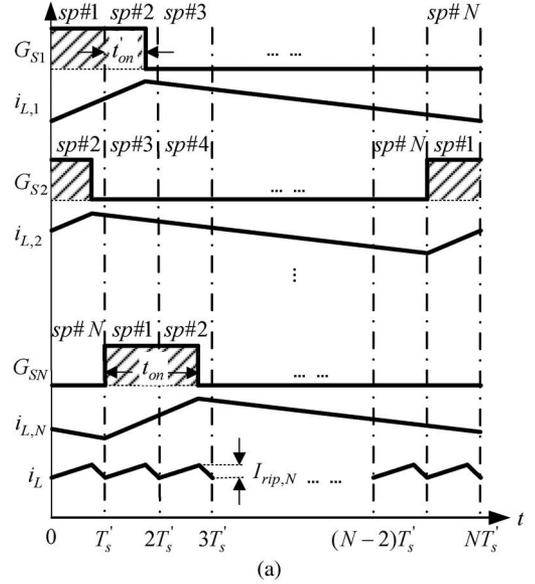

Fig. 2. Illustrated gate signals and the resulting inductor currents for (a) $T'_s < t_{\text{on}} \leq 2T'_s$ ($M = 2$) and (b) $(N-2)\,T'_s < t_{\text{on}} \leq (N-1)T'_s$ ($M = N-1$).

Consequently, once the given turn-on time t_{on} is within the range $(M-1)T'_s < t_{\text{on}} \leq MT'_s$ (integer $M \leq N$), there are always $(M-2)$ "turning-on" switches, one "partial-on" switch, and $(N-M)$ "turning-off" switches at each subperiod.

In each boost converter, the inductor current rising rate is $|v_s|/L$ when the switch is turning on. The inductor current falling rate is $(V_d^* - |v_s|)/L$ when the switch is turning off. Therefore, the rising rate m_L^+ and the falling rate m_L^- of the total inductor current i_L can be expressed as

$$m_L^+ = M\frac{|v_s|}{L} - (N-M)\frac{V_d^* - |v_s|}{L}$$
$$= N\frac{|v_s|}{L} - (N-M)\frac{V_d^*}{L} \quad (9)$$

$$m_L^- = -(M-1)\frac{|v_s|}{L} + (N-M+1)\frac{V_d^* - |v_s|}{L}$$
$$= -N\frac{|v_s|}{L} + (N-M+1)\frac{V_d^*}{L}. \quad (10)$$
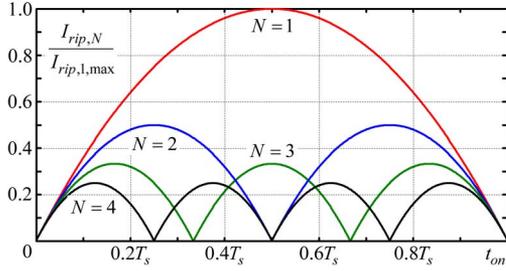
Fig. 3. Inductor current ripple with various turn-on times t_{on}.

Fig. 4. Equivalent average model with the phase-shedding operation.

Then, both multiplying the rising rate m_L^+ by current rising time t_{on}' and multiplying the falling rate m_L^- by current falling time $(T_s' - t_{\text{on}}')$ can yield the total current ripple $I_{\text{rip},N}$

$$I_{\text{rip},N} = m^+ t_{\text{on}}' = m^- \left(T_s' - t_{\text{on}}'\right). \tag{11}$$

By substituting (9) and (10) into (11), the absolute value of the input rectified voltage $|v_s|$ would be equal to

$$|v_s| = \frac{(N - M + 1)V_d^*}{N} - \frac{V_d^* t_{\text{on}}'}{N T_s'}. \tag{12}$$

From (9) and (12), the total current ripple $I_{\text{rip},N}$ becomes

$$I_{\text{rip},N} = \frac{V_d^* T_s}{NL} \left(\frac{t_{\text{on}}'}{T_s'} - \left(\frac{t_{\text{on}}'}{T_s'} \right)^2 \right). \tag{13}$$

The value of t_{on}' that produces the maximum current ripple $I_{\text{rip},N,\text{max}}$ occurs when $dI_{\text{rip},N}/dt_{\text{on}}' = 0$ which yields

$$1 - 2\left(\frac{t_{\text{on}}'}{T_s'} \right) = 0. \tag{14}$$

Solving (14) for t_{on}' gives $t_{\text{on}}' = 0.5T_s'$ for the maximum current ripple $I_{\text{rip},N,\text{max}}$. The maximum current ripple becomes

$$I_{\text{rip},N,\text{max}} = \frac{V_d^* T_s}{4NL}. \tag{15}$$

The maximum current ripple $I_{\text{rip},N,\text{max}}$ in (15) decreases with the increase of the topology phase number N. For comparison, the maximum current ripple of the conventional boost-type SMR with an inductor L is $I_{\text{rip},1,\text{max}} = V_d^* T_s/(4L)$.

The inductor current ripples for one-, two-, three-, and four-phase boost-type SMRs with various turn-on time signals t_{on} are plotted in Fig. 3. It is clear that the current ripples for phase number $N > 1$ are smaller than those of the conventional one-phase boost-type SMR ($N = 1$).

C. Average Current Model With Phase-Shedding Operation

To consider the practical condition, the nonzero inductor resistors r_L are assumed. In addition, the effects of the voltage drops across the diode bridge rectifier, the freewheeling diode, and the semiconductor switch are also considered.

The total voltage drop in the "switch-on" path is the sum of the voltage drops across the bridge rectifier and the semiconductor switch. The total voltage drop in the "switch-off" path is the sum of the voltage drops across the bridge rectifier and the freewheeling diode. Both voltage drops in the "switch-on" path
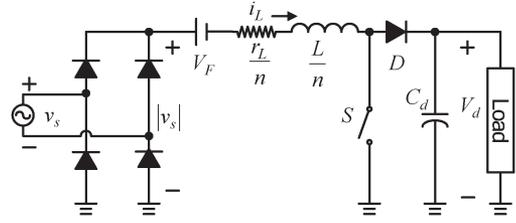
and the "switch-off" path are assumed to be equal to V_F in this section.

The KVL equation for boost converter #k ($1 \le$ integer $k \le N$) in terms of the average inductor current $\bar{i}_{L,k}$ within the switching period T_s and the duty ratio d is

$$L\frac{d\bar{i}_{L,k}}{dt} = |v_s| - r_L\bar{i}_{L,k} - V_F - V_d^*(1 - d_k). \tag{16}$$

Due to the identical duty ratios d in (8), all boost cells have the same average voltage equation. In the phase-shedding operation, only n boost converters ($1 \le$ integer $n \le N$) are active, and the number n can be changed according to the load condition to obtain higher efficiency.

By considering the phase-shedding operation, there are n KVL equations like (16) for the n active boost converters. Consequently, by summing n KVL equations and arranging the terms, the total average current $\bar{i}_L$ can be obtained

$$\frac{L}{n}\frac{d\bar{i}_L}{dt} = V_{sp}|\sin \omega t| - \frac{r_L}{n}\bar{i}_L - V_F - V_d^*(1 - d). \tag{17}$$

Therefore, from (17), the behavior of the average total inductor current with the active-phase number n in an N-phase boost-type SMR can be equivalently modeled by a boost-type SMR, as shown in Fig. 4. The model includes a reduced inductance (L/n), a reduced inductor resistance (r_L/n), and the same conduction voltage V_F. If the inductors are not identified, the inductor current would not be balanced, and (17) can be modified by replacing (L/n) and (r_L/n) with the equivalent inductor L_{eq} and the equivalent resistance r_{eq}, respectively.

From (17), the behavior of the average total inductor current is obtained in terms of the circuit parameters and the integer n. Because the active-phase number n is not fixed and may change due to the phase-shedding operation, the following proposed ICSC also needs to compensate the effect of the change of the integer number n.

III. ICSC

The proposed ICSC can be seen as a proportional–integral (PI)-type voltage controller illustrated in Fig. 5(a), cascaded with a turning-on time generator shown in Fig. 5(b). It is obvious that only the input voltage v_s and the output voltage V_d are sensed.

After generating the voltage error signal ε_v, the original phase shift signal θ is equal to the sum of the proportional term $K_p\varepsilon_v$ and the integral term $(K_I\varepsilon_v/s)$ by the well-known PI-type calculation. The original phase shift signal θ is limited to $\theta_{\text{max}}(n)$ for the overload protection of the overall system.
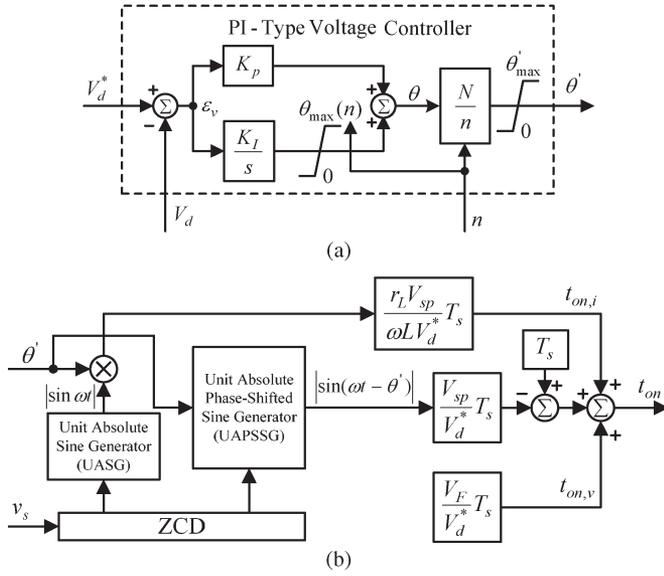
Fig. 5. Proposed ICSC: (a) PI-type voltage controller and (b) turn-on time generator.

To provide the overload protection to each active boost cell, the final phase shift signal θ' is limited to the maximum value $\theta'_{\max}$ based on the capability of the individual boost cell. Thus, the $\theta'_{\max}$ can be expressed as

$$\theta'_{\max} = \frac{n}{N}\theta_{\max}(n), \qquad 1 \leq \text{integer } n \leq N. \quad (18)$$

To meet the efficiency requirement, the phase-shedding operation is required, and the phase number n of active boost cells may change actively according to the load level. The change of the phase number n would contribute to the change of the equivalent model in Fig. 4. Thus, the consideration of the phase-shedding operation is very important for the control design.

A. With Consideration of Phase-Shedding Operation

In the proposed ICSC, an adjustable gain (N/n) is cascaded to the output of the voltage controller for the phase-shedding operation. From Fig. 5(a), the resulting phase shift signal θ' becomes

$$\theta' = \frac{N}{n}\theta, \qquad 1 \leq \text{integer } n \leq N. \quad (19)$$

A unit-absolute sine signal $|\sin \omega t|$, in phase with the rectified input voltage $|v_s|$, is generated by the zero-crossing detector (ZCD) and the unit-absolute sine generator. After obtaining the original phase shift signal θ', a unit-absolute phase-shifted sine signal $|\sin(\omega t - \theta')|$ with the phase θ' leading the rectified input voltage $|v_s|$ is also generated by the corporation of ZCD and the unit-absolute phase-shifted sine generator.

To compensate the effect of the equivalent inductor resistance (r_L/n) and the conduction voltage V_F, two compensated signals $t_{\text{on},i}$ and $t_{\text{on},v}$ in Fig. 5(b) are given by

$$t_{\text{on},i} = \theta' \frac{V_{sp}}{V_d^*} \frac{r_L}{\omega L}|\sin \omega t| T_s \quad (20)$$

$$t_{\text{on},v} = \frac{V_F}{V_d^*}T_s. \quad (21)$$

The resulting turn-on time signal t_{on} can be expressed as

$$t_{\text{on}} = T_s - T_s \frac{V_{sp}}{V_d^*}|\sin(\omega t - \theta')| + t_{\text{on},i} + t_{\text{on},v}. \quad (22)$$

Consequently, the duty ratio $d = t_{\text{on}}/T_s$ can be simplified to

$$d = 1 - \frac{V_{sp}}{V_d^*}|\sin(\omega t - \theta')| + \theta'\frac{V_{sp}}{V_d^*}\frac{r_L}{\omega L}|\sin(\omega t)| + \frac{V_F}{V_d^*}. \quad (23)$$

B. Independent Sinusoidal Current Amplitude

By substituting (18) and (23) into (17) and arranging the terms, the first-order differential equation for the average inductor current $\bar{i}_L$ can be obtained

$$\frac{L}{n}\frac{d\bar{i}_L}{dt} = V_{sp}\left(|\sin \omega t| - \left|\sin\left(\omega t - \frac{N\theta}{n}\right)\right|\right)$$

$$+ \left[\theta\frac{N\hat{V}_s}{\omega L}|\sin(\omega t)| - \bar{i}_L\right]\frac{r_L}{n}. \quad (24)$$

It is noted that the terms regarding V_F in (24) are canceled out.

When the term $N\theta/n$ is small and near zero, the approximations $\sin(N\theta/n) \approx (N\theta/n)$ and $\cos(N\theta/n) \approx 1$ can be used. Then, by using the common trigonometric identity $\sin(\alpha - N\theta/n) = \sin(\alpha)\cos(N\theta/n) - \sin(N\theta/n)\cos(\alpha)$, $\sin(\alpha - N\theta/n)$ can be approximated to $(\sin \alpha - N\theta \cos \alpha/n)$. Thus, the first term $|\sin \omega t| - |\sin(\omega t - N\theta/n)|$ in the right-hand side of (24) may be approximated to

$$|\sin \omega t| - \left|\sin\left(\omega t - \frac{N\theta}{n}\right)\right| \approx \frac{N\theta}{n}\text{sign}(\sin \omega t)\cos \omega t \quad (25)$$

where the sign operator $\text{sign}(X)$ had been defined in (3).

By using the approximation in (25), the first-order differential equation in (24) can be rewritten as

$$\frac{d\bar{i}_L}{dt} \approx \frac{NV_{sp}\theta}{L}\text{sign}(\sin \omega t)\cos \omega t$$

$$+ \frac{r_L}{L}\left[\frac{NV_{sp}\theta}{\omega L}|\sin \omega t| - \bar{i}_L\right]. \quad (26)$$

It is noted that the active-phase number n is canceled out in (26). Since $d|\sin \omega t|/dt = \text{sign}(\sin \omega t)\cos \omega t$, substituting (27) into the second term of the right-hand side of (26) would make the second term zero. Thus, the following inductor current (27) must be the solution to (26) even when the inductor resistance r_L is not neglected

$$\bar{i}_L \approx \frac{NV_{sp}\theta}{\omega L}|\sin \omega t| = \frac{NV_{sp}\theta}{\omega L}\text{sign}(\sin \omega t)\sin \omega t. \quad (27)$$

From (2), the average input current $\bar{i}_s$ becomes

$$\bar{i}_s(t) \approx \theta\frac{NV_{sp}}{\omega L}\sin \omega t = I_{sp}\sin \omega t \quad (28)$$
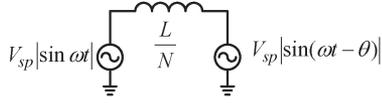
Fig. 6. Basic circuit of the power flow in the power system.

where I_{sp} is the peak value of the input sinusoidal current and it is independent of the active-phase number n. It means that the change of the active-phase number n (i.e., phase-shedding operation) has no effect on the sinusoidal input current amplitude I_{sp}.

Due to the input voltage $v_s = V_{sp} \sin(\omega t)$ and the in-phase sinusoidal current i_s in (28), the average input power $\overline{P}_s$ can be expressed as

$$\overline{P}_s = \frac{V_{sp} I_{sp}}{2} = \frac{N V_{sp}^2}{2\omega L} \theta = \frac{V_{sp}^2}{2\omega(L/N)}\theta. \qquad (29)$$

It is clear that the change of active-phase number n (i.e., phase-shedding operation) has no effect on the average input power $\overline{P}_s$, and thus, the phase-shedding operation has no effect on the output dc voltage. That is, the proposed ICSC is suitable for the phase-shedding operation.

Additionally, the average input power $\overline{P}_s$ in (29) is proportional to the controllable signal θ which also shows that the PI-type calculation is able to generate the adequate phase signal θ.

The proposed ICSC is based on [10], and the results in [10] are helpful to the sensitivity study of ICSC. The sensitivity study shows that, with parameter uncertainty, the PI-type controller is able to regulate the dc output voltage, but the current harmonics may be yielded.

C. Design of Controller Parameters

The transfer function between the output voltage perturbation ΔV_d and the phase perturbation $\Delta\theta$ can be obtained from the power balance between input power P_s, output power P_d, and capacitor power P_C [10].

From (29), the average input power P_s with the small perturbation ΔP_s becomes

$$\overline{P}_s + \Delta\overline{P}_s = \frac{V_{sp} I_{sp}}{2} = \frac{N V_{sp}^2}{2\omega L}(\theta + \Delta\theta). \qquad (30)$$

The output power P_d with the small perturbation ΔP_d can be represented by the output voltage perturbation ΔV_d

$$P_d + \Delta P_d = \frac{(V_d^* + \Delta V_d)^2}{R_L} \approx \frac{(V_d^*)^2}{R_L} + \frac{2V_d^* \Delta V_d}{R_L}. \qquad (31)$$

The small perturbation ΔP_C of the capacitor power can be represented by the output voltage perturbation ΔV_d

$$\Delta P_C = \frac{d\left(\frac{C}{2}(V_d^* + \Delta V_d)^2\right)}{dt} \approx C V_d^* \frac{d\Delta V_d}{dt}. \qquad (32)$$

TABLE II
SIMULATED CIRCUIT PARAMETERS

|	
Input line voltage(peak)	$\hat{V}_s = 155V\,(110V_{rms})$
Voltage command	$V_d^* = 300V$
Rated output power	$700W$
Input line frequency	$f = 50Hz$
Capacitance	$C_d = 1880uF$
Inductor	$L = 4mH$
Inductor resistance	$r_L = 0.25\Omega$
Conduction voltage	$V_F = 3.68V$
Carrier frequency	$f_s = 1/T_s = 10kHz$
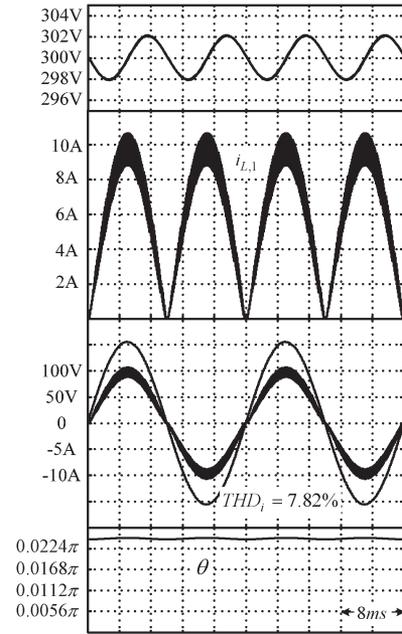
(a)
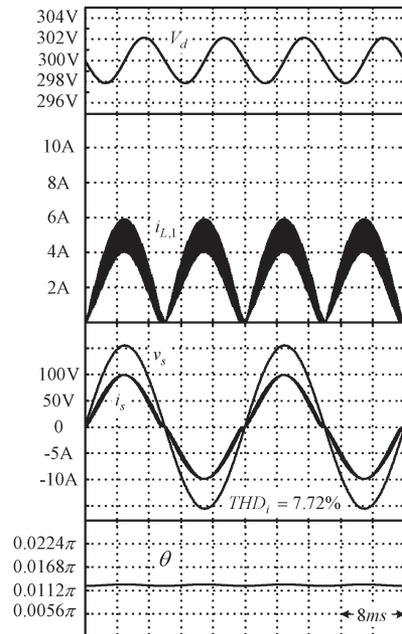
(b)

Fig. 7. Simulated waveforms for (a) the boost-type SMR ($N = 1$) and (b) two-phase boost-type SMR ($N = 2$).
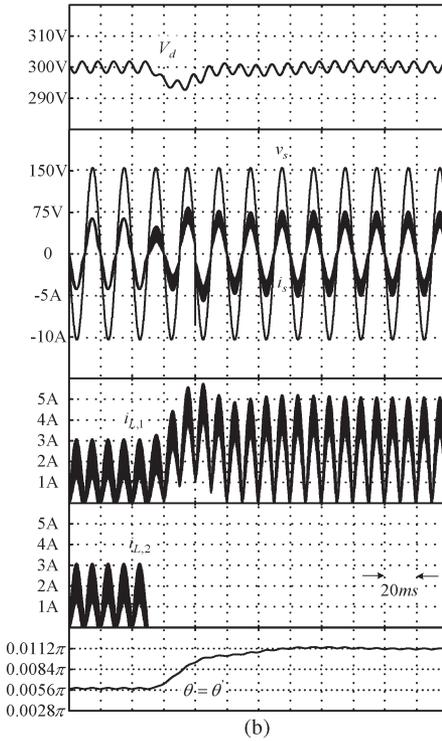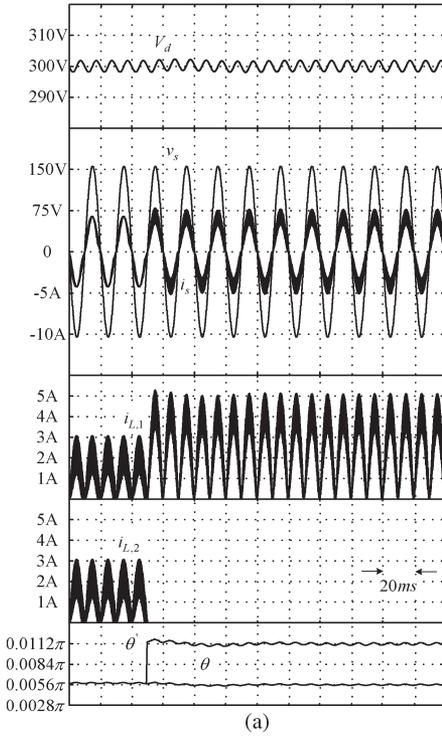
Fig. 8. Simulated responses during the change of active-phase number n from 2 to 1: (a) with the adjustable gain (N/n) and (b) without the adjustable gain (N/n).

The balance $\Delta P_s = \Delta P_C + \Delta P_d$ between the power perturbations can yield the following small-signal transfer function $G_s(s)$ for the sinusoidal input current:

$$G_s(s) = \frac{\Delta V_d}{\Delta \theta} = \frac{N V_{sp}^2}{2 C V_d^* \omega L} \frac{1}{\left(s + \frac{2}{CR_L}\right)} = k_s \frac{1}{\left(s + \frac{2}{CR_L}\right)}. \tag{33}$$
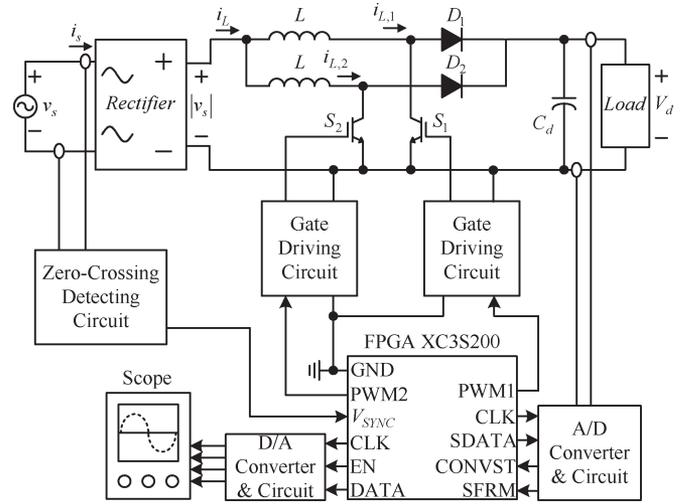

Fig. 9. Implementation of proposed ICSC and a two-phase boost-type SMR.
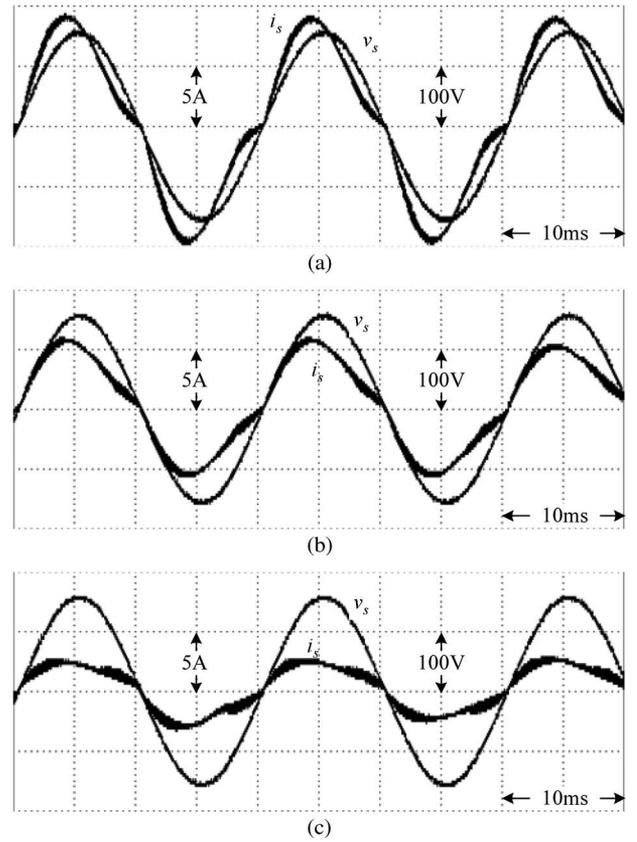
Fig. 10. Experimental input voltage and current waveforms. (a) 600 W. (b) 400 W. (c) 200 W.

It is clear that the behavior of output voltage can be seen as a first-order model. Additionally, the change of the active-phase number n has no effect on the transfer function $G_s(s)$. Thus, the output voltage can be well regulated by including the simple PI-type controller in the proposed ICSC.

By setting the ratio of the proportional gain k_P and the integral gain k_I to the pole of $G_s(s)$

$$\frac{k_I}{k_P} = \frac{2}{CR_L} \tag{34}$$

TABLE III
INPUT CURRENT HARMONICS AND THEIR LIMITATIONS OF IEC 61000-3-2

	Class A (A_{rms})	600W		400W		200W	
		Class D (A_{rms})	Fig.10(a) (A_{rms})	Class D (A_{rms})	Fig.10(b) (A_{rms})	Class D (A_{rms})	Fig.10(c) (A_{rms})
3rd	2.300	2.040	1.360	1.360	0.486	0.680	0.358
5th	1.140	1.140	0.760	0.760	0.168	0.380	0.036
7th	0.770	0.600	0.400	0.400	0.074	0.200	0.034
9th	0.400	0.300	0.200	0.200	0.009	0.100	0.022
11th	0.330	0.210	0.140	0.140	0.029	0.070	0.010
13th	0.210	0.178	0.118	0.118	0.028	0.059	0.017
15th	0.150	0.154	0.103	0.103	0.016	0.051	0.009
17th	0.132	0.136	0.091	0.091	0.008	0.045	0.010
19th	0.118	0.122	0.081	0.081	0.009	0.041	0.008
21th	0.107	0.110	0.073	0.073	0.012	0.037	0.005
PF			0.975		0.958		0.950
THD_i (%)			10.77		14.22		19.51
DPF			0.986		0.968		0.980

the closed-loop transfer function of the output voltage V_d and the output voltage command V_d^* can be obtained

$$\frac{V_d}{V_d^*} = \frac{k_P \frac{NV_{sp}^2}{2CV_d^*\omega L}}{s + k_P \frac{NV_{sp}^2}{2CV_d^*\omega L}}. \tag{35}$$

Equation (35) is a low-pass filter. To avoid the effect of the double-line-frequency voltage ripple in the output voltage, the cutoff frequency in (35) is chosen to be smaller than the 1/20 of the double line frequency (i.e., 0.1ω). Therefore, the proportional gain k_P can be obtained by

$$k_P \leq \frac{4CV_d^*\omega^2 L}{5NV_{sp}^2}. \tag{36}$$

D. Viewpoint of Power Flow

From (25), the approximation $|\sin\omega t| - |\sin(\omega t - N\theta/n)|$ can also be written as

$$|\sin\omega t| - \left|\sin\left(\omega t - \frac{N\theta}{n}\right)\right| \approx \frac{N}{n}\left(|\sin\omega t| - |\sin(\omega t - \theta)|\right). \tag{37}$$

By substituting the average inductor current $\bar{i}_L$ in (27) into (24) to cancel the last term in (24), the average inductor voltage $\bar{v}_{L/n}$ across the inductor L/n in Fig. 4 can be expressed as

$$\bar{v}_{\frac{L}{n}} = \frac{L}{n}\frac{d\bar{i}_L}{dt} \approx V_{sp}\frac{N}{n}\left(|\sin\omega t| - |\sin(\omega t - \theta)|\right). \tag{38}$$

Therefore, the average inductor voltage $\bar{v}_{L/N}$ can be expressed in terms of $\bar{v}_{L/n}$

$$\bar{v}_{\frac{L}{N}} = \frac{n}{N}\bar{v}_{\frac{L}{n}} \approx V_{sp}\left(|\sin\omega t| - |\sin(\omega t - \theta)|\right). \tag{39}$$

Equation (39) can be equivalently plotted in Fig. 6, where a fixed inductance L/N is connected between two rectified sinusoidal voltages under phase-shedding operation. These two

voltages have identified magnitudes, but little phase difference θ exists between them. It shows that phase-shedding operation has no effect on the power flow (i.e., voltage regulation).

IV. SIMULATION RESULTS

In this section, a series of the computer simulations is provided to demonstrate the proposed ICSC. The nominal values and the circuit elements are listed in Table II. The simple PI-type loop with the antiwindup mechanism is used as the voltage controller to automatically adjust the controllable phase shift signal θ. According to (34) and (36), the controller parameters were chosen as $k_P = 0.0053$ rad/V and $k_I = 0.0379$ rad/V/s.

A. Steady-State Performance

The simulated waveforms for the conventional boost-type SMR ($n = N = 1$), as shown in Fig. 1, and the two-phase boost-type SMR ($n = N = 2$) were plotted in Fig. 7(a) and (b), respectively. In Fig. 1, a 150-Ω resistor is connected across the output voltage, and the average power is near 600 W. It is noted that, in this simulation, all their boost cells were active, and thus, $n = N$ and $\theta = \theta'$ in the proposed ICSC.

From Fig. 7(b), the output voltage V_d is well regulated to the voltage command $V_d^* = 300$ V, and all their input currents i_s were shaped to a sinusoidal waveform, in phase with the input voltage v_s. With the increase of phase number N, both the input current ripple and total current harmonic distortion (THD$_i$) decrease, although their individual inductor current ripples were equal to each other. Therefore, the proposed ICSC is able to yield the desired power factor correction function without sensing any current.

B. Phase-Shedding Operation

When one phase (i.e., one boost converter) of a two-phase boost-type SMR ($N = 2$) turns down, the active-phase number

n changes from $n = 2$ to $n = 1$. It follows that the proposed ICSC automatically changes the gain (N/n) from $2/2$ $(= 1)$ to $2/1$ $(= 2)$ and thus yields the final phase shift signal $\theta' = 2\theta$. The simulated output voltage V_d, input current i_s, two inductor currents $i_{L,1}$ and $i_{L,2}$, and two phase signals θ and θ' of the proposed ICSC were plotted in Fig. 8(a).

At the instant of the change of active-phase number n, the final phase signal θ suddenly rises to a double level, which contributes to a small voltage fluctuation in Fig. 8(a).

C. Without Adjustable Gain (N/n)

For comparison, the simulated responses without the proposed adjustable gain (N/n) in Fig. 5(a) are also plotted in Fig. 8(b). It is clear that the PI-type voltage controller must take some time to regulate the output voltage during the phase-shedding operation. However, the voltage dip in Fig. 8(b) is larger than that in Fig. 8(a). It follows that the proposed ICSC is able to perform well during the phase-shedding operation.

V. EXPERIMENTAL RESULTS

The field-programmable gate array (FPGA)-based implementation of the proposed ICSC and the two-phase boost-type SMR $(N = 2)$ has been plotted in Fig. 9, where the circuit parameters have been tabulated in Table II. Since the GSD in Fig. 1 cannot be implemented in the general microcontroller chips, the proposed controller is implemented in an FPGA-based environment.

Because there is no A/D and no D/A function in a commercial FPGA XC3S200 chip, an external A/D converter is used to sense the output voltage, and some D/A converters are used to show the control variables of the implemented ICSC in the scope. In addition, a zero-crossing detecting circuit is used to detect the zero crossing of the input voltage.

A. Steady-State Performance

The input voltage and input current waveforms with various load powers of 600, 400, and 200 W were plotted in Fig. 10(a)–(c), respectively. Due to the practical current-dependent conduction voltage drop, the experimental input current waveforms were not purely sinusoidal waveforms, as shown in the simulated waveforms in Fig. 7. However, from the measured input current harmonics and the listed class D harmonic limitations of IEC61000-3-2 in Table III, the harmonic performance of the proposed ICSC was able to meet the standards.

As plotted in Fig. 5, the circuit parameters r_L and L are used in the proposed ICSC, and therefore, the practical difference between the real circuit parameters and the nominal parameters may have an effect on the performance of ICSC. In the simulation environment, the control parameters were exactly equal to the circuit parameters, and thus, the simulated current waveforms were purely sinusoidal waveforms.

Therefore, current distortion due to parameter mismatch can be easily found in the experimental waveforms. However, the
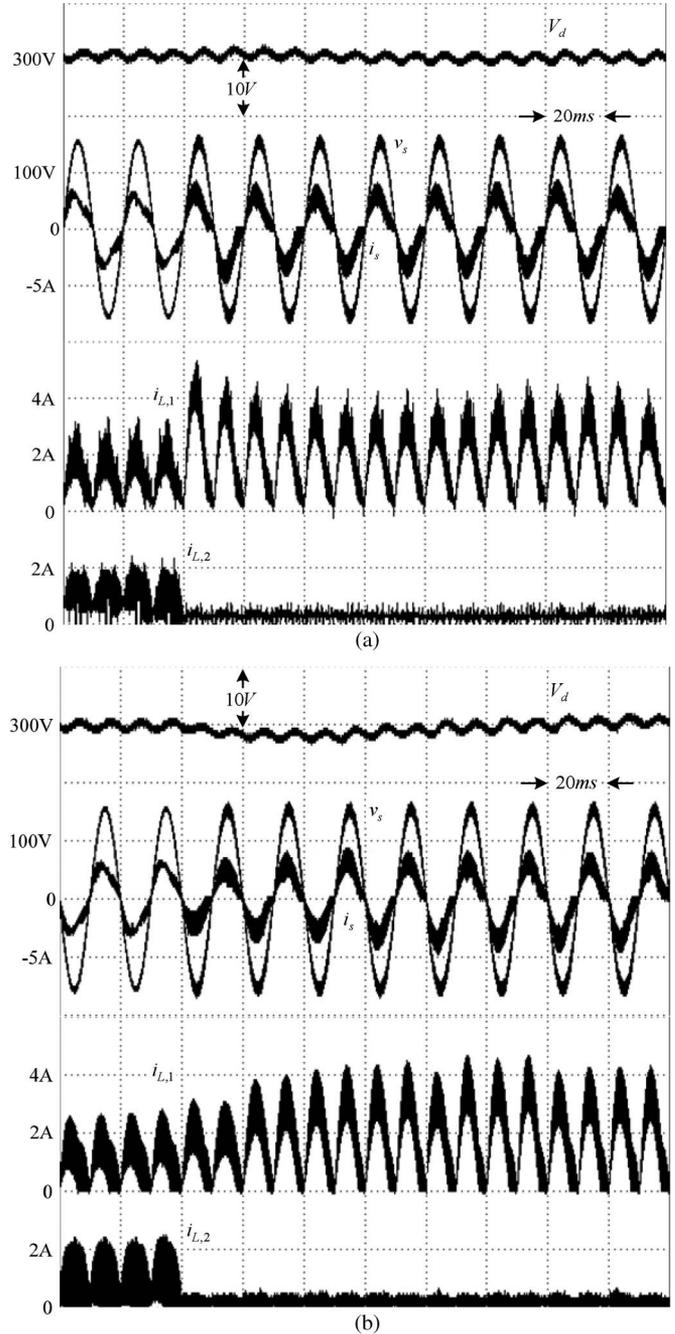

Fig. 11. Experimental responses during the change of active-phase number n from 2 to 1: (a) with the adjustable gain (N/n) and (b) without the adjustable gain (N/n).

harmonic currents were acceptable to the standard limits in Table III.

B. Phase-Shedding Operation

At light load, more than one boost cell should be shut down to reduce the total switching loss and to increase the light-load efficiency. To work well under the phase-shedding operation, an adjustable gain (N/n) was included in the proposed ICSC.

Some experimental waveforms with and without an adjustable gain (N/n) were plotted in Fig. 11(a) and (b), respectively. Like the simulation results, the proposed adjustable gain

(N/n) was able to reduce the voltage dip due to the phase-shedding operation.

VI. CONCLUSION

The ICSC has been proposed and implemented in this paper. A two-phase boost-type SMR had also been established in FPGA-based environment for evaluation. From the provided simulation and experimental results, the proposed ICSC is able to meet the harmonic standards and has near-zero voltage dip during the phase-shedding operation.

The proposed ICSC is the first method applied to the multiphase boost-type SMR. In addition, the proposed ICSC only needs to sense two voltage signals without sensing any current signal. Thus, ICSC may become a competitive solution for the digital control of an N-phase boost-type SMR with phase-shedding operation.

ACKNOWLEDGMENT

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