A 81-dB Dynamic Range 16-MHz Bandwidth $\Delta\Sigma$ Modulator Using Background Calibration

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***Abstract*—A fourth-order discrete-time delta-sigma modulator (DSM) was fabricated using a 65-nm CMOS technology. It combines low-complexity circuits and digital calibrations to achieve high speed and high performance. The DSM is a cascade of two second-order loops. It has a sampling rate of 1.1 GHz and an input bandwidth of 16.67 MHz with an oversampling ratio of 33. It uses high-speed opamps with a dc gain of only 10. Two different types of digital calibrations are used. We first employ the integrator leakage calibration to correct the poles of the integrators. We then apply the noise leakage calibration to minimize the leaking quantization noise from the first loop. The noise leakage calibration also relaxes the component-matching requirements. Both calibrations can operate in the background without interrupting the normal DSM operation. The chip's measured signal-to-noise-and-distortion ratio and dynamic range are 74.32 and 81 dB, respectively. The chip consumes 94 mW from a 1 –V supply. The active area is $0.33\ \times\ 0.58\ \mathrm{mm}^2$.**

***Index Terms*—Analog–digital conversion, analog-to-digital converter (ADC), calibration, delta-sigma modulation, oversampling, switched-capacitor circuits.**

I. Introduction

THE delta-sigma modulator (DSM) is an analog-to-digital conversion technique that uses oversampling and noise shaping to enhance the conversion resolution. Compared with Nyquist-rate ADCs that offer similar input signal bandwidth, the DSMs operate at a much higher circuit speed. The performance of a wide-band discrete-time (DT) DSM is usually limited by its internal opamps that realize the integrator function. For an input bandwidth of 20 MHz and an over-sampling ratio (OSR) of 32, the corresponding sampling rate is $f_s = 1.28$ GHz, and the required opamp unity-gain frequency is about $5f_s = 6.4$ GHz. It is difficult for an opamp with such a speed to have a decent dc gain. Circuit-level gain enhancement techniques, such as multiple-stage configuration [1], correlated double sampling [2], and correlated level shifting [3], all sacrifice the speed.

In a DT DSM, an integrator realized with a low-gain opamp loses some of its ability to suppress in-band quantization noises. The integrator transfer function is also more sensitive to process-voltage-temperature (PVT) variations. The dc gain requirement for the opamps can be relaxed by increasing the order of the DSM loop, or by employing the multi-stage noise-shaping (MASH) structure [4]–[7]. A higher-order DSM may require more quantization levels from its internal analog-to-digital converter (ADC) and digital-to-analog (DAC) to stabilize the loop [8], yielding complex circuits. On the other hand, the MASH modulators may require calibration to correct the effects of component mismatches and integrator variations [9], [10]. There is an alternative MASH structure that can mitigate the matching requirements [11].

This paper describes a DT DSM that combines low-complexity circuits and digital calibration to achieve wide bandwidth and large dynamic range. It is a MASH modulator consisting of two cascaded second-order loops. The number of the quantization levels of its internal ADCs and DACs is only 4. The internal integrators are realized with high-speed opamps with a dc gain of only 10. Two different types of digital calibrations are applied. We first employ the integrator leakage calibration to correct the poles of the integrators. We then use the noise leakage calibration to minimize the quantization noise from the first loop leaking to the DSM combined output. The noise leakage calibration also relaxes the component matching requirements for the MASH structure. Since each calibration adjusts only one parameter, it is robust. All calibration can proceed in the background without interrupting the normal DSM operation. The calibration processors are simple digital circuits. They do not include any complex filter. The modulator was fabricated using a 65 nm CMOS technology. It has a sampling rate of 1.1 GHz and an input bandwidth of 16.67 MHz with an oversampling ratio (OSR) of 33. The measured signal-to-noise-and-distortion ratio (SNDR) and dynamic range (DR) are 74.32 and 81 dB, respectively. The chip consumes 94 mW from a 1-V supply. The active area is $0.33\ \times\ 0.58\ \mathrm{mm}^2$.

The remainder of this paper is organized as follows. Section II describes the DSM architecture and its design parameters. Section III describes the integrator leakage calibration and its design consideration. Section IV describes the noise leakage calibration. Section V describes the design of the crucial circuits. Section VI shows the experimental results. Section VII draws conclusions. In addition, Appendices A and B analyze the transient behavior and the fluctuation of the integrator leakage calibration, respectively.

II. DSM Architecture

Fig. 1 shows the reported fourth-order DT DSM architecture. In its core is a MASH modulator consisting of two stages of second-order modulation loops. There are four integrators, H_1 to H_4. Each integrator is modeled with a gain factor α and a pole β. Table I shows the design values for α and β. For an ideal integrator with an opamp dc gain $A_0 = \infty$, $\beta = 1$.

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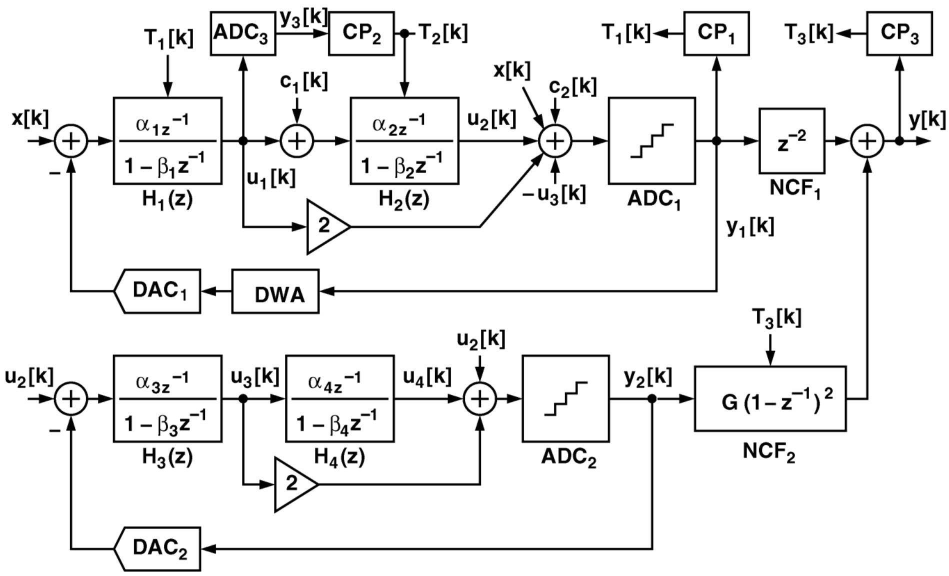

Fig. 1. Fourth-order MASH DSM with digital calibrations.

TABLE I
INTEGRATOR VARIATIONS DUE TO OPAMP DC GAIN A_0

A_0	α_1	α_2	α_3	α_4	β_1	β_2	β_3	β_4
∞	0.410	0.455	1	1	1	1	1	1
10	0.359	0.396	0.833	0.833	0.964	0.957	0.917	0.917

There are two ADCs (digitizers), ADC_1 and ADC_2. Each one is a 2-bit flash ADC comprising three comparators. There are two corresponding DACs, DAC_1 and DAC_2. DAC_1 covers an output range of $\pm V_R$, while DAC_2 covers an output range of $\pm(1/2)V_R$. The adders preceding the two ADCs are passive switched-capacitor circuits. In the first loop, a data-weighted averaging (DWA) dynamic element matching logic [12] is added before DAC_1 to mitigate its conversion errors. A full-scale sine-wave input is defined as $V_R \sin \omega_i t$, which has a signal power of $P_S = (1/2)V_R^2$. In our design, $V_R = 1$ V. The use of multibit ADCs leads to smaller quantization errors and stability improvement. The combination of filter feedforward and multibit ADCs relaxes the linearity and voltage swing requirements for the analog circuitry [13].

As shown in Fig. 1, the raw digital outputs from the two modulation loops are y_1 and y_2, respectively. Due to the use of feedforward, both loops have a signal transfer function (STF) of 1, i.e., $\mathrm{STF}_1 = Y_1/X = 1$ and $\mathrm{STF}_2 = Y_2/U_2 = 1$. The two digitizers ADC_1 and ADC_2 introduce quantization noises, denoted as e_1 and e_2, respectively. The two noise transfer functions are defined as $\mathrm{NTF}_1 = Y_1/E_1$ and $\mathrm{NTF}_2 = Y_2/E_2$. NTF_1 is a function of H_1 and H_2, while NTF_2 is a function of H_3 and H_4. Applying the α and β parameters listed in Table I with an opamp dc gain $A_0 = \infty$, the resulting noise transfer functions are $\mathrm{NTF}_1 = (1-z^{-1})^2/(1-1.18z^{-1}+0.37z^{-2})$ and $\mathrm{NTF}_2 = (1-z^{-1})^2$. Two digital noise-cancellation filters NCF_1 and NCF_2 combine the two outputs y_1 and y_2 to generate the final DSM output y, which can be expressed as

$$Y = X \times \mathrm{NCF}_1 + E_1 \times \mathrm{NLF} + E_2 \times \mathrm{NTF}_2 \cdot \mathrm{NCF}_2 \quad (1)$$

where the noise leakage transfer function NLF is defined as

$$\mathrm{NLF} = \frac{Y}{E_1} = \mathrm{NTF}_1 \times (\mathrm{NCF}_1 - H_1 \cdot H_2 \cdot \mathrm{NCF}_2). \quad (2)$$

If we choose the digital filters $\mathrm{NCF}_1 = z^{-2}$ and $\mathrm{NCF}_2 = G(1-z^{-1})^2$ with $G = 1/(\alpha_1\alpha_2) \approx 5.36$, then, in the DSM combined output y, e_1 is completely eliminated, and e_2 is shaped by a fourth-order function $(1-z^{-1})^4$.

In the wide-bandwidth applications, the DSM uses high-speed opamps to implement the integrators. In our design, the opamps in the integrator configuration have a unity frequency of 6 GHz, but have a dc gain A_0 of only 10. Table I shows the effect of A_0 on the integrators. Their gain factors α change and their poles β become less than 1. When placing these integrators in the DSM, the corresponding NTF exhibits a degraded capability of suppressing quantization noise in the signal band. Besides the A_0 effect on α and β, the capacitor mismatch in an integrator also causes a change in α. Both the α and the β variations yield $\mathrm{NLF} \neq 0$. This phenomenon is called noise leakage, when a portion of e_1 leaks out to the DSM output y.

Fig. 2 shows the effect of β on the noises e_1 and e_2 appearing in the output y. It plots the ratio of noise power to the signal power of a full-scale sine-wave input, $P_S = 0.5V_R^2$. The noise power includes only the frequency components within the signal band. An OSR of 33 is assumed. P_{e1} is the noise power of e_1 in y and P_{e2} is the noise power of e_2 in y. It is assumed that all integrators have the same β. In our design, P_{e2} is a weak function of β. It can be neglected if the expected signal-to-noise ratio (SNR) of the entire DSM is 80 dB. On the other hand, P_{e1} is a strong function of β. It requires $|1-\beta| < 1.4 \times 10^{-3}$, so that P_{e1} is 85 dB below P_S.

From (1) and (2), and since $\mathrm{NCF}_1 = z^{-2}$ is a simple delay, the digital filter NCF_2 must match the analog integrators H_1 and H_2 to reduce P_{e1}. The filter NCF_2 can become adaptive to accommodate the variations in H_1 and H_2 [14]. However, if the β parameters in H_1 and H_2 are away from 1, the calibration

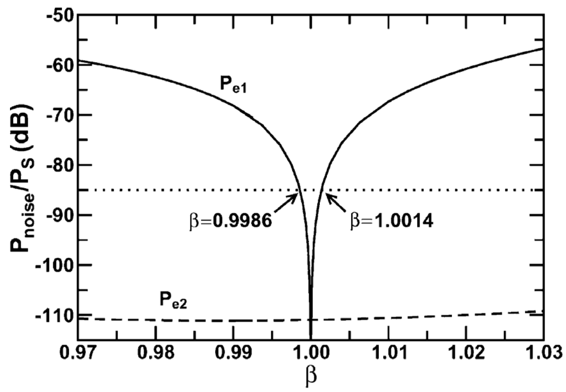

Fig. 2. Effect of integrator pole β on the noises e_1 and e_2 in the DSM output.

for NCF_2 are complex. In our design, we first calibrate integrators H_1 and H_2 to simplify the requirement for NCF_2. We then calibrate NCF_2 to minimize the NLF of (2). We apply the integrator leakage calibration described in Section III to integrators H_1 and H_2 to recover their capability of noise suppression and make their β approximate 1. We simplify the second noise-cancellation filter as $\mathrm{NCF}_2 = G(1 - z^{-1})^2$, which has only one adaptive parameter G. We then apply the noise leakage calibration described in Section IV to find G. All calibrations are operated in the background without interrupting the normal DSM function.

The ADC_1 quantization noise e_1 may contain harmonic tones or idle tones. These tones may show up in the signal band of the DSM output y. Furthermore, these tones may correlate with the calibration signals introduced by the aforementioned calibrations, corrupting the calibration process. Therefore, as shown in Fig. 1, a dithering signal $-u_3$ is added to the input of ADC_1 to randomize e_1. This dithering signal is taken from the output of the integrator H_3, which is the quantization noise e_2 with first-order noise shaping. The dithering signal is not included in the following analyses since its effect is minuscule.

III. Integrator Leakage Calibration

The reported DSM includes four switched-capacitor (SC) integrators. Each SC integrator contains an opamp. Neglecting its settling behavior, the integrator transfer function is $H(z) = \alpha z^{-1}/(1 - \beta z^{-1})$. If the dc gain of the opamp is finite, then $\beta < 1$, and the integrator becomes lossy. If the input of this integrator is 0, then its output can then be expressed as $V_o[k+1] = \beta V_o[k]$. Its output loses an amount of $(1-\beta)V_o$ for every clock cycle. The issue is known as integrator leakage.

Fig. 3 shows the integrator with leakage compensation. It is driven by two nonoverlapping clocks ϕ_1 and ϕ_2. The switches labeled with 1 are turned on when $\phi_1 = 1$. The switches labeled with 2 are turned on when $\phi_2 = 1$. The circuit is a conventional noninverting integrator with an additional C_f positive feedback for leakage compensation [15]. The capacitor C_f puts back $C_f V_o$ amount of charge into C_i for every clock cycle. The β of the integrator becomes

$$\beta = \frac{1 + \frac{C_f}{C_i} + \frac{1}{A_0}\left(1 + \frac{C_p}{C_i}\right)}{1 + \frac{1}{A_0}\left(1 + \frac{C_s + C_f + C_p}{C_i}\right)} \tag{3}$$

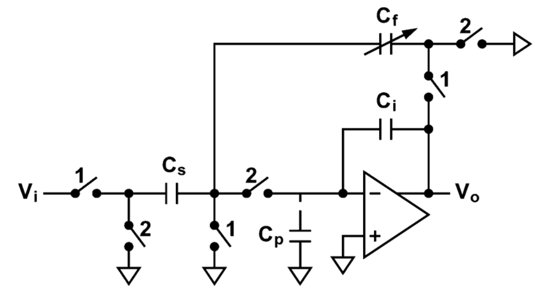

Fig. 3. Integrator with leakage compensation.

where A_0 is the opamp dc gain, and C_p is the parasitic capacitance at the opamp input. To obtain a lossless integrator, we want $C_f = C_s/(A_0 - 1)$ so that $\beta = 1$. Comparing with C_s, C_f is relatively small. The capacitor C_f itself and its associated switches add minuscule loading and noise to the integrator. Since the optimal value for C_f depends on voltage gain A_0, which is sensitive to PVT variations. The capacitor C_f is automatically adjusted by the calibration described below.

As shown in Fig. 1, the integrator leakage calibration is applied to the integrators H_1 and H_2 of the first modulation loop. Consider the calibration of the first integrator H_1. The C_f capacitor in H_1 is controlled by a digital signal T_1 such that

$$C_{f1} = C_{f1,0} + \Delta C_{f1} \times T_1 \tag{4}$$

where T_1 is an integer, ΔC_{f1} is the C_f digital control step size and $C_{f1,0}$ is the C_f capacitance when $T_1 = 0$. From (3), the corresponding β_1 of H_1 is approximated by

$$\beta_1 = \beta_{1,0} + \Delta\beta_1 \times T_1 \tag{5}$$

where $\Delta\beta_1 \approx \Delta C_{f1}/C_{i1}$. The control signal T_1 is generated from a calibration processor, CP_1. To calibrate H_1, a calibration signal c_1 is added to the input of the second integrator H_2. CP_1 receives the ADC_1 output y_1, and detects the β_1 of H_1 from the c_1-related signal embedded in y_1. It then adjusts T_1 to make β_1 approximate 1.

Fig. 4 shows the CP_1 block diagram and its input components. At the CP_1 input, the digital stream y_1 is a summation of (1) the input x, (2) the ADC_1 quantization noise e_1 shaped by the noise transfer function NTF_1, and (3) the calibration signal c_1 shaped by the calibration-signal transfer function CTF_1, which is defined as $\mathrm{CTF}_1 = Y_1/C_1$. The calibration signal c_1 is a square wave with f_{c1} frequency, V_{c1} amplitude, and 50% duty cycle. The square wave c_1 excites CTF_1, yielding d_1. Thus, embedded in y_1, d_1 is the step response of CTF_1 triggered by c_1. This step response settles toward a final value of

$$V_{cf1} \approx V_{c1} \times \frac{1 - \beta_1}{\alpha_1}. \tag{6}$$

V_{cf1} shows the same polarity as $1 - \beta_1$. Thus, CP_1 can determine if β_1 is above or below 1 by detecting the polarity of V_{cf1}.

As shown in Fig. 4, CP_1 extracts the V_{cf1} information from y_1 by correlating y_1 with a triple-valued sequence $g_1 \in \{-1, 0, +1\}$. This g_1 waveform has the same polarity as c_1, but its value is set to 0 during the initial transition phase of d_1. The resulting signal sequence r is accumulated on an

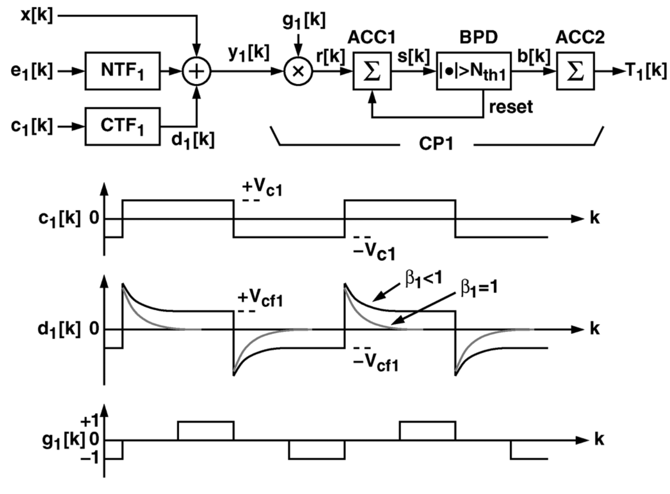

Fig. 4. Calibration of integrator H_1.

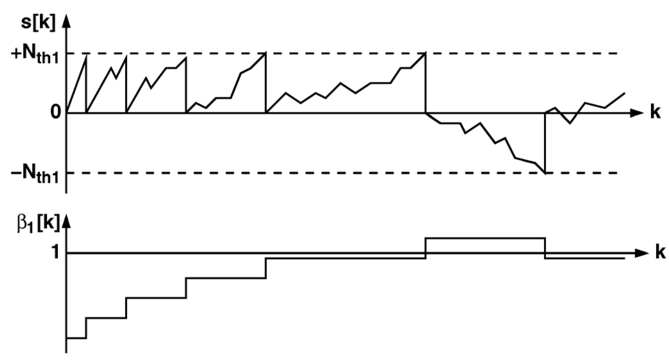

Fig. 5. AAR operation.

accumulator ACC1 followed by a binary peak detector (BPD). Together they perform the accumulation-and-reset (AAR) operation [16]–[18] to guess the polarity of V_{cf1} while removing the perturbations caused by x and e_1. The AAR operates as follows. The accumulator ACC1 accumulates the r sequence. Its output s is monitored by the BPD with a threshold $N_{\rm th1} > 0$. Whenever s reaches either $+N_{\rm th1}$ or $-N_{\rm th1}$, the BPD issues an output $b = +1$ or $b = -1$ for one clock cycle respectively and reset accumulator output s to 0. The BPD output b remains at 0 when $-N_{\rm th1} < s < +N_{\rm th1}$. The BPD output b is an estimate of the polarities of V_{cf1} and $1 - \beta_1$. CP$_1$ uses it to increase or decrease the control signal T_1. Thus, following b is another accumulator, ACC2, that accumulates the b sequence. Its output T_1 controls the capacitor C_{f1} of the integrator H_1, thus adjusts its β_1. Fig. 5 illustrates the time-domain waveform of the ACC1 output s, and the waveform of the resulting β_1. When β_1 approaches 1, both $|1 - \beta_1|$ and V_{cf1} become smaller, and it takes a longer time to activate the BPD.

The above calibration scheme involves signal correlation and AAR operation. For this calibration to be effective, it requires that the calibration signal c_1 has no correlation with other signals in y_1, including the input x and the quantization noise e_1. Since c_1 is out of the signal band of x, there is no correlation between c_1 and x. Assume e_1 is a white noise. There are frequency components in e_1 that can have correlation with c_1. However, this correlation is weak since those frequency components have randomly varying phases. The effect of this correlation can be overcome by choosing a large BPD threshold $N_{\rm th1}$.

This calibration scheme has five design parameters, including the c_1 amplitude, V_{c1}, the c_1 frequency, f_{c1}, the g_1 duty ratio, D_g, the BPD threshold, $N_{\rm th1}$, and the T_1 control step size, ΔC_{f1}. Referring to Fig. 4, the duty ratio D_g is defined as the ratio of the time for $g_1 = +1$ to the time for $c_1 = +V_{c1}$. The duty ratio for $g_1 = -1$ and $c_1 = -V_{c1}$ is assumed to be the same as D_g.

As shown in Fig. 4, the calibration square wave c_1 triggers a step response d_1. Let c_1 have a frequency of f_{c1}, a corresponding period of $T_{c1} = 1/f_{c1}$, and a duty cycle of 50%. We want f_{c1} to be larger than the signal bandwidth so that it can be removed by the decimation filter following the DSM. We also want $T_{c1}/2$ to be longer than the time required for d_1 to settle so that its final value V_{cf1} can be extracted by correlating d_1 with g_1. In our design, $T_{c1} = 64T_s$ and $D_g = 1/2$, so that, in each d_1 transient, d_1 has a period of 16 clock cycles to settle before g_1 is activated for 16 clock cycles. The frequency of c_1 is $f_{c1} = f_s/64$. As long as $\mathrm{OSR} > 32$, the frequency components of d_1 is outside the signal band.

The injection of c_1 increases the signal ranges of the integrators' outputs, u_1 and u_2. A larger u_1 and larger u_2 raise the nonlinearity effect of the integrators. A large u_2 may even overload the second modulation loop, yielding large e_2. Thus, an increase in the c_1 amplitude, V_{c1}, degrades the SNDR of the DSM. On the other hand, from (6), if V_{c1} is too small, the corresponding V_{cf1} is too small to ensure a robust calibration. We choose V_{c1} by using simulations. In the simulations, all integrators are assumed to have a pole at $\beta = 1$. Without the injection of c_1, the peak SNDR of the entire DSM is 88.5 dB occurring at an input level of -0.25 dBFS. The peak SNDR is degraded by more than 6 dB if $V_{c1} > 0.2V_R$. For our design, we choose $V_{c1} = 0.08V_R$. The resulting peak SNDR is maintained at 88 dB. Without c_1, the signal standard deviation for u_1 and u_2 are $\sigma(u_1) = 0.085V_R$ and $\sigma(u_2) = 0.075V_R$, respectively. When c_1 with $V_{c1} = 0.08V_R$ is injected, $\sigma(u_1)$ and $\sigma(u_2)$ become $0.115V_R$ and $0.160V_R$, respectively.

Fig. 5 illustrates the transient response of β_1 during the calibration. As analyzed in Appendix A, this averaged transient behavior can be modeled as a first-order linear system. The transient response of β_1 can be expressed as

$$\beta_1[k] = 1 - (1 - \beta_1[0]) \times e^{-k/\tau_1} \tag{7}$$

where the time constant τ_1 is

$$\tau_1 = \frac{N_{\rm th1}}{D_{g1}} \cdot \frac{V_R}{V_{c1}} \cdot \frac{\alpha_1}{\Delta\beta_1}. \tag{8}$$

It is assumed the digitizer ADC_1 has an analog-to-digital conversion gain of $1/V_R$. From (8), a smaller $N_{\rm th1}$ and a larger $\Delta\beta_1$ lead to smaller τ_1, yielding a faster calibration speed.

Fig. 5 shows that, as the calibration process converges, the behavior of β_1 becomes a discrete random fluctuation around 1. Referring to Fig. 4, both the input x and the quantization noise e_1 induce this fluctuation. Their effects are diminished by the AAR operation. A larger $N_{\rm th1}$ and a smaller $\Delta\beta_1$ lead to a smaller fluctuation in β_1, yielding the better SNDR performance for the DSM. As $N_{\rm th1}$ increases, the standard deviation of β_1

fluctuation, $\sigma(\beta_1)$, converges to an averaged value that can be expressed as [17]

$$\sigma(\beta_1) = \frac{\Delta\beta_1}{\sqrt{6}}. \tag{9}$$

Appendix B contains a simplified derivation of the above equation. As shown in Fig. 2, the deviation of β from 1 increase the noise power P_{e1}. we want $3\sigma(\beta) < 1.4 \times 10^{-3}$ so that P_{e1} is 85 dB below P_S. In this design, we choose $\Delta\beta_1 = 1.126\times10^{-3}$ and $N_{th1} = 32$, yielding a time constant $\tau_1 = 2.481 \times 10^5$. If the clock rate $f_s = 1/T_s =$ 1 GHz, the physical time constant is $\tau \times T_s =$ 248.1 μs.

Referring to Fig. 1, to calibrate the second integrator H_2, a calibration square wave c_2 is added to the input of ADC_1. An additional digitizer ADC_3 is added to convert u_1, the output of the first integrator H_1, into a digital stream y_3. ADC3 is also a flash ADC, comprising three comparators with thresholds at $\{0, \pm(1/9)V_R\}$. The calibration processor CP_2 receives y_3 and generates T_2 to adjust the β_2 of H_2. The control signal T_2 adjusts β_2 by controlling the C_f capacitor in H_2. The control mechanism is similar to (4) and (5).

The ADC_3 output y_3 comprises: 1) the ADC_3 quantization noise e_3; 2) the ADC_1 quantization noise e_1 shaped by CTF_2; and 3) the calibration signal c_2 shaped by CTF_2, where $\mathrm{CTF}_2 = U_1/C_2$ is the transfer function from c_2 to u_1. The calibration signal c_2 is a square wave with f_{c2} frequency, V_{c2} amplitude, and 50% duty cycle. Similar to the c_1-to-d_1 response shown in Fig. 4, c_2 triggers the step response of CTF_2. This step response settles toward a final value of

$$V_{cf2} \approx V_{c2} \times -\frac{1-\beta_2}{\alpha_2}. \tag{10}$$

This V_{cf2} is extracted by CP_2 to detect the polarity $1-\beta_2$. The operation of CP_2 is identical to that of CP_1. It correlates y_3 with a triple-valued sequence $g_2 \in \{-1, 0, +1\}$, which has a duty ratio of D_{g2}. The AAR eliminates the perturbation caused by e_1 and e_3. The AAR has a BPD threshold of N_{th2}. Comparing to the V_{cf1} of (6), V_{cf2} has an opposite polarity. Thus, comparing with the g_1 of Fig. 4, the polarity of g_2 is inverted. For our design, c_2 has a period of $T_{c2} = 64T_s$ and an amplitude of $V_{c2} = 0.11V_R$. The duty ratio of g_2 is $D_{g2} = 1/2$. The BPD threshold for the AAR is $N_{\mathrm{th2}} = 32$. The β_2 control step size is $\Delta\beta_2 = 2.24 \times 10^{-3}$. The above design parameters result in a calibration time constant of $\tau_2 = 1.013 \times 10^5$ or $\tau_2 \times T_s =$ 101.3 μs with a 1-GHz clock. When the calibration signal c_2 is injected into the DSM, the signal standard deviations for u_1 and u_2 are $\sigma(u_1) = 0.095V_R$ and $\sigma(u_2) = 0.120V_R$, respectively.

The H_1 calibration and the H_2 calibration are executed sequentially. They do not interfere with each other. The operations are robust. The calibration signals c_1 and c_2 are easy to generate. The calibration processors CP_1 and CP_2 can be realized with simple digital circuits. They use the masking signals g_1 and g_2 to extract the calibration data. Complex filter is not needed.

IV. Noise Leakage Calibration

From (1) and (2), the ADC_1 quantization noise e_1 can leak into the DSM output y if the noise leakage transfer function $\mathrm{NLF} \neq 0$. After the integrator leakage calibration described in Section III, the β_1 of H_2 and the β_2 of H_2 are close to 1.

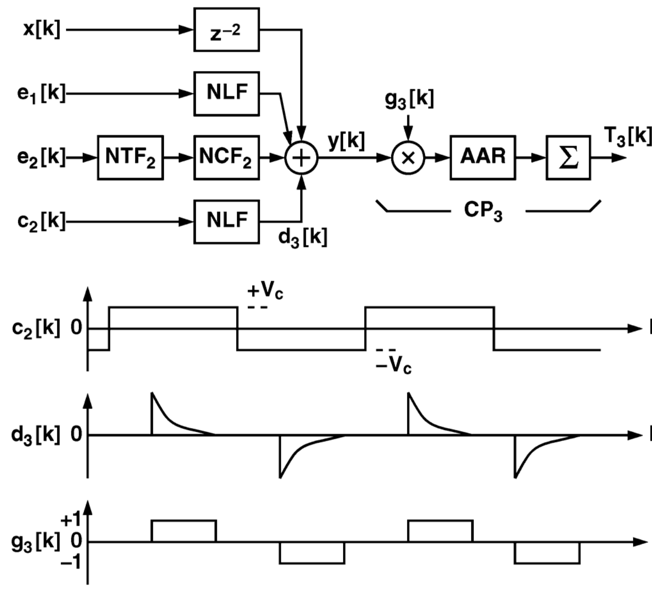

Fig. 6. Noise leakage calibration and calibration processor CP_3.

However, the gain factors α_1 and α_2 are still subjected to PVT variations. With $\beta_1 \approx 1$ and $\beta_2 \approx 1$, the second noise-cancellation filter can be simplified as $\mathrm{NCF}_2 = G(1-z^{-1})^2$, where G is a gain factor. Since $\mathrm{NCF}_1 = z^{-2}$, the noise leakage function for e_1 can be approximated by

$$\mathrm{NLF} \approx \mathrm{NTF}_1 \times z^{-2}(1 - \alpha_1\alpha_2 \cdot G). \tag{11}$$

We want $G \approx 1/(\alpha_1\alpha_2)$ to minimize NLF. As shown in Fig. 1, the gain factor G is adjusted by a digital control T_3, such that

$$G = G_0 + \Delta G \times T_3 \tag{12}$$

where T_3 is an integer, ΔG is the control step size, and G_0 is the value of G when $T_3 = 0$. The control T_3 is generated from the calibration processor CP_3.

During the integrator leakage calibration of H_2, a calibration square wave c_2 is added to the input of ADC_1. Similar to the ADC_1 quantization noise e_1, c_2 passes through NLF and appears in the DSM combined output y. Thus, CP_3 can observe y, extract the c_2-related signal in y, and then adjust G through T_3 to make c_2 disappear from y.

Fig. 6 shows the CP_3 block diagram and its input components. The DSM output y contains: 1) the input x delayed by the filter $\mathrm{NCF}_1 = z^{-2}$; 2) the quantization noise e_1 shaped by NLF; 3) the quantization noise e_2 shaped by $\mathrm{NTF}_2 \times \mathrm{NCF}_2$; 4) the calibration signal c_2 shaped by NLF. The calibration square wave c_2 excites the NLF filter, yielding d_3. Thus, embedded in y, d_3 is the step response of NLF triggered by c_2. As expressed in (11), the NLF filter is a NTF_1 filter with a time delay of two clock cycles and a gain factor of $1-\alpha_1\alpha_2 G$. The NTF_1 filter is a high-pass filter with two zeros close to dc. Thus, the time-domain step response of NLF is a spike and settles toward zero. CP_3 detects the energy of those spikes and then adjusts G to eliminate the spikes. The operation of CP_3 is similar to those of CP_1 and CP_2. It correlates y with a triple-valued sequence $g_3 \in \{-1, 0, +1\}$ with a duty cycle of D_{g3}. The sequence g_3 is aligned with the spikes in d_3. Its active region overlaps the major

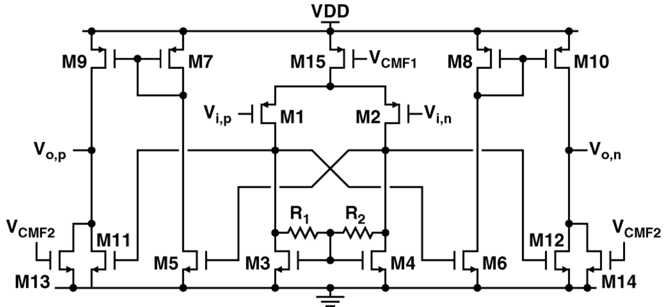

Fig. 7. Operational amplifier schematic.

area of the spikes. The AAR in CP3 eliminates the perturbation caused by e_1, e_2, and x. The AAR has a BPD threshold of $N_{\text{th}3}$. The output T_3 adjusts G as expressed in (12). For our design, the duty ratio of g_3 is $D_{g3} = 0.25$. The BPD threshold for the AAR is $N_{\text{th}3} = 96$. The G control step size is $\Delta G = 0.25$. The above design parameters result in a calibration time constant of $\tau_3 = 6.514 \times 10^5$ or $\tau_3 \times T_s =$ 651.4 μs with a 1-GHz clock. This time constant is larger than the time constants for the integrator leakage calibration, τ_1 and τ_2.

During the power-on phase, CP_3 is reset and $T_3 = 0$ and $G = G_0$. According to (11), when the calibration converges, $G \approx 1/(\alpha_1\alpha_2)$. To reduce the initial calibration convergence time, we choose a G_0 that is close to $1/(\alpha_1\alpha_2)$, which can be calculated as

$$G_0 = \frac{C_{i1}}{C_{s1}}\frac{C_{i2}}{C_{s2}}\left(1+\frac{C_{f1}}{C_{s1}+C_{f1}}+\frac{C_{f1}}{C_{i1}}\right)\left(1+\frac{C_{f2}}{C_{s2}+C_{f2}}+\frac{C_{f2}}{C_{i2}}\right) \quad (13)$$

where C_{i1}, C_{s1}, and C_{f1} are the capacitors in the integrator H_1, and C_{i2}, C_{s2}, and C_{f2} are the capacitors in the integrator H_2. Capacitors C_{f1} and C_{f2} are functions of control signals T_1 and T_2 respectively. The power-on sequence for calibration is described as follows. The DSM first executes the H_1 calibration for $4\tau_1 T_s \approx$ 1 ms, and then the H_2 calibration for $4\tau_2 T_s \approx$ 0.4 ms. Afterward, the DSM uses the values of T_1 and T_2 from the above calibrations to estimate C_{f1} and C_{f2}, and applies (13) to calculate G_0. The DSM then activates CP3 every time when the H_2 calibration is in progress.

V. Circuit Design

Here, we describe the circuit design to implement the DSM of Fig. 1. The DSM is to be fabricated using a 65-nm CMOS technology. The supply voltage is 1 V. The DSM is expected to achieve a sampling rate higher than 1 GS/s and a DR larger than 80 dB.

Fig. 7 shows the schematic of the opamps used in the integrators. It is a two-stage class-AB amplifier without frequency compensation [19]. All MOSFETs are sized with the minimum channel length of 60 nm. The amplifier has a dc voltage gain of 10. Its dominant poles are located at the output nodes $V_{o,p}$ and $V_{o,n}$. When configured as an integrator, the opamp achieves an unity-gain frequency of 6 GHz and a phase margin of 63 degrees. The voltages V_{CMF1} and V_{CMF2} are generated by two separate continuous-time common-mode feedback (CMFB) circuits. Each CMFB contains additional voltage amplification to increase the loop gain and improve the common-mode rejection against power-line fluctuation. The push-pull output stage also provides additional common-mode rejection.

The opamp is used to realize the fully differential version of the integrator shown in Fig. 3. The input common-mode voltage of the opamp is set to $V_{DD}/4$. The analog switches connected to the opamp's inputs are nMOSFETs with boosting gate control [19]. Consider the integrator H_1. Its ideal value of the gain factor α_1 is determined by the capacitor ratio C_{s1}/C_{i1}.

In our design, the thermal noise from the first integrator H_1 is the dominant source of thermal noise. Its total noise power showing up in the signal band of the DSM output y is about $(14/3)(kT/C_{s1})$ [8]. We choose $C_{s1} =$ 1.9 pF so that the power of this thermal noise in the signal band, P_θ, is 90 dB below the power of a full-scale sine-wave input, P_S. By using the periodic noise analysis of the circuit simulator, we estimate that the total P_θ of the entire DSM is 86 dB below P_S.

The control signal T_1 adjusts the capacitor C_{f1} in the integrator H_1 as described by (4), thus varying β_1 as described by (5). The capacitor step size ΔC_{f1} determines the step size $\Delta\beta_1$. From Section III, we want $\Delta\beta_1 = 1.126 \times 10^{-3}$. In our design, T_1 is a 6-bit control signal, and C_{f1} can be varied from 0 to 378 fF with a step size $\Delta C_{f1} =$ 6 fF. As a result, β_1 can be varied from 0.964 to 1.028 with a step size $\Delta\beta_1 \approx 1.13 \times 10^{-3}$. Similarly, the CP_2 output T_2 controls the capacitor C_{f2} in the integrator H_2. The signal T_2 is a 5-bit control signal, and C_{f2} can be varied from 0 to 186 fF with a step size $\Delta C_{f2} =$ 6 fF. As a result, β_2 can be varied from 0.957 to 1.027 with a step size $\Delta\beta_2 \approx 2.24 \times 10^{-3}$.

Fig. 8 shows the schematic of DAC_1 and the adder preceding ADC_1 in the first modulation loop of the DSM. Only one side of the fully-differential circuit is depicted. The adder is a passive switched-capacitor circuit [20], comprising three capacitors C_{a1} to C_{a3}. The capacitors have an identical capacitance of 60 fF. During $\phi_2 = 1$, the preamplifier in the comparator is reset with its input shorted to its output. Meanwhile, the inverse of u_1 from the integrator H_1, the output u_3 from the integrator H_3, and a comparator threshold voltage $V_{\text{th}1}$ are sampled onto capacitors C_{a1}, C_{a2}, and C_{a3}, respectively. The input offset of the preamplifier is also stored on the capacitors. During $\phi_1 = 1$, the output u_1 from H_1, the output u_2 from H_2, and the modulator input x are connected to the capacitors respectively, yielding a differential voltage $x + 2u1 + u2 - u3 - V_{\text{th}1}$ at the input of the preamplifier. Upon the falling edge of ϕ_1, the latch in the comparator compares $V_a = x + 2u1 + u2 - u3$ with the threshold $V_{\text{th}1}$, generating a single-bit digital output D_1. There are 3 comparators in ADC_1. They compare V_a with three different thresholds, which are $V_{\text{th}1} = -(2/3)V_R$, $V_{\text{th}2} = 0$, and $V_{\text{th}3} = +(2/3)V_R$.

All of the integrators in this DSM sample their input during $\phi_1 = 1$ and perform the integration during $\phi_2 = 1$. As shown in Fig. 8, the input sampling capacitor C_{s1} of the integrator H_1 is divided into three identical capacitors C_{s1a}, C_{s1b}, and C_{s1c} to implement the 2-bit equally weighted DAC_1. During $\phi_1 = 1$, the input x is sampled onto all three capacitors. During $\phi_2 = 1$, the capacitors are connected to either V_R or 0, depending on the three binary signals B_1, B_2, and B_3, respectively. For capacitor C_{s1a}, it is connected to V_R if $B_1 = 1$ and is connected to ground if $B_1 = 0$.

The analog input of the DSM, $x(t)$, is sampled onto the capacitor C_{s1} in the first integrator H_1 and the capacitor C_{a3} in the

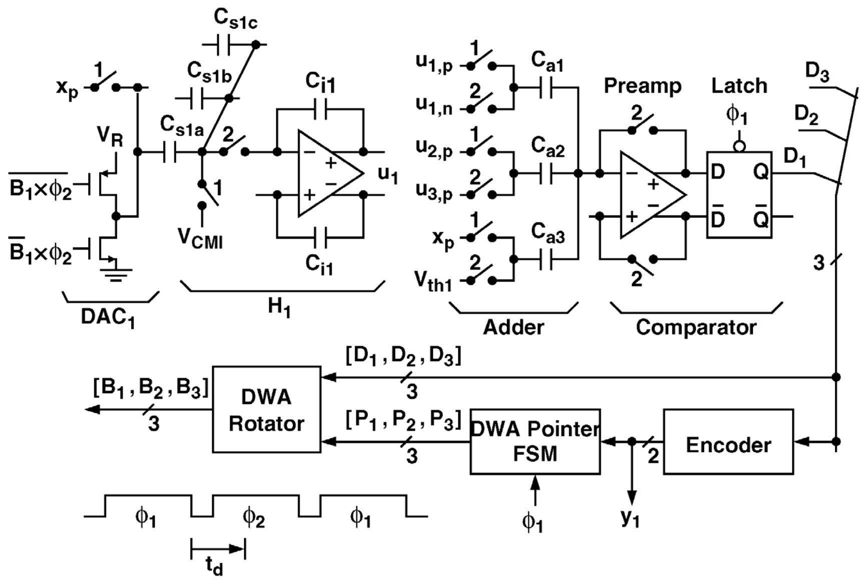

Fig. 8. Schematic of the first loop in the DSM and its timing scheme.

passive adder simultaneously. The sampling switches connected to C_{s1a}, C_{s1b}, and C_{s1c} are boostrapped nMOSFET switches [21]. These switches need to meet the linearity requirement the DSM. The sampling switches connected to the C_{a3} capacitors are regular CMOS switches. The linearity requirement of these switches are less critical.

In Fig. 8, the comparator output set $\mathbf{D} = [D_1, D_2, D_3]$ is a thermometer code. An encoder converts $\mathbf{D}$ into a 2-bit Gray code y_1, which serves as the ADC_1 output. A data-weighted-averaging (DWA) rotator also receives $\mathbf{D}$ and generates the DAC_1 input set $\mathbf{B} = [B_1, B_2, B_3]$ to mitigate the mismatches among C_{s1a}, C_{s1b}, and C_{s1c}. The rotator is a passive switch matrix controlled by a DWA pointer, which is a finite-state machine (FSM) [22].

In Fig. 8, the critical path is from the latch in the comparator to the first integrator H_1. Upon the falling edge of ϕ_1, the latches in all three comparators begin the regeneration process to update $\mathbf{D} = [D_1, D_2, D_3]$. The change must propagate to the DAC_1 switches in time so that the integrator H_1 receives the correct DAC_1 output during $\phi_2 = 1$. The duration from the ϕ_1 falling edge that triggers the latches in the comparators to the ϕ_2 falling edge that ends the H_1 integration operation is only half of the clock period. If the sampling frequency of the DSM is 1 GHz, half of the clock period is 500 ps. We define the propagation delay from the latch in the comparator to the DAC_1 switches as t_d. It is critical to minimize t_d so that the integrator H_1 is given enough time to settle during $\phi_2 = 1$.

As illustrated in Fig. 8, a comparator consists of a preamplifier followed by a latch. The preamplifier is a two-path amplifier that combines the high gain of a two-stage amplifier with the high-speed of a single-stage amplifier [23]. The latch is a cascade of a dynamic sense amplifier [24] and a static S-R latch [25]. The preamplifier has a dc gain of 22 dB. It achieves a unit-gain frequency of 16.5 GHz with a phase margin of 68 degree. The propagation delay t_d defined in Fig. 8 depends on the signal magnitude $|V_a - V_{\mathrm{th1}}|$, where $V_a = x + 2u1 + u2 - u3$ is the comparator input and V_{th1} is the threshold of the comparator. As $|V_a - V_{\mathrm{th1}}|$ decreases, it takes longer time for the latch to regenerate a valid output. In our design, $t_d = 125$ ps if $|V_a - V_{\mathrm{th1}}| = 1$ mV. That leaves about 300 ps for the first integrator H_1 to settle during $\phi_2 = 1$, if the rise time, fall time, and nonoverlapping time of the clocks are taken into account.

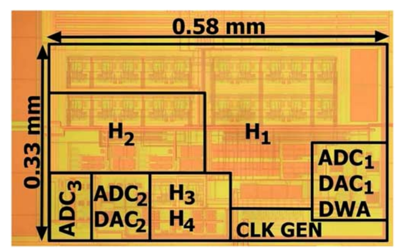

Fig. 9. Modulator chip micrograph.

TABLE II
POWER AND AREA OF CIRCUIT BLOCKS

Block	Power (mW)	Power (%)	Area (%)
Integrator H_1	56.4	60	50
Integrator H_2	17.7	19	22
Integrator H_3	3.75	4	4.5
Integrator H_4	3.75	4	4.5
ADCs, DACs	12.4	13	19
Total	94	100	100

VI. EXPERIMENTAL RESULTS

The DSM shown in Fig. 1 was fabricated using a 65-nm CMOS technology. Fig. 9 shows the chip micrograph. Its active area is 0.58×0.33 mm^2. The calibrations processors CP_1, CP_2, and CP_3 and the noise cancellation filters NCF_1 and NCF_2 are realized off-chip. Operating at $f_s = 1.1$ GHz sampling rate, the chip consumes a total of 94 mW from a 1-V supply. The power and area of the circuit blocks are listed in Table II.

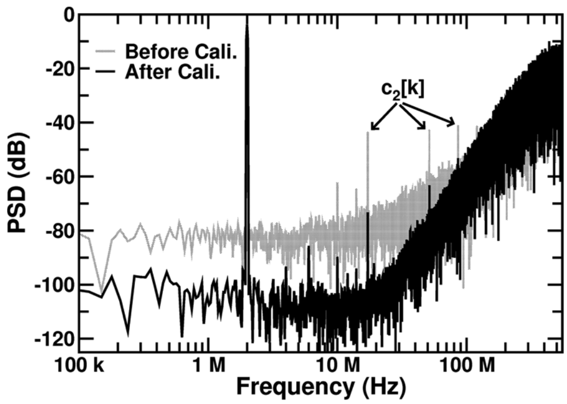

Fig. 10. Measured output spectra of the DSM.

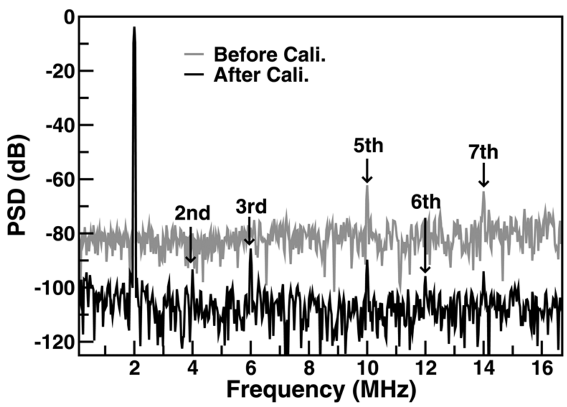

Fig. 11. Measured in-band output spectra of the DSM.

The DSM chip is mounted directly on a printed circuit board for measurement. The ADC outputs, including y_1, y_2, and y_3, are taken off-chip through current-steering buffers with low-voltage-swing differential outputs. The y_1, y_2, and y_3 data were collected using a logic analyzer and analyzed subsequently. The calibration signals c_1 and c_2 are generated on chip. They can be enabled externally. The control signals T_1 and T_2 are generated externally and are fed to the chip to adjust integrators H_1 and H_2. The reference $V_R = 1$ V, the input common-mode voltage $V_{\rm CMI} = (1/4)V_{\rm DD}$, and the output common-mode voltage $V_{\rm CMO} = (1/2)V_{\rm DD}$ are supplied externally. The differential full-scale input range is $\pm V_R$.

The DSM has a sampling rate of $f_s = 1.1$ GHz. Its signal bandwidth is 16.67 MHz if the OSR is 33. Fig. 10 is the measured DSM output spectra before and after the calibration. The input signal is a -3-dBFS 2-MHz sine wave. Without the calibration, the quantization noise of the first stage e_1 dominates the low-frequency band and is shaped by a 40-dB/decade slope for frequencies above 10 MHz. The calibration signal c_2 is visible. It has a frequency of $f_s/64 = 17.19$ MHz. The measured SNR is 57 dB. The SNDR is 54 dB. After the calibration, the quantization noise e_1 is minimized. The noise floor drops, and the noise at high frequency is shaped by a 80 dB/decade slope. The calibration signal c_2 is attenuated by 30 dB. The measured SNR and SNDR become 76 and 74 dB, respectively. If the calibration signal c_1 is injected instead of c_2, the c_1 tones are -34 dB in the DSM output spectra. Fig. 11 shows the passband details of the output spectra. Before the calibration, the fifth and seventh harmonics are the dominant tones. The spurious-free dynamic range (SFDR) is 58 dB. After the calibration, the third harmonic becomes the dominant tone. The SFDR increases to 83 dB.

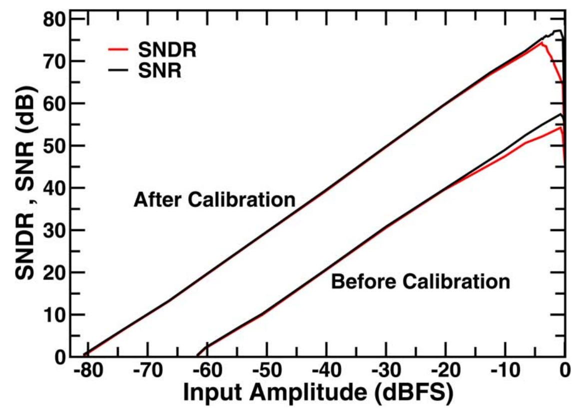

Fig. 12. Measured dynamic performance of the DSM.

Fig. 12 shows the measured SNR and SNDR versus the input signal level. The input is a 2-MHz sine wave. Before the calibration, the peak SNR and the peak SNDR are 57.42 and 54.23 dB, respectively, at -0.71-dBFS input level. The DR is 62 dB. After the calibration, the peak SNR is 77.22 dB at -0.93-dBFS input level, and the peak SNDR is 74.32 dB at -3.85-dBFS input level. The DR increases to 81 dB. Note that, before the calibration, there is a visible difference between the SNR and the SNDR for the input level higher than -20 dBFS. This is because the quantization noise e_1 leaking to the DSM output contains input harmonics. After the calibration, the e_1 leakage is reduced, and the difference between SNR and SNDR is also decreased.

In our design, the opamps employ the constant-current biasing scheme. Simulations show that the dc gain of the opamps varies from 10.74 to 8.76 if the temperature changes from 0 °C to 80 °C. Thus, after calibration, the SNR of the DSM will degrade by -3 dB if the temperature changes by 10 °C. However, this degradation will not occur if the time for the temperature change is much longer than the calibration time constant. On the other hand, the dc gain of the opamp varies from 9.77 to 10.87 if the supply voltage changes from 0.9 to 1.1 V. Thus, after calibration, the SNR degradation is less than -3 dB if the supply voltage variation is less than ± 50 mV.

Table III summarizes the performance of this DSM chip and compares it with other wide-bandwidth DSMs. The figure of merit (FOM) are defined as follows [26]:

$$\mathrm{FOMs} = \mathrm{DR_{dB}} + 10\log_{10}\frac{\mathrm{BW}}{\mathrm{Power}}$$
$$\mathrm{FOMw} = \frac{\mathrm{Power}}{2\mathrm{BW} \times 2^{\frac{(\mathrm{SNDR}-1.76)}{6.02}}}. \qquad (14)$$

The FOMs of this chip is 163.487 dB, and the FOMw is 660 fJ/level. Comparing with other discrete-time (DT) DSMs, this DSM has the highest sampling rate, operates under the lowest supply voltage, and achieves competitive FOMs and FOMw. In Table III, the continuous-time (CT) DSMs show better FOMw

TABLE III
COMPARISON OF WIDE-BANDWIDTH DSMs

Publication	This work	[27]	[28]	[4]	[5]	[6]	[7]	[29]	[30]	[31]	[32]	[33]
Type	DT	DT	DT	DT	DT	DT	DT	CT	CT	CT	CT	CT
Process (nm)	65	65	180	32	180	90	90	90	90	65	130	90
Supply (V)	1.0	1.25	1.8	1.05	1.8	1.2	1.4	1.2	1.2	1.2	1.5	1.4
Clock (MHz)	1100	240	160	400	80	420	330	3600	500	2400	900	600
OSR	33	8	8	10	8	10.5	8	50	10	64	22.5	30
BW (MHz)	16.67	15	20	20	10	20	20	36	25	18.8	20	10
DR (dB)	81	-	64	66	75.5	-	-	83	72	78	-	-
Peak SNR (dB)	77.22	-	63	-	74	72	67	76	69	76	81	83
Peak SNDR (dB)	74.32	67	63	63	74	70	63	71	68	74	78	78
Power (mW)	94	37	16	28	22	28	73	15	8.5	39	87	16
Die Size (mm^2)	0.19	0.28	0.36	0.13	0.62	1	1.3	0.12	0.23	0.075	0.45	0.36
FOMs (dB)	163.5	153*	155	155	162	161*	151*	176.8	167	165	165*	171*
FOMw (pJ/conv.)	0.66	0.67	0.35	0.61	0.27	0.27	1.5	0.07	0.09	0.25	0.33	0.12

* Assume DR equals to peak SNDR or peak SNR.

performance. However, they require clocks of more stringent jitter performance.

VII. CONCLUSION

A fourth-order discrete-time DSM was fabricated using a 65-nm CMOS technology. It has a sampling rate of 1.1 GHz and an input bandwidth of 16.67 MHz with an OSR of 33. We use low-complexity circuits to achieve high speed. The opamps have a unity-frequency of 6 GHz in the integrator configuration, but have a dc gain of only 10. The low-gain opamps result in lossy integrators. We apply the integrator leakage calibration to adjust the leakage-compensating capacitors of the integrators to move their poles β back to 1. We use the noise leakage calibration to minimize the quantization noise of the first loop leaking to the DSM's combined output. The noise leakage calibration relaxes the matching requirement for the MASH structure. The calibration is simplified since it does not need to correct the β coefficients. Both digital calibrations can operate in the background without interrupting the normal DSM operation. The calibration processors are simple digital circuits. They do not have complex filters. The chip's measured SNDR and DR are 74.32 and 81 dB, respectively. The chip consumes 94 mW from a 1-V supply. The active area is 0.33×0.58 mm^2.

We demonstrate that the combination of low-complexity circuits and digital calibration can yield a high-speed high-performance DSM. The design technique is specially suitable for advanced nanoscale CMOS technologies.

APPENDIX A
AVERAGED TRANSIENT BEHAVIOR OF β_1

As shown in Fig. 1, CP_1 receives the ADC_1 output y_1. ADC_1's input thresholds are at $\{0, \pm(2/3)V_R\}$, and its corresponding digital outputs are $y_1 \in \{\pm 1/3, \pm 1\}$. ADC_1 has a conversion gain of $G_{A1} = 1/V_R$. From Fig. 4, the averaged variation of s for one clock cycle is $\Delta s = (D_{g1}V_{cf1}) \times G_{A1}$. The voltage V_{cf1} is expressed as (6). As illustrated in Fig. 5, s takes an average of $N_{\mathrm{th1}}/\Delta s$ cycles to accumulate from 0 to $+N_{\mathrm{th1}}$ (or $-N_{\mathrm{th1}}$). Once s reaches the threshold, T_1 is changed by 1 and β_1 is changed by $\Delta\beta_1$. Thus, the averaged β_1 variation rate is

$$\frac{d\beta_1}{dk} = \frac{\Delta\beta_1}{N_{\mathrm{th1}}/\Delta s} \approx \frac{\Delta\beta_1 D_{g1} V_{c1}}{\alpha_1 N_{\mathrm{th1}} V_R}(1-\beta_1). \tag{15}$$

The above equation leads to (7) and (8).

APPENDIX B
AVERAGED STANDARD DEVIATION OF β_1

When the H_1 calibration process converges, the behavior of β_1 becomes a discrete random fluctuation around 1. If $N_{th1} = \infty$, β_1 alternates between only two values, which are $\beta_a = 1 - x\Delta\beta_1$ and $\beta_b = 1 + (1-x)\Delta\beta_1$, where $0 \leq x \leq 1$ depending on $\beta_{1,0}$. Define the probability for $\beta_1 = \beta_a$ as P_a, and the probability for $\beta_1 = \beta_b$ as P_b. Since the expected value of β_1 is 1, i.e., $\beta_a P_a + \beta_b P_b = 1$, we have $P_a = 1 - x$ and $P_b = x$. If x is given, define the standard deviation of β_1 as

$$\sigma(\beta_1[x]) = \sqrt{(\beta_a - 1)^2 P_a + (\beta_b - 1)^2 P_b} = \Delta\beta_1 \sqrt{x(1-x)}. \tag{16}$$

If x is uniformly distributed from 0 to 1, the standard deviation of β_1 is

$$\sigma(\beta_1) = \sqrt{\int_0^1 \sigma\left(\beta_1[x]\right)^2 dx} = \frac{\Delta\beta_1}{\sqrt{6}}. \tag{17}$$

The above equation is the same as (9).

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REFERENCES

[1] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance adapting compensation for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 445–451, Feb. 2011.

[2] H. Yoshizawa, T. Yabe, and G. C. Temes, "High-precision switched-capacitor integrator using low-gain opamp," *Electron. Lett.*, vol. 47, no. 5, p. 315, 2011.

[3] T. Musah and U.-K. Moon, "Correlated level shifting integrator with reduced sensitivity to amplifier gain," *Electron. Lett.*, vol. 47, no. 2, p. 91, 2011.

[4] B. Carlton, H. Lakdawala, E. Alpman, J. Rizk, Y. Li, B. Perez-Esparza, V. Rivera, C. Nieva, E. Gordon, P. Hackney, C.-H. Jan, I. Young, and K. Soumyanath, "A 32 nm, 1.05 V, BIST enabled, 10–40 MHz, 11-9 Bit, 0.13 mm^2 digitized integrator MASH $\Delta\Sigma$ ADC," in *Proc. Symp. VLSI Circuits*, 2011, pp. 36–37.

[5] S. Lee, J. Chae, M. Aniya, S. Takeuchi, K. Hamashita, P. K. Hanumolu, and G. C. Temes, "A double-sampled low-distortion cascade $\Delta\Sigma$ modulator with an adder/integrator for WLAN application," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2011, pp. 1–4.

[6] P. Malla, H. Lakdawala, K. Kornegay, and K. Soumyanath, "A 28 mW spectrum-sensing reconfigurable 20 MHz 72 dB-SNR 70 dB-SNDR DT $\Delta\Sigma$ ADC for 802.11n/WiMAX receivers," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 496–631.

[7] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "An 11-Bit 330 MHz 8X OSR $\Sigma - \Delta$ modulator for next-generation wlan," in *Proc. Symp. VLSI Circuits*, Dec. 2006, pp. 166–167.

[8] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Piscataway, NJ, USA: IEEE, 2005.

[9] J. Silva, X. Wang, P. Kiss, U. Moon, and G. C. Temes, "Digital techniques for improved $\Delta\Sigma$ data conversion," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2002, pp. 183–190.

[10] Z. Zhang, J. Steensgaard, G. C. Temes, and J.-Y. Wu, "A 14-bit dual-path 2-0 MASH ADC with dual digital error correction," *Analog Integr. Circuits Signal Process.*, vol. 59, no. 2, pp. 143–150, Dec. 2008.

[11] N. Maghari, S. Kwon, and U.-K. Moon, "74 dB SNDR multi-loop sturdy-mash delta-sigma modulator using 35 dB open-loop opamp gain," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2212–2221, Aug. 2009.

[12] R. Baird and T. Fiez, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II, Analog Dig. Signal Process.*, vol. 42, no. 12, pp. 753–762, Dec. 1995.

[13] J. Silva, U. Moon, J. Steensgaard, and G. Temes, "Wideband low-distortion delta-sigma ADC topology," *Electron. Lett.*, vol. 37, no. 12, p. 737, 2001.

[14] J. Silva and G. C. Temes, "Low-distortion delta-sigma topologies for MASH architectures," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2004, pp. I-1144–I-1147.

[15] R. Schreier, "On the use of chaos to reduce idle-channel tones in delta-sigma modulators," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 41, no. 8, pp. 539–547, Aug. 1994.

[16] C.-C. Huang and J.-T. Wu, "A background comparator calibration technique for flash analog-to-digital converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 9, pp. 1732–1740, Sep. 2005.

[17] C.-Y. Wang and J.-T. Wu, "A multiphase timing-skew calibration technique using zero-crossing detection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 6, pp. 1102–1114, Jun. 2009.

[18] C.-C. Huang, C.-Y. Wang, and J.-T. Wu, "A CMOS 6-Bit 16-GS/s time-interleaved ADC using digital background calibration techniques," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 848–858, Apr. 2011.

[19] S. Rabii and B. Wooley, "A 1.8-V digital-audio sigma-delta modulator in 0.8- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783–796, Jun. 1997.

[20] K. Nam, S.-M. Lee, D. Su, and B. Wooley, "A low-voltage low-power sigma-delta modulator for broadband analog-to-digital conversion," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1855–1864, Sep. 2005.

[21] H. Park, K. Nam, D. Su, K. Vleugels, and B. Wooley, "A 0.7-V 870-μW digital-audio CMOS sigma-delta modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1078–1088, Apr. 2009.

[22] S.-J. Huang and Y.-Y. Lin, "A 1.2 V 2 MHz BW 0.084 mm^2 CT $\Delta\Sigma$ ADC with -97.7 dBc THD and 80 dB DR using low-latency DEM," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 172–173, 173a.

[23] M. Bolatkale, L. J. Breems, R. Rutten, and K. A. A. Makinwa, "A 4 GHz continuous-time $\Delta\Sigma$ ADC with 70 dB DR and 74 dBFS THD in 125 MHz BW," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2857–2868, Dec. 2011.

[24] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18 ps setup+hold time," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2007, pp. 252–253.

[25] B. Nikolic, V. Oklobdzija, V. Stojanovic, and M. Ming-Tak Leung, "Improved sense-amplifier-based flip-flop: Design and measurements," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 876–884, Jun. 2000.

[26] V. Singh, N. Krishnapura, S. Pavan, B. Vigraham, D. Behera, and N. Nigania, "A 16 MHz BW 75 dB DR CT $\Delta\Sigma$ ADC compensated for more than one cycle excess loop delay," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1884–1895, Aug. 2012.

[27] S.-C. Lee, B. Elies, and Y. Chiu, "An 85 dB SFDR 67 dB SNDR 8OSR 240 MS/s $\Delta\Sigma$ ADC with nonlinear memory error calibration," in *Proc. Symp. VLSI Circuits*, Jun. 2012, vol. 1, pp. 164–165.

[28] J. Chae, S. Lee, M. Aniya, S. Takeuchi, K. Hamashita, P. K. Hanumolu, and G. C. Temes, "A 63 dB 16 mW 20 MHz BW double-sampled $\Delta\Sigma$ analog-to-digital converter with an embedded-adder quantizer," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, vol. 1, pp. 1–4, no. c.

[29] P. Shettigar and S. Pavan, "Design techniques for wideband single-bit continuous-time $\Delta\Sigma$ modulators with FIR feedback DACs," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2865–2879, Dec. 2012.

[30] P. Witte, J. G. Kauffman, J. Becker, Y. Manoli, and M. Ortmanns, "A 72 dB-DR $\Delta\Sigma$ CT modulator using digitally estimated auxiliary DAC linearization achieving 88 fJ/conv in a 25 MHz BW," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2012, vol. 24, no. 3, pp. 154–156.

[31] G. Taylor and I. Galton, "A reconfigurable mostly-digital $\Delta\Sigma$ ADC with a worst-case FOM of 160 dB," in *Proc. Symp. VLSI Circuits*, Jun. 2012, pp. 166–167.

[32] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time $\Delta\Sigma$ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, Dec. 2009.

[33] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, and P. K. Hanumolu, "A 16-mW 78-dB SNDR 10-MHz BW CT $\Delta\Sigma$ ADC using residue-cancelling VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2916–2927, Dec. 2012.

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