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Modulation of Interface and Bulk States in Amorphous InGaZnO Thin-Film Transistors with Double Stacked Channel Layers

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A high-performance amorphous InGaZnO (a-IGZO) thin-film transistor (TFT) was achieved using a double stacked channel layer (DSCL). An oxygen-poor IGZO film was deposited in pure argon ambient as a buffer layer to prevent oxygen plasma bombardment and improve device performance. An oxygen-rich IGZO film was then deposited on top of that buffer layer to modulate device stability. With this structure, an interface with low oxygen-plasma-induced damage and few oxygen vacancies in the bulk was achieved using DSCL, leading to a higher stability of the threshold voltage. © 2013 The Japan Society of Applied Physics

Amorphous InGaZnO (a-IGZO) is a very promising channel material in thin-film transistors (TFTs) for advanced applications in flat panel display, because of its advantages such as high mobility, room-temperature deposition, and potential flexibility. To date, much effort has been devoted to improve the electrical performance of a-IGZO TFTs.[1–5] However, the stability of a-IGZO TFTs still remains the most crucial issue for their practical applications. For oxide TFTs, their stability has been found to be dominated by interface traps (between the channel layer and gate insulator) and/or bulk traps in the channel layer. Thus, it is important to optimize the interface and bulk states of a-IGZO TFTs to achieve better stability. Generally, interface states could be improved by thermal annealing, plasma treatment, or the use of a high-*k* dielectric as a gate insulator,[6–8] while better bulk states might be achieved using appropriate conditions for channel layers, such as chamber pressure and reactive gases.[9,10] In particular, front-channel and back-channel protecting layers were applied to improve the interface and bulk states.[11] Recently, it has been reported by our group and other researchers that a TFT with a double-stacked channel layer (DSCL) might exhibit better performance and stability since its interface and bulk states could be effectively modulated.[12,13] However, those previous reports have not clearly explained the mechanism underlying the improvement. Moreover, design rules for DSCLs, e.g., how to define the thickness in DSCL IGZO-TFTs are still unclear. In this study, the effects of both the thickness of the front-channel layer and the oxygen flow rate (OFR) for the back-channel layer on the performance and stability of DSCL IGZO TFTs are studied. In particular, the impact of oxygen plasma damage to the front channel interface is discussed. Finally, the design rules for DSCL are summarized.

We fabricated a DSCL by firstly depositing an IGZO layer in pure argon ambient, and then depositing a subsequent IGZO layer under controlled oxygen pressure. The rationale of the experimental design is to prevent oxygen plasma from damaging the interface between the gate-insulation and channel layers, as oxygen plasma causes more damages than argon plasma. The second-step deposition under controlled oxygen pressure is to control oxygen vacancies for better device stability.[12,13]

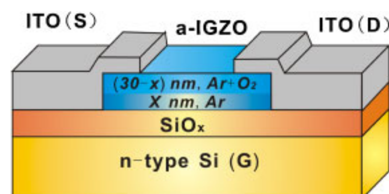

Fig. 1. (Color online) Schematic diagram of the a-IGZO TFT with DSCL. An x-nm-thick a-IGZO film was deposited without oxygen, then a $(30 - x)$-nm-thick a-IGZO film was deposited at different OFRs. The total thickness of the channel layer was fixed at 30 nm.

The device was fabricated as follows: As shown in Fig. 1, a piece of heavily doped silicon substrate was used as the gate electrode, and a-IGZO channel layers were grown by RF magnetron sputtering at room temperature on a 100-nm-thick thermal SiO_2 as the gate insulator. The a-IGZO channel and source/drain electrodes were defined by a shadow mask. ITO layers as source/drain electrodes were deposited by RF magnetron sputtering. For the channel layer, IGZO films deposited without and with oxygen, called oxygen-poor (pure argon ambient) and oxygen-rich IGZO films, were served as the front- and back-channel layers, respectively. The total thickness of channel layer was fixed at 30 nm, and TFTs with front-channel layers of various thicknesses (x) were fabricated to study the thickness effects on device performance and stability. The channel length (L) and channel width (W) were 200 and 1000 μm, respectively. All of the a-IGZO TFTs were annealed at 350 °C for 1 h in a nitrogen furnace to improve their electrical properties. The thickness of the a-IGZO films was determined by atomic force microscopy (Vecco Nanoscope IIIA) and the oxygen content of the a-IGZO films was measured by X-ray photoemission spectroscopy (XPS; Thermal-fisher ESCLAB 250). The electrical characteristics of a-IGZO TFTs were obtained at room temperature using a Keithley 4200 semiconductor characterization system.

It has been reported that the increase in OFR for deposition may produce IGZO films of higher oxygen contents. Here, we further carried out XPS measurement to verify this point. The XPS spectra of O 1s signals in three types of a-IGZO thin films deposited at different OFRs of 0 (pure argon

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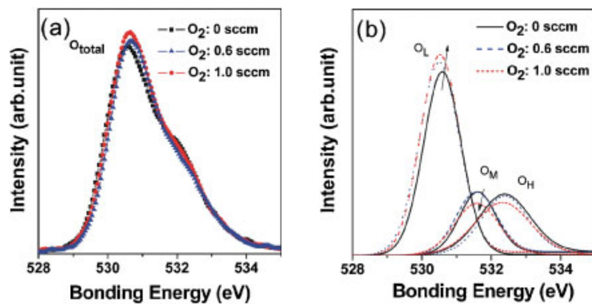

Fig. 2. (Color online) XPS spectra of IGZO thin films: (a) O 1s at different OFRs. (b) The O_H, O_M, and O_L fitting spectra extracted from the O 1s of IGZO films deposited at different OFRs of 0, 0.6, and 1.0 sccm, respectively.

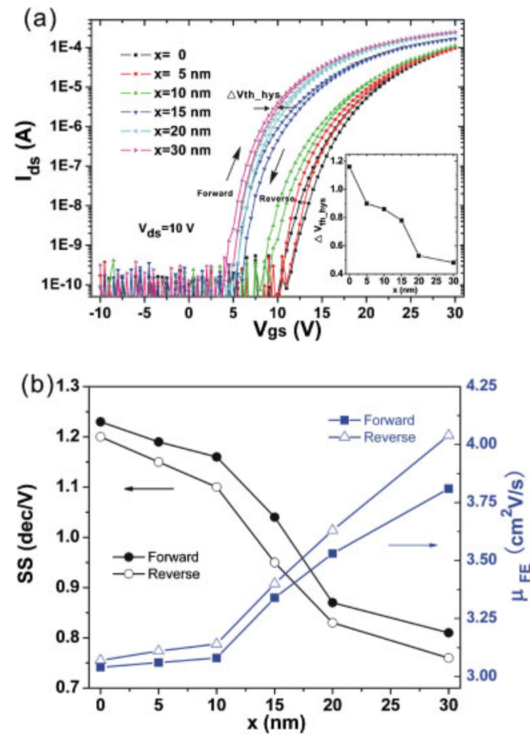

Fig. 3. (Color online) (a) I_{ds}–V_{gs} multisweep transfer curves at $V_{ds} = 10$ V, and (b) SS and μ_{FE} for the DSCL TFTs as functions of the thickness (x) of the front channel layer deposited without oxygen. The back-channel layer was deposited at an OFR of 0.6 sccm.

ambient), 0.6, and 1.0 sccm are shown in Fig. 2(a). The O 1s peak can be fitted by three nearly Gaussian distributions, approximately centered at 530.5, 531.6, and 532.4 eV,[14] as shown in Fig. 2(b). The low-binding-energy peak (O_L) at 530.5 eV is related to O^{2-} ions that combined with the Zn, Ga, and In atoms in the IGZO compound system. The high-binding-energy peak (O_H) at 532.4 eV is associated with loosely bonded oxygen on the IGZO film surface, such as $-CO_3$, absorbed H_2O, and O_2. The binding energy component (O_M) at 531.6 eV is attributed to O^{2-} ions that are in the oxygen-deficient region in the IGZO matrix. In general, O_M-related oxygen vacancies supply free-electron carriers in the IGZO film, resulting in an increase in electron concentration.[2] The decrease in area of the O_M peak with increasing OFR is attributed to the reduction in the number of oxygen vacancies, resulting from the abundant supply of O atoms. The ratios of oxygen vacancies to total oxygen (O_M/O_{tot}) in IGZO films significantly diminishes from 18.65 to 17.74% as the OFRs decrease from 1.0 to 0 sccm. Our results provide quantitative evidence indicating that a-IGZO films of fewer oxygen vacancies can be achieved by reducing the OFR for the deposition of IGZO films.

It was reported by our group that using an oxygen-poor IGZO film as a front-channel layer improved device performance and interface states.[12] In this study, DSCL a-IGZO TFTs with different-thickness front-channel layers were proposed to further investigate the improvement in interface states, which were not well studied previously. The electrical characteristics of DSCL TFTs with different-thickness front-channel layers are shown in Fig. 3(a), where a hysteresis loop was obtained under a sweeping V_{gs} from -10 to 30 V at the same sweep speed. Here, IGZO films deposited at an OFR of 0.6 sccm were used as the back-channel layer. The related performance parameters including field effect mobility (μ_{FE}), subthreshold swing (SS), and ΔV_{th_hys} are shown in Fig. 3(b). ΔV_{th_hys} shown in Fig. 3(a) is defined as the threshold voltage (V_{th}) change in hysteresis loops. It is found that, as the thickness (x) of the front-channel layer increases, better electrical properties are achieved, such as higher μ_{FE}, lower SS, and lower ΔV_{th_hys}, which were associated with the increase in the carrier density of the channel layer.[12] Positive shifts in the hysteresis loops are observed, which could be ascribed to interface states between the channel layer and the gate insulator.[15] For forward sweeping, the interface states initially discharge trapped carriers and then begin trapping carriers while gate bias sweeps into the subthreshold region. Hence, lower SSs for the samples are obtained. Unfilled interface states could also degrade the effective mobility, as shown in Fig. 3(b). In contrast, for reverse sweeping, interface states are filled with carriers and become noninfluential in the subthreshold region, so that SS decreases. Moreover, carrier trapping/detrapping causes hysteresis. Thus, this result suggests that the improvement in the hysteresis characteristic of DSCL TFTs with thicker front-channel layers contributes to fewer traps at or near the channel layer-gate insulator interface, and an oxygen-poor IGZO film appears to be a buffer layer.

The mechanism for the oxygen-poor IGZO film serving as a front-channel layer could be explained as follows. For a-IGZO with DSCL, when oxygen is applied at a flow rate that produces oxygen-rich IGZO film as a back-channel layer, the effect of oxygen plasma on the channel layer-gate insulator interface should be considered. For the device fabricated with oxygen ($x = 0$ nm), more traps could be created at or near the interface between the channel layer and the gate insulator owing to the ion bombardment of oxygen plasma, leading to higher SS and ΔV_{th_hys}. While the front-channel layer of the IGZOs film deposited in pure argon ambient is applied, the oxygen plasma damage could be alleviated and a decrease in the interface trap density is observed, leading to the improvement in SS. Therefore, when the thickness (x) of the front-channel layers increases to 20 nm or larger, a slight change in SS is observed. This reveals that, as the front-channel layer formed by oxygen-poor a-IGZO film is thick enough, which acts as a buffer

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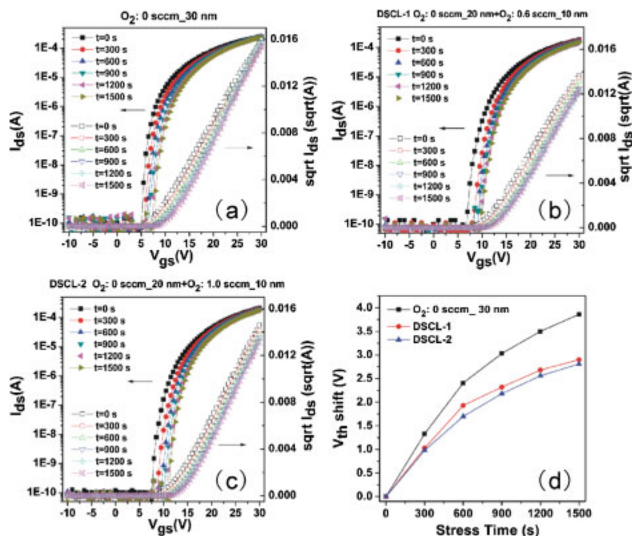

Fig. 4. (Color online) Time variations of (a)–(c) transfer curves and (d) threshold voltage shifts for TFTs with single channel layer, and different DSCLs under positive bias stress at room temperature.

layer, the number of defects induced by the following processes for the back-channel layer using oxygen-rich a-IGZO film is effectively reduced.

According to the investigation of the thickness effect of the front-channel layer on device performance, a 20-nm-thick oxygen-poor IGZO film was adopted as the front-channel layer, which was found to be thick enough to achieve a good interface state. On the other hand, it is also important to employ an oxygen-rich IGZO film as a back channel to improve device stability. Therefore, we applied the IGZO film depostied at different OFRs of 0, 0.6, and 1.0 sccm as the back-channel layers, respectively. The hysteresis of those devices reveals that stable interface states could be obtained (data not shown here). A DC-positive bias stress for 1,500 s was applied to TFTs with DSCL and single channel layer at room temperature in the ambience. Figure 4 shows the dependence of stress time on V_{th} for three types of a-IGZO TFTs under the stress conditions of $V_{gs} = 20$ V and $V_{ds} = 0$ V. It can be seen that all the devices exhibit positive shifts in V_{th} with little changes in SS and μ_{FE}. Importantly, the TFTs with DSCL are more stable than those with a single channel layer. Besides, DSCL-2 (OFR of 1.0 sccm for the back-channel layer) shows the highest stability among the three types of IGZO TFTs.

For the a-IGZO TFTs with a DSCL, there are several reasons for the improved device stability. First, back-channel layers influence the bulk state of the entire channel layer. It was reported that the PBS-induced V_{th} shift was contributed to charge trapping at the channel layer-gate insulator interface and/or in the bulk of the channel layer, when slight changes in SS and μ_{FE} were observed.[14] Since similar front-channel layer interface states are obtained for the three types of TFTs, the increase in OFR for the back-channel layer leads to fewer oxygen vacancies in the entire channel layer. Thus, fewer defects in the bulk are achieved, resulting in better device stability. Second, the ambient effect may induce instability for unpassivated TFTs, which was discussed previously.[12] Therefore, the variation in the bulk state and the back-channel layer leads to a difference in the PBS for a-IGZO TFTs.

Therefore, we can draw a conclusion on the basic design rules of DSCL IGZO TFTs. With an increase in front-channel-layer thickness, the electrical performance of DSCL IGZO-TFTs is improved owing to better interface states. However, an oxygen-rich IGZO of the back-channel layer is required to enhance electrical stability owing to the decrease in the number of bulk traps and/or ambient effect. According to our experimental results, the device with a front-channel layer of $x = 20$ nm and a back-channel layer deposited at an OFR of 1.0 sccm is the best conditions for achieving both relatively good performance parameters ($\mu_{FE} = 3.60\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, SS = 0.91) and good stability ($\Delta V_{th} = 2.81$ V).

In summary, the electrical performance and stability of a-IGZO TFTs with DSCL are investigated. An improved interface is obtained using an oxygen-poor IGZO film of appropriate thickness as the front channel layer, which acts as a buffer layer for reducing the oxygen plasma damage to the channel layer/gate insulator interface induced by the process of the upper oxygen-rich IGZO film. On the other hand, compared with conventional TFTs with single channel layers, TFTs with DSCL may achieve better electrical stability owing to weaker ambient effect and fewer defects in the bulk. The results indicate that not only the interface property but also the device stability of IGZO TFTs could be improved if an appropriate DSCL structure is designed.

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