TECHNICAL PAPER

A low-power self-biased rail-to-rail preamplifier as a readout circuit for a capacitor-type microphone

Tse-Yi Tu · Paul C. -P. Chao · Yueh-Teng Mai

Abstract This study is dedicated to design a readout circuit to extract the output signal of a capacitive-type MEMS microphone. A low-power preamplifier is forged for a capacitive-type microphone to meet the demands on cell phone applications. The design starts with modeling the electro-mechanical behavior of a biased capacitive-type microphone using combination of AV and DC voltages sources. This aims to enable co-simulation of the microphone and the readout circuit design. The output signal of a capacitance-to-voltage converter is normally small and may cause substantial noise in the output signals. Therefore, a preamplifier is designed and applied to amplify the signal to an acceptable level for the convenience of ensuing signal processing. The designed readout circuit consists of two main sub-circuits, responsible for functions in two different stages. One is a newly-designed self-bias circuit in the structure of a capacitance-to-voltage converter at the first stage, while another is a low-voltage low-power two-stage or rail-to-rail MOS operational amplifier at the second stage. The proposed circuit is implemented by using the technology of TSMC 0.35 μm Mixed-Signal MODE (2P4M, 3.3 V/5 V) POLYCIDE. The supply voltage is fixed at low voltage (3 V), the total power dissipation is merely 200 μW. Experiments are finally conducted to validate the performance of the designed readout circuit from 20 to 20k Hz with appropriate add-on high- and low-pass filters.

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1 Introduction

Recent advances in the technology of micro-electro-mechanical systems (MEMS) (ITRC 2005) have accelerated design and application a micro-sensors and actuators based on electrostatic actuation. The MEMS microphone becomes popular electronic device to be implemented in cell phones. As the traditional microphone, the MEMS microphone (Bergqvist and Rudolf 1994; Bernstein and Borenstein 1996; Scheeper et al. 1994; Kuhnel and Hess 1992) could be capacitive-type, piezo-resistive, piezo-electronic or optical (Bergqvist 1993; ITRC 2005; Voorthuyzen et al. 1989; Hsu et al. 1998; Hsieh et al. 1997). For the MEMS microphone, it is generally the capacitive-type microphone (Bergqvist and Rudolf 1994; Bernstein and Borenstein 1996; Scheeper et al. 1994; Kuhnel and Hess 1992). A capacitive-type microphone has a dielectric material that has been charged or discharged. Special material and structure are involved in the device, making the electronic characteristics complex beyond linearity.

This work is focused on designing a new sensing readout circuit for electrets condenser microphone sensor in acoustic application with low-power dissipation (Baker and Sarpeshkar 2003; Hsu et al. 1998, 2007; Huang et al. 2011; Ferri et al. 2007; Chiang et al. 2010). Due to the rising demand for portable battery-operated electronic devices, a low-power preamplifier is designed in this study for electrets condenser microphone to meet the needs from cell phone applications. The designed readout circuit consists of two main sub-circuits, responsible for the functions in two different stages. One is a novel self-bias circuit for the central output of the capacitance-to-voltage converter at the first stage, while the other is a low-power high-swing rail-to-rail MOS operational amplifier (Hui 2007; Cheng 2006; Guo et al. 2011;

Arbet et al. 2012) in the second stage. This self-bias circuit is aimed to read the microphone signal at the first stage, while the rail-to-rail MOS operational amplifier amplifies the output signal of the self-biased circuit in the second stage. The proposed circuit is implemented by using the TSMC 0.35 μm Mixed-Signal MODE (2P4M, 3.3 V/5 V) POLYCIDE technology. The supply voltage is fixed at low voltage (3 V), the power dissipation is only 200 μW. The experiment results are validated. It is shown that the proposed preamplifier circuit can be widely used at low-power, low-voltage applications, such as electrets condenser microphones.

2 Capacitive MEMS condenser microphone

Many types of small-sized microphones can be constructed using silicon micro- machining techniques at low cost; therefore promising for consumer electronics. Three types of silicon microphones have been developed: piezoelectric, piezoresistive, and capacitive-type. Capacitive micro-phones show the highest sensitivity while maintaining low power consumption. In this study aluminum is used for the diaphragm electrode which is the same as the backplate electrode as shown in Fig. 1. The performance of the microphone depends on the size and residual stress of the diaphragm. Other parameters, such as air gap distance and the bias voltage, also affect the sensitivity. The mechanical behavior of the microphone can be described by the mechanical equivalent circuit as shown in Fig. 2, which relates force (potential) and velocities (flow) in the microphone structure. For a complete description of this circuit, radiation and compliance of the diaphragm, air-streaming resistance in the air gap and acoustic holes in backplate, and compliance of the backplate and back-chamber are included (Bergqvist 1993). The mechanical components in the equivalent circuit are given by the following relations. Diaphragm radiation:

$$R_r = \frac{\rho_0 a^4 \omega^2}{2\pi c}, \ M_r = \frac{8\rho_0 a^3}{3\pi\sqrt{\pi}}. \tag{1}$$

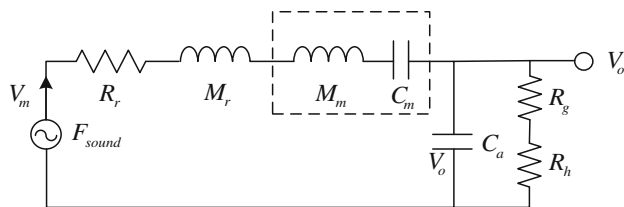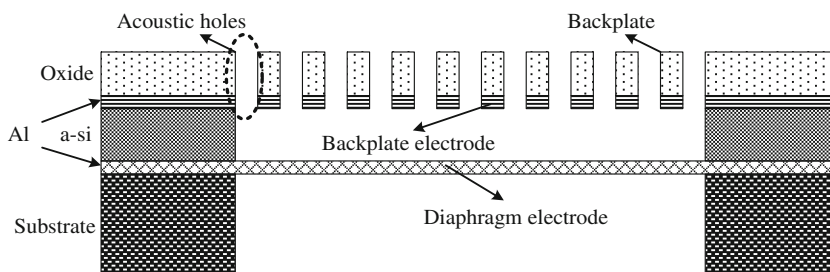Diaphragm compliance and mass inertia are, respectively,

Fig. 2 Equivalent electrical circuit of the capacitor-type condenser microphone

$$C_m \cong \frac{32a^2}{\pi^6(2\pi^2 D + a^2 T)}, \ M_m = \frac{\pi^4 \rho(2\pi^2 D + a^2 T)}{64T}. \tag{2}$$

The viscosity loss in the air gap and its compliance is

$$R_g = \frac{12ua^2}{nd^3\pi}\left(\frac{\alpha}{2} - \frac{\alpha^2}{8} - \frac{\ln\alpha}{4} - \frac{3}{8}\right), \ C_a = \frac{d}{\rho_0 c^2 \alpha^2 a^2}. \tag{3}$$

The viscosity loss of back plate holes is approximated as (Voorthuyzen et al. 1989):

$$R_h \approx \frac{8uha^2}{\pi n r^4}. \tag{4}$$

In the above equations, a is the side length of the microphone, ρ_0 is the density of air, c is the speed of sound in air, ω is the angular frequency, ρ is tensile force per unit length, and n is the hole density in the backplate, and α is the surface fraction occupied by the holes, and u is the air viscosity coefficient, and d is the average air gap distance, and h is the back plate height and r is the radius of hole. The sensitivity of the microphone is then the output voltage under the presence of the acoustical pressure loading, i.e.

$$S_e = \frac{V_0}{P} = \frac{V_b a^2}{j\omega d Z_t}. \tag{5}$$

where P is the sound pressure, V_b is the bias voltage between two electrodes, and Z_t is the total equivalent impedance of the circuit, which is

$$Z_t = R_r + j\omega(M_r + M_m) + \frac{1}{j\omega C_m} + \frac{R_g + R_h}{1 + j\omega(R_g + R_h)C_a}. \tag{6}$$

The sensitivity of the microphone, S_e, is henceforth a function of the frequency. A goal in our design is to
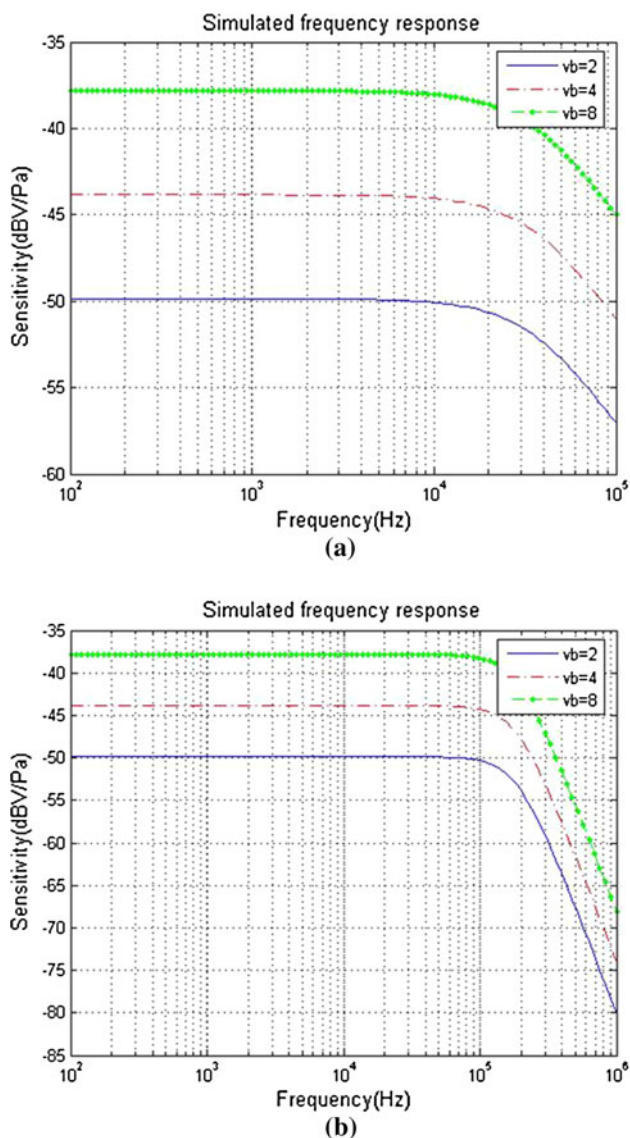
Fig. 1 Cross section of the capacitor-type condenser microphone

Fig. 3 Calculated sensitivity frequency response for a 2 mm microphone with **a** 400; **b** 256 backplate holes/mm^2

maximize the sensitivity subject to fabrication and bias voltage constraints.

Seven design variables are considered: diaphragm edge width, diaphragm thickness, air gap distance, back plate thickness, holes edge width, and the surface fraction occupied by the holes. Based on typical designs, the frequency response is calculated for the microphone at different holes, which is shown in Fig. 3. The sensitivity decays in the high frequency range due to viscous loss in the air gap and back vent holes. The polarization voltage is the DC voltage in the preamplifier. One of the design factors for the preamplifier is to determine the DC voltage that affects on C–V converter at first stage of the preamplifier. The input stage of the C–V converter needs to

amplify the output of the microphone which is as small as 1–3 mV. Therefore, at the second stage of preamplifier design is to magnify the signal.

3 CMOS Readout circuit design

A low-power, low-voltage preamplifier of the capacitive-type MEMS microphone is designed in this study. First, a capacitance-to-voltage converter is forged to extract the signal in quality from the microphone. It is noted that the capacitance in the structure of two plates is changed by the sound pressure. One of the plates is a membrane is vibrated and then change the capacitance of the microphone. Second, in order to get large signal, an amplifier is designed to increase the magnitude of the signal. This amplifier is realized by a traditional two-stage operational amplifier. While the preliminarily-designed capacitance-to-voltage converter and the two-stage amplifier are combined, the output signal is found nonlinear at different frequencies. In order to improve the linearity of the preamplifier, the rail-to-rail amplifier is designed and used to render large input, better linearity, output swing range and higher SR (Slew Rate).

3.1 A self-bias circuit for centering the output of the capacitance-to-voltage converter

A capacitance-to-voltage converter is designed herein which does not amplifier the signal, but reads the capacitance of the capacitor-type microphone. There are high input resistor and low output resistor in the circuit. This circuit has eight p-type transistors and two capacitances and two resistors, shown in Fig. 4. One of the sub-circuits is the very low pass filter that has non-sensitive for alternating current. Another one is the high pass filter that limits the low frequency of the bandwidth and filters the direct current of the microphone. From Fig. 4, considering the direct current, getting

$$V_{p1} - V_{CC} = V_{DC} - V_{O}. \tag{7}$$

In order to keep the midway of the output, substituting $V_O = \frac{1}{2}V_{CC}$ into Eq. 7 gives

$$V_{p1} = \frac{1}{2}V_{CC} + V_{DC}. \tag{8}$$

V_{p1} is the result of V_{p2} that pass though the low pass filter. Then V_{p1} and V_{p2} have the same direct current. Therefore, yielding

$$V_{p1} - V_{CC} = V_{DC} - \frac{1}{2}V_{CC}, \quad V_{p2} = \frac{1}{2}V_{CC} + V_{DC}, \tag{9}$$
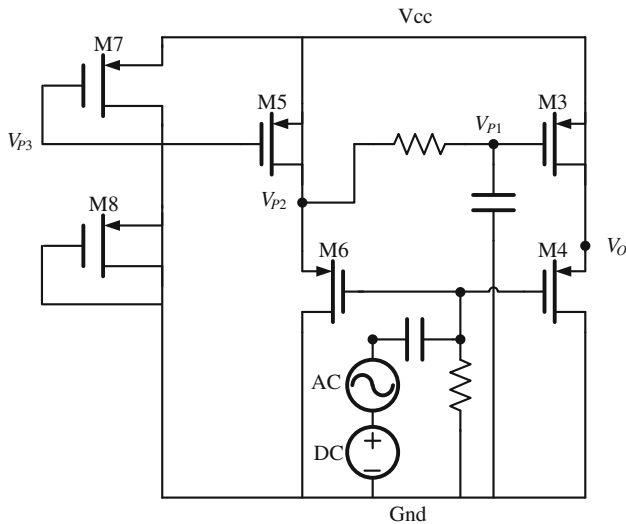
Fig. 4 The self-bias for the central output of capacitance-to-voltage converter

$$V_{p3} - V_{CC} = V_{DC} - V_{p2} = V_{DC} - \left(\frac{1}{2}V_{CC} + V_{DC}\right),$$

$$V_{p3} = \frac{1}{2}V_{CC}. \tag{10}$$

In order to keep Eq. 10 that M_7 and M_8 must connect drain and gate. Considering the alternating current, and Eq. 8 getting

$$V_{p1} - V_{CC} = (V_{DC} + V_{AC}) - V_O, \ V_O = \frac{1}{2}V_{CC} + V_{AC}. \tag{11}$$

In this circuit, the low pass and high pass filters play important roles in the design. The input stage in Fig. 4 consists of those managing the alternating current and the direct current of the capacitor-type microphone. The direct current part takes care of the dc bias of the microphone, while the current part does the variation from the capacitance of the microphone. In this way, the output is changed by the current part of the capacitor-type microphone.

3.2 Rail-to-rail low-voltage low-power differential amplifier

3.2.1 Two-stage operational amplifier

It is common that the AC component in the output voltage of the previous newly-designed self-bias converter, as shown in Eq. 11 is considerably small as compared to its DC counterpart $\frac{1}{2}V_{CC}$. Therefore, the amplifier needs to be designed subsequently to simplify the AC component that
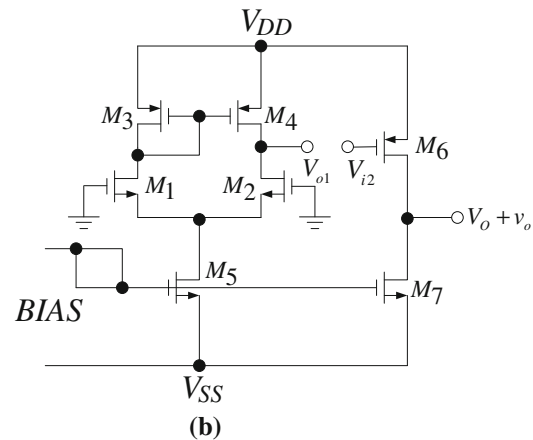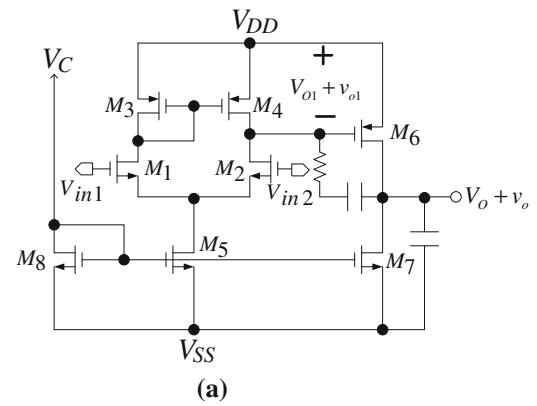

(a)

(b)

Fig. 5 a More-detailed schematic diagram of a typical two-stage operational amplifier. **b** Two-stage amplifier with first and second stages disconnected to show the effect of interstage coupling on input-referred offset voltage

embeds sound content (Lee and Higman 2011; Guo et al. 2011).

This system is basic on two-stage operational amplifier. To calculate the *PSRR* from the V_{DD} supply for the op amp in Fig. 5a, we will divide the small-signal gain $A^+ = v_0/v_{dd}$ into the gain from the input. For this calculation, assume that the V_{SS} supply voltage is constant and that both op-amp inputs in Fig. 5a are connected to small-signal ground. As the applied frequency increases, the impedance of the compensation capacitor in Fig. 5a decreases, effectively shorting the gate of M_6 to its drain for high-frequency ac signals. If the gate-source voltage on M_6 is constant, the variation on the negative supply is fed directly to the output at high frequencies. Therefore, $A^- \approx 1$ at frequencies high enough to short the capacitor, assuming the compensation capacitor is bigger than load capacitor. The same phenomenon causes the gains A_{dm} and A^+ to decrease as frequency increases, so that the $PSRP^+$ remains relatively constant with increasing frequency. Since A^- increases to unity as A_{dm}, however, $PSRP^-$ decreases and reaches unity at the frequency where $|A_{dm}| = 1$.

3.2.2 Frequency response

The basic two-stage CMOS op amp topology shown in Fig. 5a is essentially identical to its bipolar counterpart. As a consequence, the equivalent circuit of Fig. 6 can be used to represent the second stage with its compensation capacitance (Gray et al. 2000). At the frequency $|z|$ the gain characteristic of the amplifier flattens out because of the contribution to the gain of +6 dB/octave from the zero. As a consequence, the amplifier will have negative phase margin and be unstable when the influence of the next most dominant pole is felt. In effect, the zero halts the gain roll-off intended to stabilize the amplifier and simultaneously pushes the phase in the negative direction. Any feedback applied around the overall amplifier will then be positive instead of negative feedback, resulting in oscillation. At very high frequencies, C acts like a short circuit diode-connecting the second stage as shown is Fig. 7a, which then simply presents a resistive load of $1/g_m$ to the first stage, again showing the loss of 180° of phase shift. A way to deal with the right half-plane (RHP) zero is to insert a resistor in series with the compensation capacitor, as shown in Fig. 7b. Rather than eliminate the feedforward current, the resistor modifies this current and allows the zero to be moved to infinity. If the zero moves to infinity, the total forward current at the output node that is related to v_1 must go to zero when $\omega \to \infty$. When $\omega \to \infty$, capacitor C is a short circuit and therefore the feed forward current is only due to R_z. This zero moves to infinity when R_z equals $1/g_m$. Making the resistor greater than $1/g_m$ moves the zero into the left half-plane, which can be used to provide positive phase shift at high frequencies and improve the phase margin of a feedback circuit that uses this op amplifier.

3.2.3 Adaptive biasing

In order to improve the linearity of the preamplifier, we try to design a rail-to-rail amplifier that has large input swing range and higher SR. Figure 6a shows the basic topology of an NMOS symmetrical amplifier (Laker and Sansen 1994). Its voltage gain is gives as

$$A_r = B \frac{g_{m1}}{g_{ds6} + g_{ds7}}, \tag{12}$$

where

$$B = \frac{(W/L)_9}{(W/L)_3} = \frac{(W/L)_6}{(W/L)_4}. \tag{13}$$

The GBW value is given by

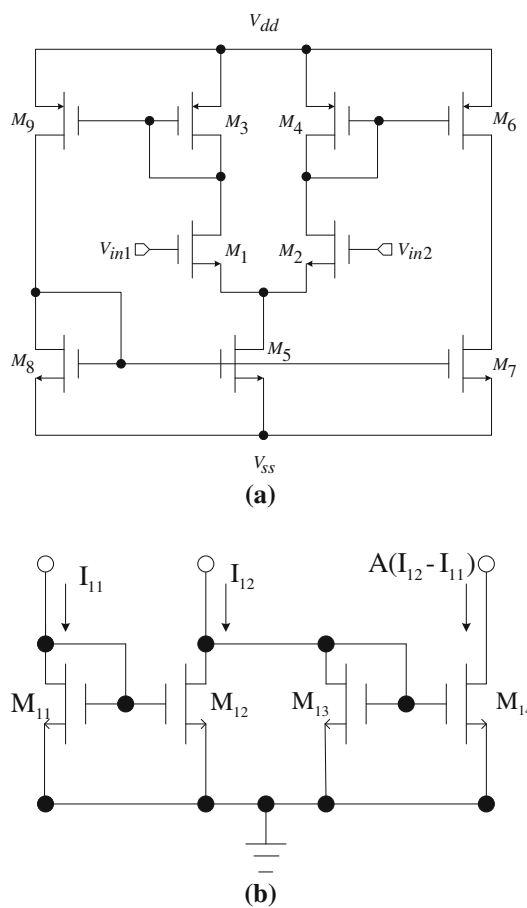$$GBW = B \frac{g_{m1}}{2\pi C_L}, \tag{14}$$

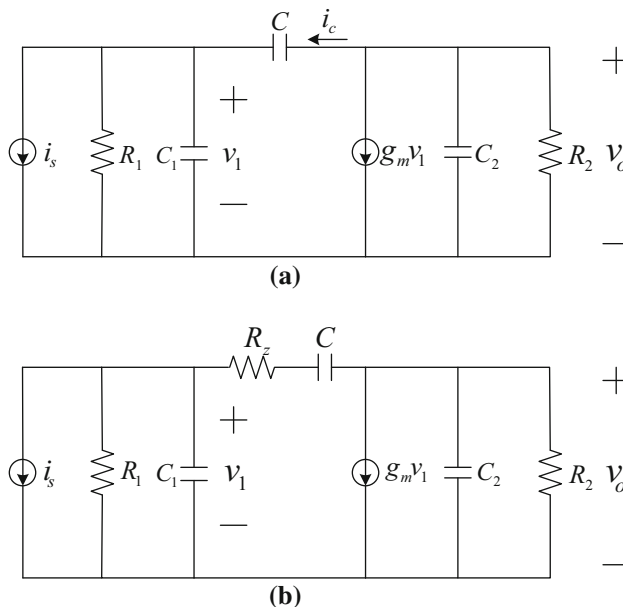Fig. 6 **a** NMOS symmetrical operational amplifier; **b** current subtractor

Fig. 7 **a** Feedback capacitor C includes compensation capacitance; **b** small-signal equivalent circuit of a compensation stage with resistor

where C_L is the load capacitance, while the SR is

$$SR = B\frac{I_5}{C_L}, \tag{15}$$

From above two equations, we can also deduce that

$$\frac{SR}{GBW} \propto \frac{I_5}{g_{m1}}. \tag{16}$$

In order to enhance SR without changing GBW, the biasing current must be increased with consequent power consumption enhancement. In this sense, the use of the adaptive biasing technique helps to reduce stand-by power dissipation without degrading the circuit dynamic performances.

The adaptive biasing technique adds current at the input stage only if a differential input is applied. Many adaptive biasing circuits have been proposed (Lin and Ismail 1998;
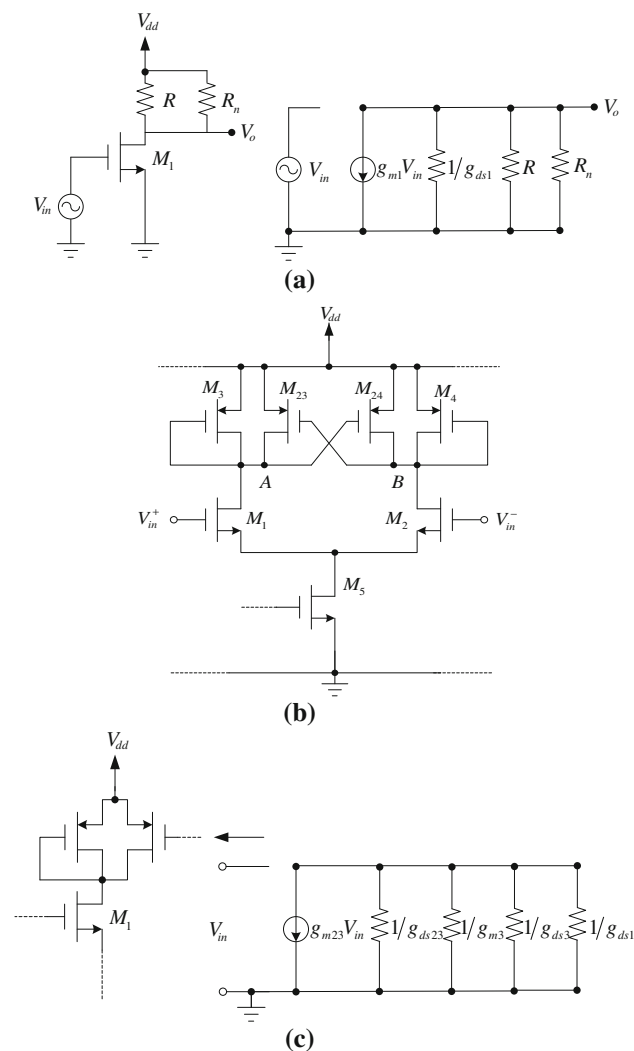

(a)

(b)

(c)

Fig. 8 a Gain enhancement circuit and the small-signal equivalent circuit; b negative compensated operational amplifier; c feedback branch structure

Ferri and Cardarilli 1998; Giustolisi et al. 2000; Cardarilli et al. 1998; Parzhuber and Steinhagen 1991; Degrauwe et al. 1982; Laker and Sansen 1994; Klinke et al. 1989; Sengupta 2005). One of the first and most diffused of them was presented in Klinke et al. (1989). It is based on the current subtract shown in Fig. 6b. In this work, it has been applied to a symmetrical amplifier (see Fig. 6a). The current given by the subtract is equal to

$$I_5 + A|I_{12} - I_{11}|, \tag{17}$$

where, considering Fig. 6b, the gain current A is given as

$$A = \frac{(W/L)_{14}}{(W/L)_{11,12,13}}. \tag{18}$$

By using the current formula for the weak inversion region proposed by Vittoz and Fellrath (1977) (Sengupta 2005) and by applying Kirchhoff's current law, Eqs. 19 and 20 can be derived. V_{in} is the voltage across the inputs of the amplifier ($V_{in} = V_{in2} - V_{in1}$).

$$I_{11} = I_{12} \cdot \exp\left(\frac{V_{in}}{nV_T}\right), \tag{19}$$

$$I_{12} = \frac{I_5}{(A+1) - (A-1) \cdot \exp(V_{in}/(nV_T))}. \tag{20}$$

The output current I_{out} and the bias current I_5 are related according to the following equation,

$$I_{out} = B(I_{11} - I_{12}) = \frac{BI_5\left(e^{V_{in}/nV_T} - 1\right)}{(1+A) - (A-1)e^{V_{in}/nV_T}}, \tag{21}$$

which is valid in the weak inversion region, and, in the case of unitary gain B between output mirrors. Since A is typically in the range between 0 and 0.9, the output maximum current is $I_5/(1-A)$. If $A = 0.9$, the output current and, consequently, SR increase by a factor of 10.

3.2.4 DC gain enhancement techniques

To increase the DC gain, the negative conductance technique has been utilized (Vittoz and Fellrath 1977). It is illustrated in the circuit diagram given in Fig. 8a. Placing a negative resistance R_{in} in parallel with the output resistance of the amplifier, the voltage gain is given as

$$A_V = \frac{V_o}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + (1/R) + (1/R_n)}. \tag{22}$$

The voltage gain is ideally infinite if the following relation is satisfied.

$$\frac{1}{R_n} = -\left[\left(\frac{1}{R}\right) + g_{ds1}\right]. \tag{23}$$

The above technique is better than others, such as cascade, because it is possible to obtain a DC gain
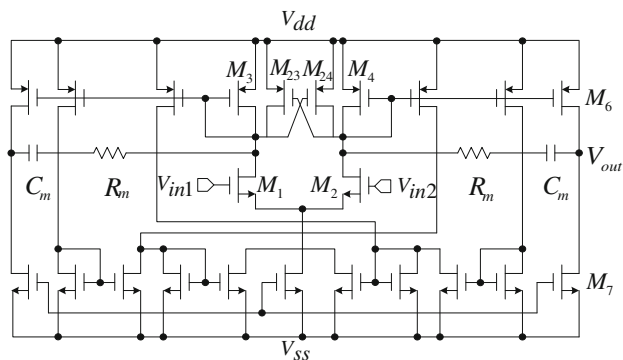
Fig. 9 NMOS amplifier structure

Table 1 Summary of parameters for frequency response of the NMOS amplifier

Parameters	R_i	R_u	C_u	C_m	C_i	R_m	R
Magnitude	1.6 MΩ	4.9 KΩ	0.77 fF	3 pF	0.81 fF	40 KΩ	5 KΩ

enhancement also for low-voltage applications. It can be applied to symmetrical operational amplifier according to the topology shown in Fig. 8b, where the gates of M_{23} and M_{24} are connected to the drain of M_3 and M_4. In this manner, at A and B nodes, a parallel resistance has been added. Transistors M_1, M_2, and M_{23}, M_{24} constitute a positive feedback loop, where the direct path is characterized by A_d voltage gain and the feedback loop, formed by M_{23}, M_1, and M_3, has a gain equal to β. The overall gain is given by

$$A = \frac{A_d}{1 - A_d \beta} = \frac{A_d}{1 - G_{loop}}, \tag{24}$$

where G_{loop} is the loop gain equal to $A_d \beta$. The gain A_d is given as

$$A_d = \frac{g_{ml}}{g_{m3} + g_{ds23} + g_{ds3} + g_{ds1}}. \tag{25}$$

To calculate the loop gain G_{loop} the input voltage has to be grounded, and a signal has to be forced in an arbitrary
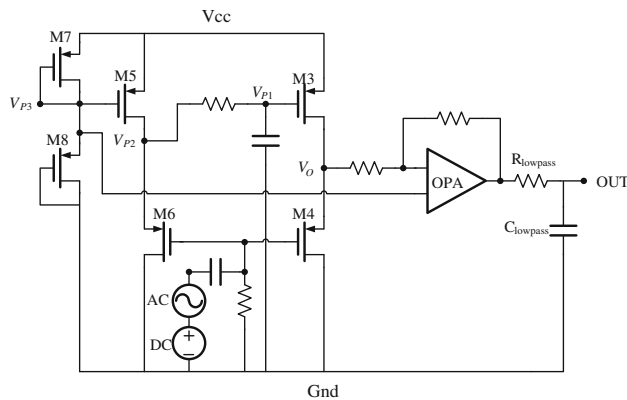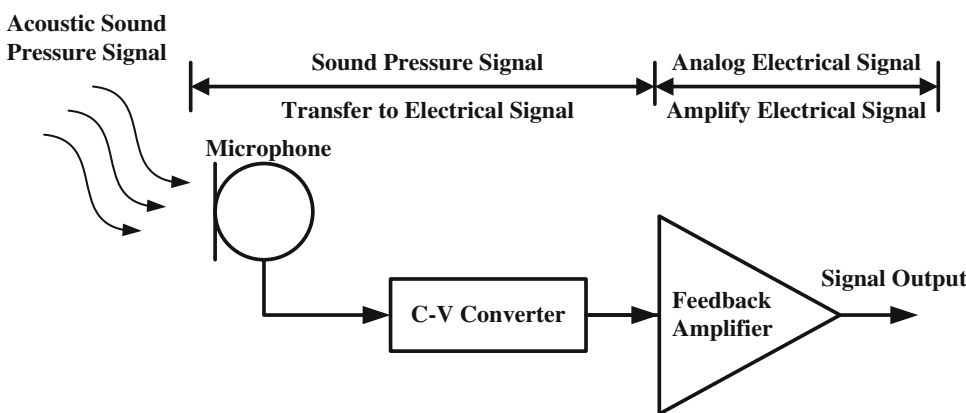
node inside the same loop. The G_{loop} is the ratio between the signal processed by the loop and the forced signal. Figure 8c shows the feedback branch structure. From the small-signal analysis we can write

$$G_{loop} = \frac{V_{out}}{V_{in}} = \frac{g_{m23}}{g_{m3} + g_{ds23} + g_{ds3} + g_{ds1}}. \tag{26}$$

Stability is ensured if G_{loop} lower than 1. From Eq. 26, this is easily obtained if g_{m3} is closed to g_{m23}. In this case, since the overall gain A can be expressed as

$$A = \frac{g_{m1}}{g_{m3} - g_{m23} + g_{ds23} + g_{ds3} + g_{ds1}} \approx \frac{g_{m1}}{g_{m3} - g_{m23}}, \tag{27}$$

A condition on g_{m3} and g_{m23} values can be deduced. In particular, to avoid gain A becoming infinite or changing its sign, the value of g_{m3} has been set to be lower than 94 % of the g_{m23} value.

3.2.5 NMOS amplifier stability

The NMOS amplifier is shown in Fig. 9 (Razavi 2001; Hui 2007; Gray et al. 2000). In this case, we have not applied a classical Miller compensation because the right half plane
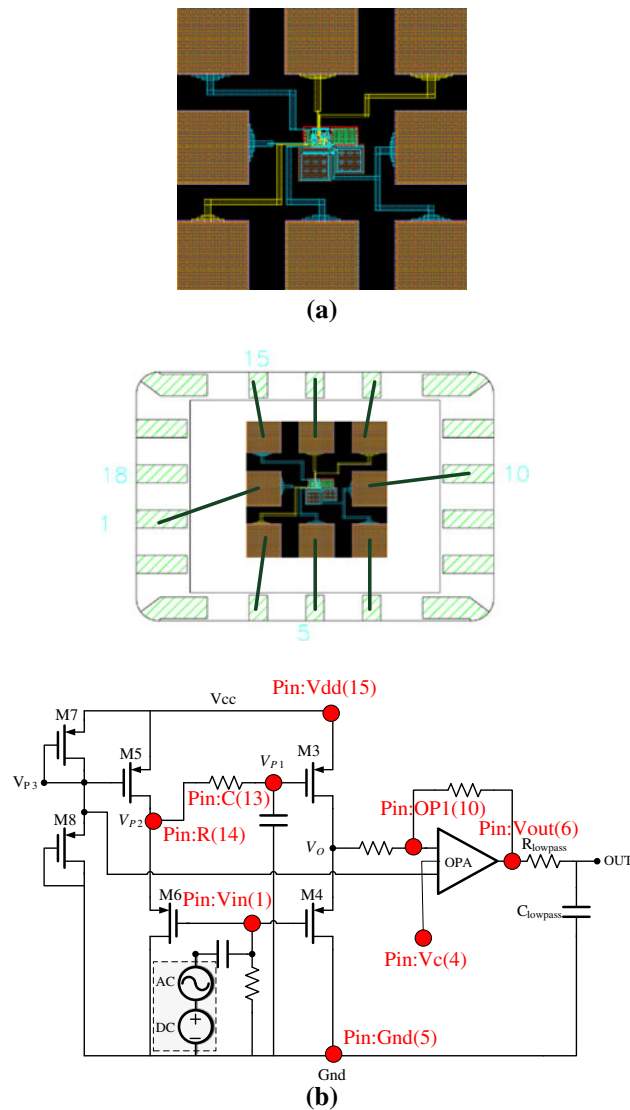

Fig. 11 The entire readout circuit

Fig. 10 Microphone front-end system topology

$$f_{p1} = \frac{1}{2\pi g_{m6} R_i R_u C_m}, \tag{28}$$

where R_i is the output resistance of the differential stage, R_u is that at the amplifier output and R is the load resistance:

$$R_i = \frac{1}{g_{m3} - g_{m23} + g_{ds3} + g_{ds23} + g_{ds1}}, \tag{29}$$

$$R_u = \frac{1}{g_{ds5} + g_{ds6} + 1/R}. \tag{30}$$

First, the non-dominant pole is given by

$$f_{p2} = \frac{g_{m6} C_m}{2\pi [C_i C_u + (C_i + C_u) C_m]} \approx \frac{g_{m6}}{2\pi C_u}, \tag{31}$$

where C_i and C_u are the first- and second-stage output capacitances. Zero occurs at the following frequency:

$$f_z = \frac{g_{m6}}{2\pi C_m (R_m - \frac{1}{g_{m6}})}. \tag{32}$$

Table 1 gives the parameters that improve the frequency response of the NMOS amplifier. It can improve the phase margin and the bandwidth. From Eqs. 30 to 32, decreasing C_m and R_m would increase the bandwidth. Making $R_m = \frac{1}{g_{m6}}$ can be used to provide positive phase shift at high frequencies and improve the phase margin of a feedback circuit that uses this operational amplifier.

3.3 The Entire readout circuit

The designed readout circuit consists of two main sub-circuits, responsible for the functions in two different stages as shown in Fig. 10. One is a self-bias circuit for the centered output of the capacitance-to-voltage converter at the first stage, while the other is the operational amplifier that is used by the two-stage amplifier and the rail-to-rail operational amplifier at the two-stages. The input stage is designed the high pass filter with $R_{highpass} = 10\ k\Omega$; $C_{highpass} = 20\ \mu F$. These are designed to limit the low frequency at 20 Hz and isolate DC part from the microphone. The output stage is designed for a low pass filter with $R_{lowpass} = 544.429\ k\Omega$; $C_{lowpass} = 14.617\ \mu F$ that is

Fig. 12 a The layout figure of the chip; b the pin pads of the chip

zero has not been nullified; rather, it has been designed at a frequency close to that related to the non-dominant pole to benefit from the lead effect. The choice of $C_m = 3\ pF$ and $R_m = 40\ k\Omega$ allows us to have a zero with a negative real part, and this partially compensates the non-dominant pole effects on the module and phase response. The dominant pole at frequency

Table 2 The parameter of the two-stage amplifier

MOS	N-M$_1$	N-M$_2$	P-M$_3$	P-M$_4$	N-M$_5$	P-M$_6$	N-M$_7$	N-M$_8$
Region	Sat	Sat	Sat	Sat	Sat	Sat	Sat	Sat
W/L	0.7/0.35	0.7/0.35	0.7/0.35	0.7/0.35	1/0.35	1.4/0.35	1/0.35	1/0.35
V_{ds}	1.24	1.24	−880 m	−880 m	881 m	−1.5046	1.4954	650 m
V_{th}	0.568	0.568	−0.729	−0.729	0.563	−0.704	0.558	0.564
g_m	24.3 u	24.3 u	13.6 u	13.6 u	43.8 u	28.4 u	48.5 u	41.9 u

Fig. 13 a The frequency response of the two-stage amplifier; **b** the frequency response of the rail-to-rail amplifier
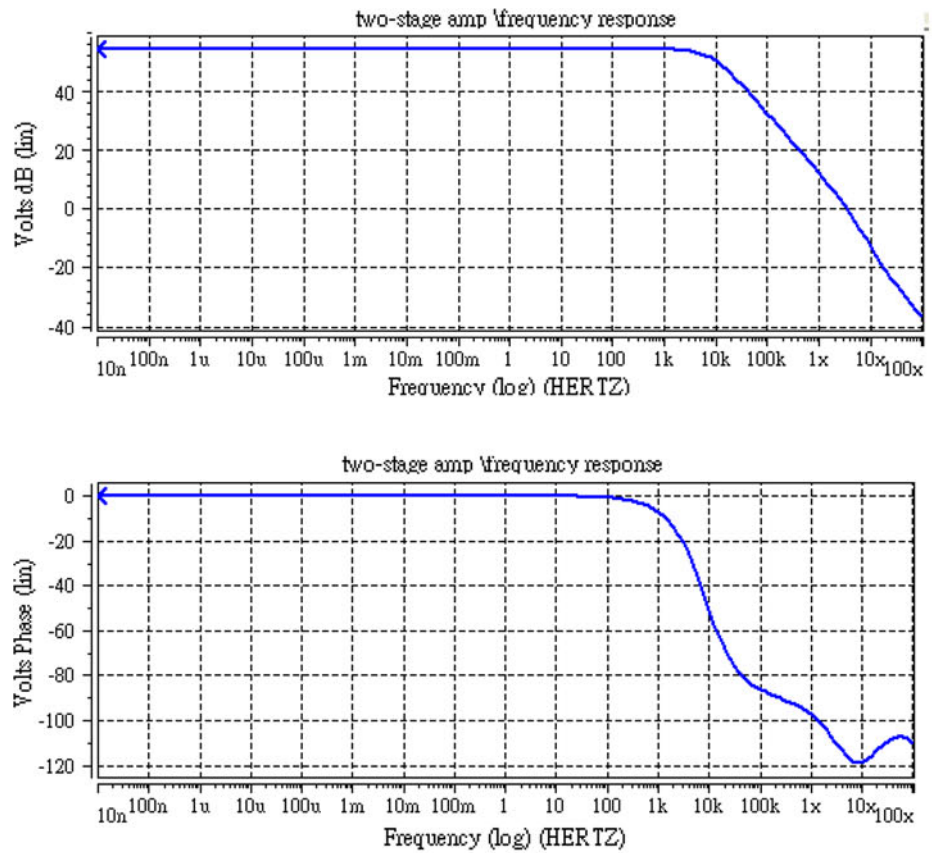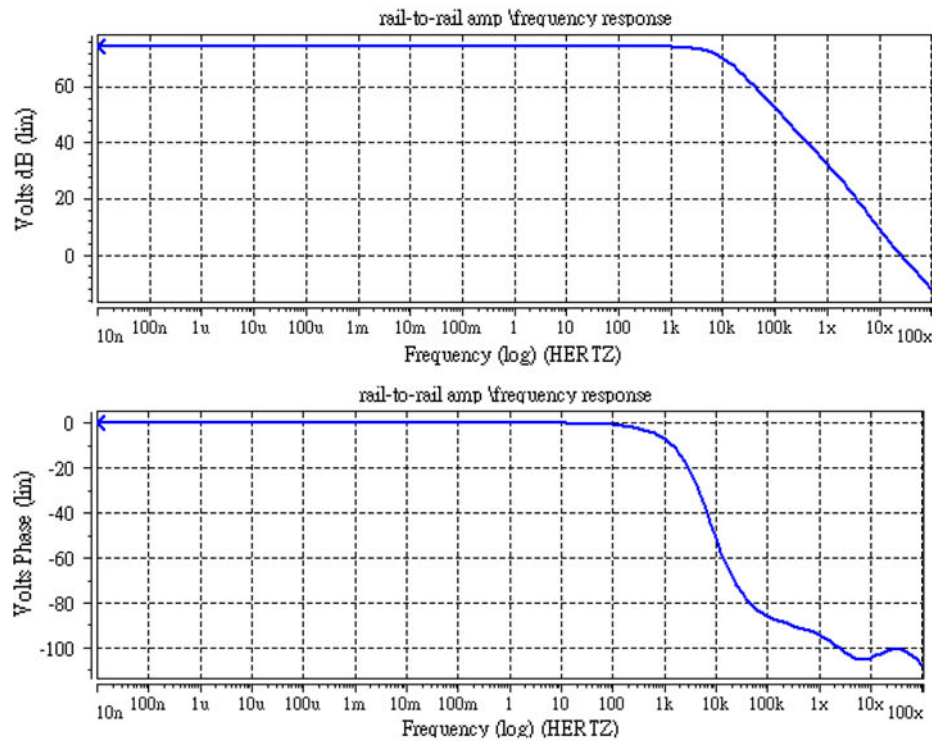
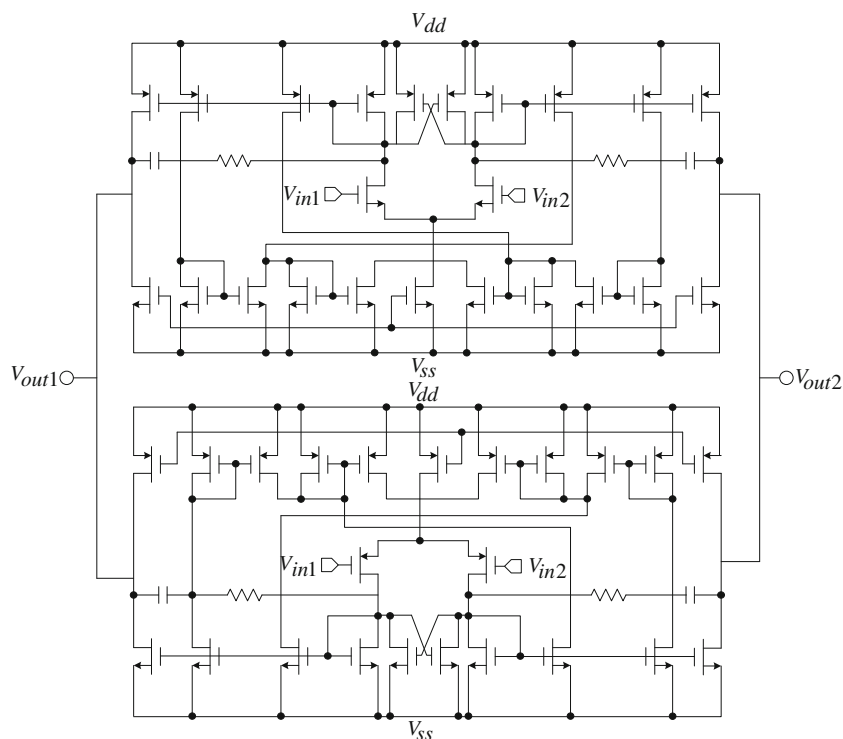**Fig. 14** Rail-to-rail configuration of the designed amplifier

Table 3 Main transistor W/L, transconductances and output conductances

| MOS	W/L	g_m	g_{ds}
M_1	0.7/0.35	1.53×10^{-4}	1.93×10^{-6}
M_3	0.7/0.35	4.2×10^{-5}	1.1×10^{-6}
M_{23}	0.775/0.35	4.56×10^{-5}	1.18×10^{-6}
M_6	1.5/0.35	10.3×10^{-5}	3.1×10^{-6}
M_7	1.5/0.35	1.58×10^{-4}	1.79×10^{-6}

design to limit the high frequency at 20k Hz and eliminate noise. The rage of bandwidth that is limited by additional-designed low pass filter and high pass filter, which limited the response from 20 to 20k Hz, in order to reduce high-frequency noise and eliminating DC component (Nakamura et al. 2012). The readout circuit designed to operate capacitor-type microphone is in principle a buffering circuit, which acting as a transimpedance to converter the very high output impedance. However, the output signal of a capacitance-to-voltage converter is normally very small and it may cause too much noise for following applications. Therefore, a preamplifier is designed and applied to amplify the signal to an acceptable prospect for the convenience of proceeding signal processing. The entire readout circuit is shown in Fig. 11. The proposed circuit is next implemented by using the TSMC

0.35 μm Mixed-Signal MODE (2P4M, 3.3 V/5 V) POLYCIDE technology. The supply voltage is fixed at low voltage (3 V), power dissipation is only 200 μW. The chip area is 0.4 mm × 0.4 mm as shown in Fig. 12a. It has eight pin pads that include of the supply voltage (3 V), the supply voltage (0.65 V), the ground, the input, the output, and the low pass filter of the pin pads shown in Fig. 12b.

4 Simulation and experimental results

Simulations on the entire readout circuit are conducted. The parameters of the two-stage amplifier are shown in Table 2. Its dc gain is 54 dB and the unit-gain-bandwidth is 3.375×10^6. The gain margin is 3.475×10^6 and the phase margin is 68.56°. The frequency response of the two-stage amplifier and the rail-to-rail amplifier are shown in Fig. 13a, b. The rail-to-rail amplifier increases the dc gain from 54 to 74 dB and invariant with the phase. The power dissipation of the amplifier is 19.418 μW. The low-voltage low-power rail-to-rail amplifier is shown in Fig. 14. The main transistor transconductance and output conductance are shown in Table 3. The phase margin is 74, but stability is always ensured by also considering temperature and technological parameter variations. The entire readout circuit that includes the self-bias circuit for the central output of the capacitance-to-voltage converter and amplifier

Fig. 15 a SR behavior with
two-stage amplifier and **b** SR
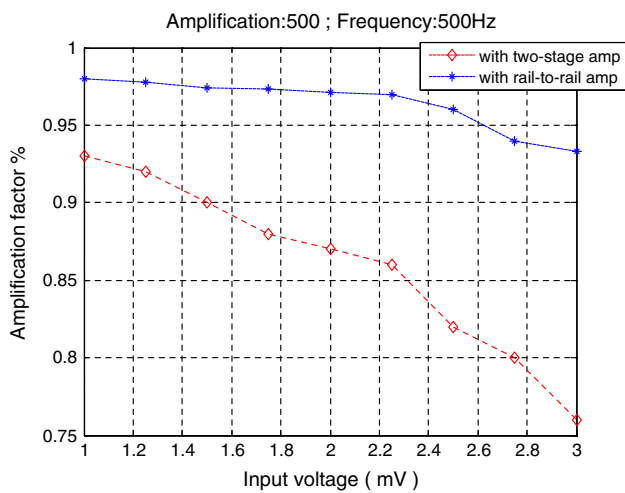behavior with rail-to-rail
amplifier
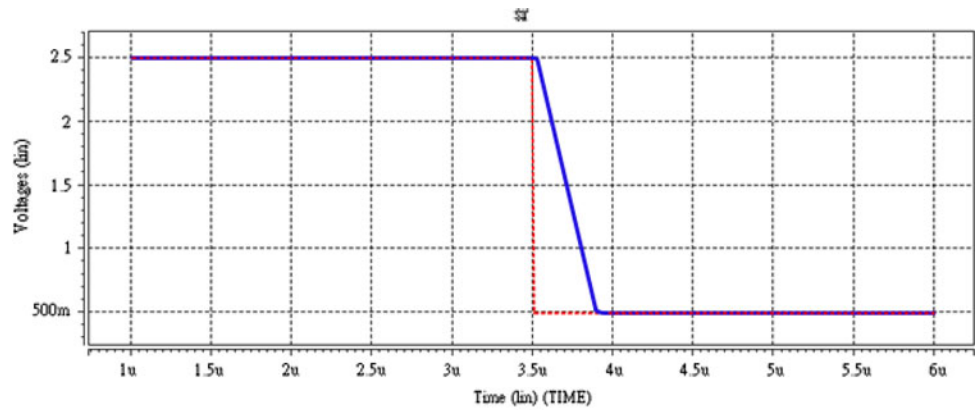
(a)
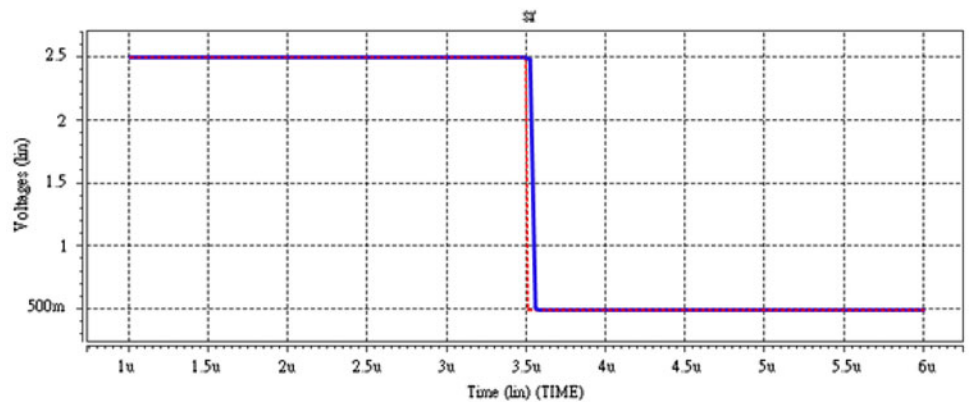
(b)

Fig. 16 The amplification factor of the amplification at 500 and the
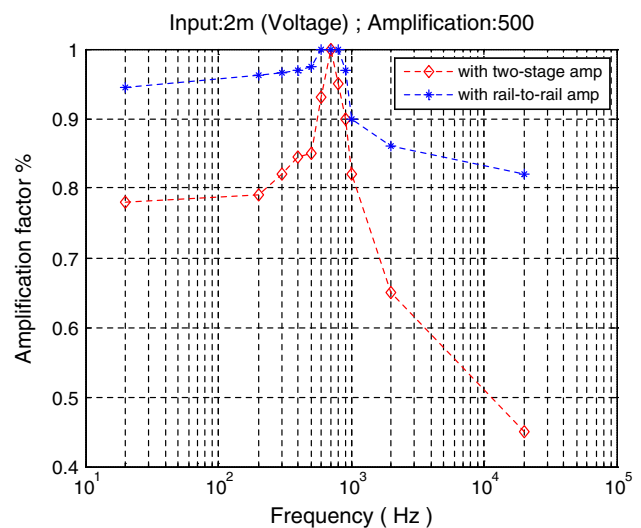frequency at 500 Hz

Fig. 17 The amplification factor of the preamplifier is at the same
input voltage and amplification and different frequency

that is used by the two-stage and rail-to-rail amplifier simulate. The output signal is checked when the input signals that has different voltage and frequency. The bandwidth that uses the high pass filter and low pass filter is limited between in 20 and 20k Hz. The output signal will distort

when the frequency of the input signal is over 20k Hz or low 20 Hz. Figure 15 reports the simulated transient response to a square input, showing SR performance between the two-stage amplifier and the rail-to-rail low-

Table 4 The specifications of the operational amplifier

Parameters	Two-stage OP	NMOS symmetrical OP	PMOS symmetrical OP	Rail-to-rail simulated
Static power dissipation (μW)	19	85	82	166
DC-gain (dB)	54	77	80	75
GBW (MHz)	3.43	4.7	6.8	9.2
Phase-margin	68.56°	74°	78°	79°
SR (V/us)	5	18	25	40
CMRR (dB)	120	142	135	132
$PSRR^+$ (dB)	560	107	114	140
$PSRR^-$ (dB)	560	114	109	145
Settling time (ns)	450	390	410	310
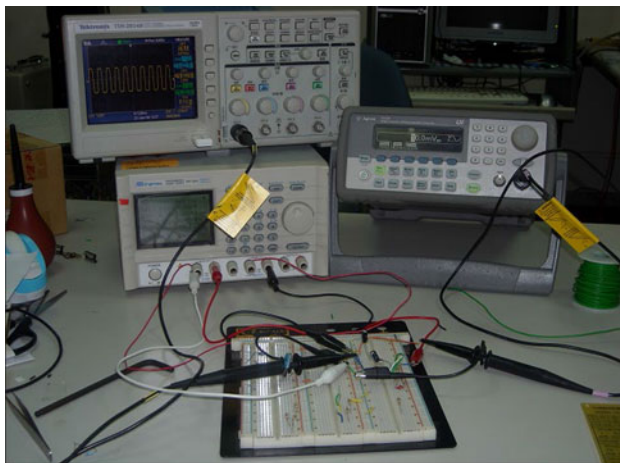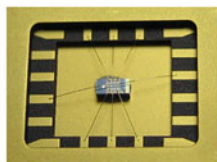
Fig. 18 **a** The apparatus of the measurement system; **b** the picture of the IC

voltage low-power amplifier. The simulated transient response of the two-stage amplifier is delay 0.4 μs and the rail to rail amplifier is delay less than 0.1 μs in the same condition. The preamplifier that used with the amplifier that includes the two-stage and rail-to-rail amplifiers is at the same amplification and frequency, as shown in Fig. 16. The input signal of microphone is ranging from 1 to 3 mV and most of amplification factor of the two-stage amplifier are <90 % in this region. In contrast to the two-stage amplifier, the amplification factors of rail-to-rail amplifier are more than 90 %. Human can sensing the signal from 20 to 20k Hz. Figure 17 is the amplification factor of the pre-amplifier that includes the two-stage and the rail-to-rail

amplifier at the same input signal with the different frequency which is from 20 to 20k Hz. The rail-to-rail amplifier that operates with the adaptive biasing allows an increase in the SR value by a factor of about 35. We use an adaptive-biased low-voltage low-power rail-to-rail amplifier with enhanced DC-gain. Based on simulation, the proposed circuit, fabricated in its rail-to-rail version, was confirmed to show the well performance results. Therefore, it is good for using, for example, in capacitor-type microphone, where power dissipation is a fundamental requirement to maintain the life of batteries. Moreover, due to high SR and low settling time values, this solution is also suitable for those applications that require high speed and precision. Table 4 shows the power dissipation for the two-stage amplifier and rail-to-rail amplifier and others. Comparing the four systems, the two-stage amplifier has the least static power dissipation but its performance in the DC-gain and SR is not good. The rail-to-rail amplifier has well performance in DC-gain and SR. For improving the SR, it integrates one NMOS OP and one PMOS OP and it needs more power. Although the static power dissipation of rail-to-rail amplifier is 166 μW but it is in the allowance region of microphone system.

The 0.35 μm 2P4M (two-poly-two-metal) CMOS TSMC process is employed to fabricate the chip which is for validating the aforementioned amplifies. The designed integrate circuit layout is followed by National Chip Implementation Center (CIC) of Taiwan, and also fabricated by this center. To verify the performance of the realized IC, two experiments are conducted. One is changing the amplitude of the sinusoid signal and using a testing capacitance. In this way we can only change the amplitude and the frequency by the function generator. The other way is using traditional capacitive-type microphone to receive the sound of the cell phone. Figure 18 is shows the measure of the system and the chip. The bandwidth of the sound that is limited between 20 and 20k Hz by high pass filter of the input stage and low pass filter of the output stage is hearing by human. The input
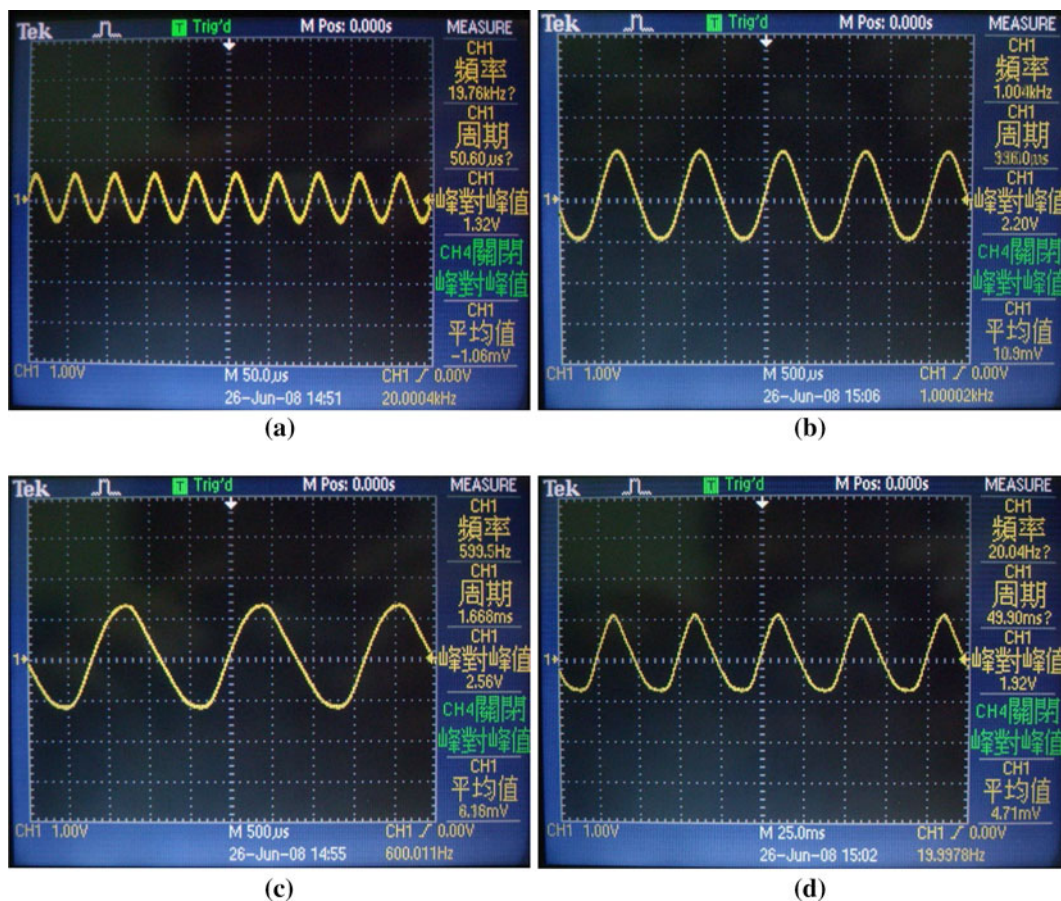
Fig. 19 The microphone output signal through to the rail to rail preamplifier on difference frequencies **a** on 20k Hz; **b** on 1k Hz; **c** on 600 Hz; **d** on 20 Hz

stage with the of capacitance and the 20 μF and 10 kΩ of resistance takes as the high pass filter. The 5 pF of testing capacitance is in front of the input signal that generated by the function generator. Figure 19a–d are shown the measure result of the output signal that between the 20 and 20k Hz of the frequency. It is difficult to sense the sound of the traditional microphone because the magnitude of the cell phone needs to control the distance between the traditional microphones. Figure 20a is shown the signal (1 kHz) that is detected by the preamplifier connected to the traditional microphone. Figure 20b is shown the signal of the music of the cell phone that is detected by the preamplifier connected to the traditional microphone. Figure 21 is shown the simulation and experiment results. The voltage gain error of the experiment is obtained by the measured results. The measured results are obtained by function generator that brings the peak to peak amplitude of the sine wave. The results are different between the simulation and experimentation as a result of the variation of the manufacture. The result of the variation of the manufacture causes DC part of the output that shifts in non-midway of supply voltages. Therefore, this is main

reason that causes the different between the simulation and experiment results.

5 Conclusion

A low-power low-voltage capacitive-type microphone preamplifier is proposed in this study. The chip of the preamplifier that includes a new self-bias circuit for centering dc level of the capacitance-to-voltage converter and the two-stage amplifier is realized by TSMC 0.35 μm Mixed-Signal MODE (2P4M, 3.3 V/5 V) POLYCIDE technology. Several analysis techniques are also applied to improve the performances of the preamplifier, such as DC gain enhancement, stability analysis and frequency compensation, etc. The capacitive-type microphone preamplifier in this study is low-power, low noise, and small area. The capacitive-type microphone preamplifier is different from the others that always have analog-to-digital converter and digital-to-analog converter with more noise and power dissipation. Followings are the concluding remarks of this study.
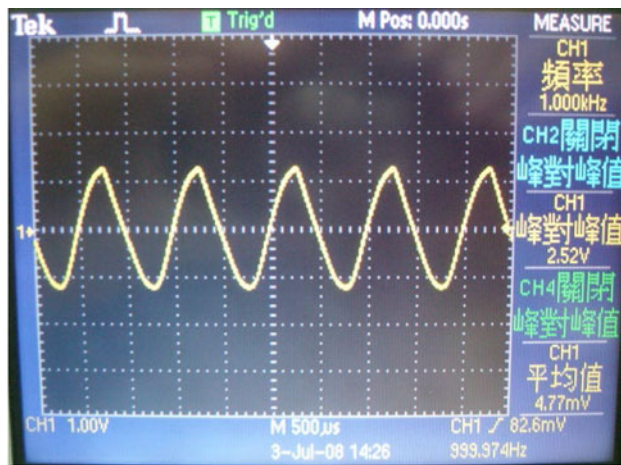
(a)
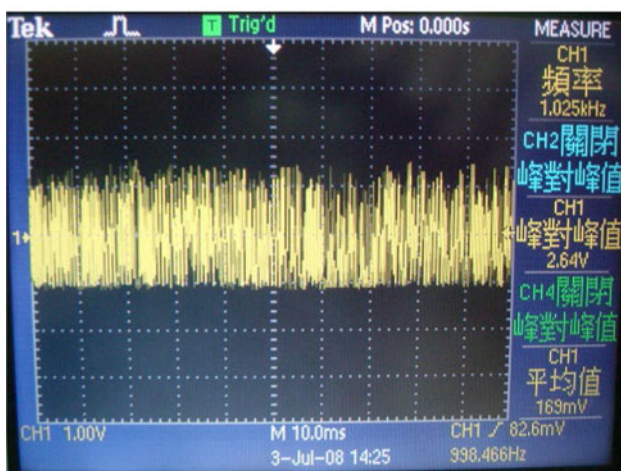
(b)

Fig. 20 **a** The output signal with the mono signal at 1k Hz; **b** the output signal with the song signal generated by the cell phone

(1) This study proposed low power dissipation, which is about 210 μW, while 3 V supply voltage is applied with 1 μF of the output load capacitance. The minimum input signal of the function generator is 10 mV. The measure with the function generator is used to decrease the amplification avoiding over output swing range. The output swing range that is not an expected value of the preamplifier is limited at 2.56 V, and therefore a rail-to-rail amp. Our team would to realize the preamplifier with rail-to-rail amplifier is designed for improving the output performance.

(2) The proposed rail-to-rail amplifier raises the DC gain to 78 dB which compared with 58 dB from the two-stage amplifier, while the phase margin is in the similar level. Based on the simulation results, the rail-to-rail amplifier owns the better performance on the amplification factor with higher input signal voltage.
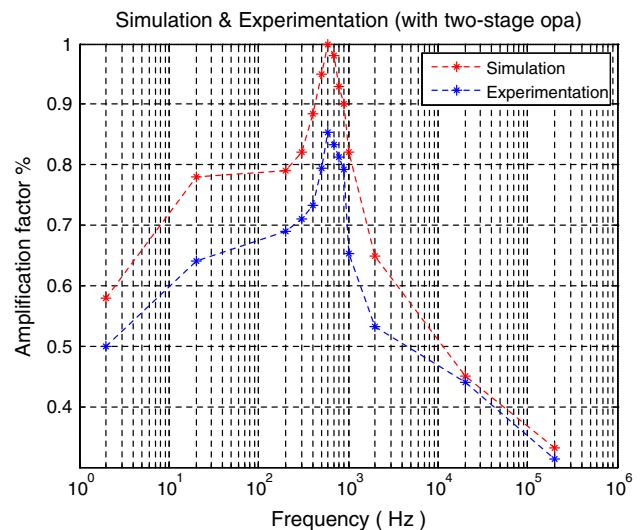

Fig. 21 Simulation and experimentation results with two-stage operator

Moreover, the simulation also validates the performance of rail-to-rail amplifier has better SR.

(3) This realized integrate circuit shows the satisfactory performance in the experiment. The frequency response from the experiment is similar to the simulation results, and could be improved by considering detailed process parameters.

(4) In this study, PSRP and the CMRP are not measured yet and will be the future works for evaluating the performance of designed amplifier.

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