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Fast Transient Low-Dropout Voltage Regulator With Hybrid Dynamic Biasing Technique for SoC Application

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***Abstract*— This brief presents a low-dropout (LDO) voltage regulator without output capacitors that achieves fast transient responses by hybrid dynamic biasing. The hybrid dynamic biasing in the proposed transient improvement circuit is activated through capacitive coupling. The proposed circuit senses the LDO regulator output change so as to increase the bias current instantly. The proposed circuit was applied to an LDO regulator without output capacitors implemented in standard 0.35-μm CMOS technology. The device consumes only 25 μA of quiescent current with a dropout voltage of 180 mV. The proposed circuit reduces the output voltage spike of the LDO regulator to 80 mV when the output current is changed from 0 to 100 mA. The output voltage spike is reduced to 20 mV when the supply voltage varies between 1.3 and 2.3 V with a load current of 100 mA.**

***Index Terms*— Capacitive coupling, hybrid dynamic biasing, low-dropout regulator, transient response, voltage spike.**

I. Introduction

Nowadays, on-chip power management units have been extensively developed, implying there are multiple power domains in the system-on-chip (SoC) design. The power management system scales down the supply voltage by low-dropout (LDO) to power many circuit blocks. Transient response time is an important dynamic specification in LDO designs because the voltage spike affects the overall performance. For the LDO loop bandwidth, it is necessary to control the locations of the loop's poles and zeros in small-signal analysis [1]–[3]. Increasing the loop bandwidth can improve small-signal performance at low and moderate frequencies. If the design focuses on the large-signal behavior, typical approaches are to increase the bias current to achieve a high slew rate, or to use large capacitors to reduce the undershoot and overshoot of the output voltage ($V_{\rm OUT}$) [4], [5]. In SoC applications [6]–[9], to reduce the undershoot or overshoot of the output voltage, the use of a large output capacitor will require an extra pin, which is therefore not preferred. To effectively increase the slew rate instantly seems to be a better approach to cope with output voltage spikes.

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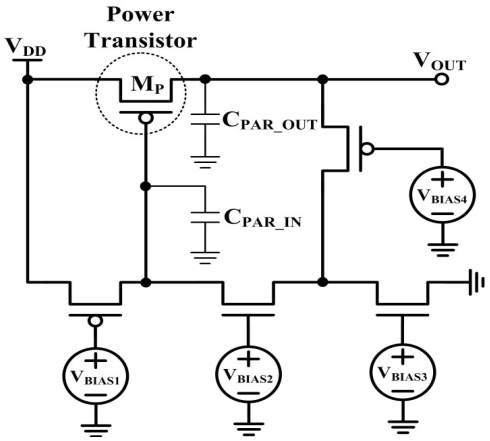

Fig. 1. LDO structure without output capacitors.

There are many ways to solve the voltage spike problem. One method is to use a constant bias current to increase the slew rate, where the bias current is not dependent on the output current. Besides, a previous design incorporates a 600-pF on-chip capacitor to reduce the output voltage ripple [10]. This method does not meet the power-saving and area-limited requirements of SoC designs.

The other method is the push–pull biasing method [11]. More bias current will be used at the transient instant only if the output current changes. The error amplifier uses a push–pull output stage to increase the current for charging and discharging the gate capacitance of the power transistor ($C_{\rm PAR\_IN}$) during the transient instant. A differential-input common-gate amplifier activates the push–pull output stage. However, the fast-changing voltage spike cannot be detected effectively because the differential common-gate amplifier has limited bandwidth. This approach is also not suitable for low output voltages.

Another method is to raise the bias current based on the significance of the output current [12], [13]. For circuits to react to a change in the output voltage quickly, an adaptive bias current should maintain a minimum value in the steady state.

In this brief, an LDO with hybrid dynamic biasing is proposed to improve the output voltage transient speed under abrupt changes of the output current. Through capacitive coupling, the fast transient circuit senses transient changes in voltage at the LDO output and instantly increases the bias current. The quiescent current is only 25 μA.

The rest of this brief is organized as follows. Section II presents the LDO architecture and operation principle of the proposed fast transient circuit through hybrid dynamic biasing. Section III shows experimental results. The final section addresses the conclusion of this brief.

II. LDO Architecture

A. LDO Architecture Without the Output Capacitor

Fig. 1 shows an LDO structure without the output capacitor [10]. Fig. 2 illustrates the large-signal responses of this structure. In Fig. 2(a), when the output voltage ($V_{\rm OUT}$) suddenly drops, it instantly decreases the $V_{\rm SG}$ of transistor M_1 and turns it off. To provide the same bias current ($I_{\rm BIAS}$), $C_{\rm PAR\_IN}$ itself releases the current. In this

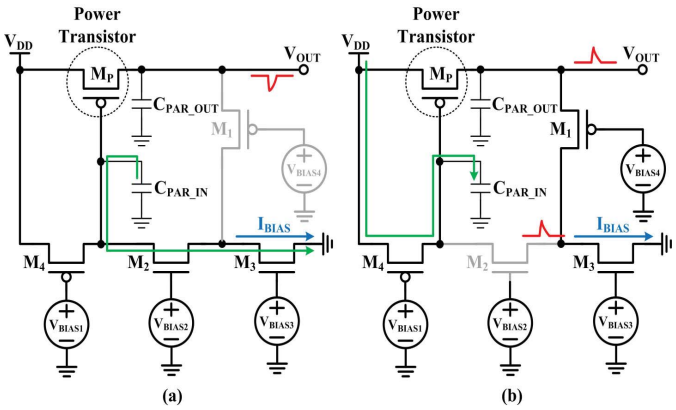

Fig. 2. Large-signal responses of the LDO structure without an output capacitor. (a) Undershoot. (b) Overshoot.

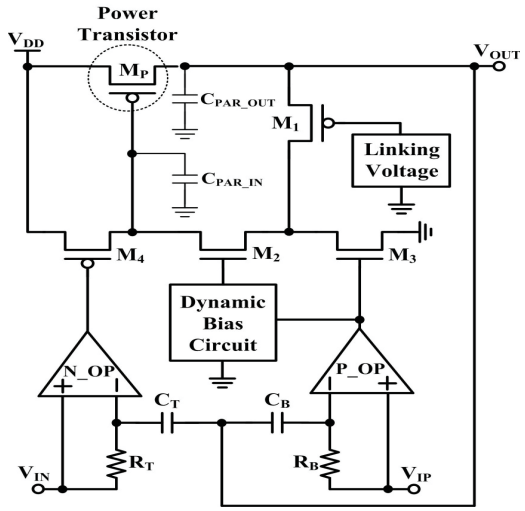

Fig. 3. LDO structure with the proposed fast transient circuit through hybrid dynamic biasing.

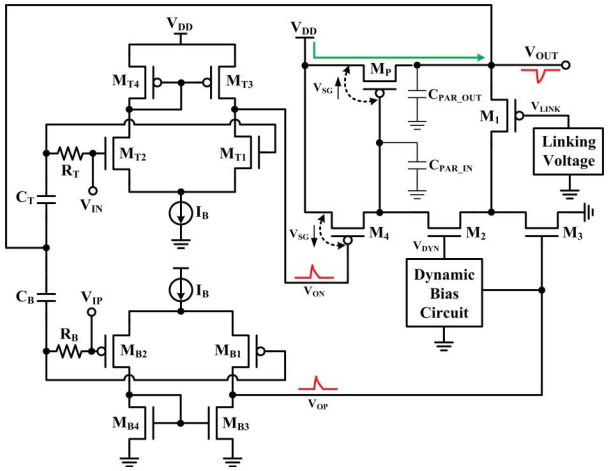

Fig. 4. Operation of the proposed circuit (undershoot).

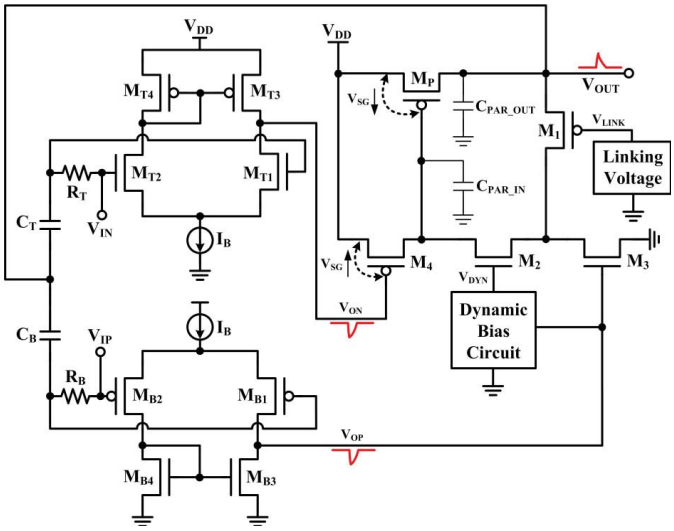

Fig. 5. Operation of the proposed circuit (overshoot).

way, the current flowing through transistor MP increases when the V_{SG} of transistor MP increases. This current pulls V_{OUT} back to the original voltage. Fig. 2(b) shows that, when V_{OUT} rises suddenly, it increases the drain voltage of transistor M_1 and the source voltage of transistor M_2. Thus, a decrease in the V_{GS} of transistor M_2 turns off transistor M_2. As a result, all current flowing through transistor M_4 is charged to C_{PAR_IN}. This phenomenon increases the gate voltage of transistor MP and decreases the V_{SG} of transistor MP. This effectively reduces the current through the transistor MP. To maintain the same I_{BIAS}, V_{OUT} is pulled down to keep the same I_{BIAS} current, thereby returning to the original voltage. The power transistor has a large size and generates a large parasitic gate capacitance. Owing to the large parasitic capacitance and the high impedance at this node, the gate of the power transistor forms a dominant pole. The other nodes are all of low impedance. Therefore, in the negative feedback loop, there only appears one pole within loop bandwidth, so the LDO does not require an output capacitor, which is therefore suitable for SoC applications.

B. Structure and Operation Principles of the Proposed Fast Transient Circuit

Fig. 3 illustrates the proposed architecture. The most critical feature of the structure is the dynamic enhancement of the slew rate. When the output voltage changes dramatically, the bias current immediately changes to improve the slew rate and reduce the LDO undershoot and overshoot. Figs. 4 and 5 analyze the large-signal performance of undershoot and overshoot, respectively. The voltage gain of the two op amps is $A_v = -g_{m1}(r_{o1}//r_{o3})$. The gain of the proposed circuit is larger than that of the circuit in [8], enabling it to amplify the detected transient signals more efficiently to enhance the transient driving capabilities and slew rates of transistors M_4 and M_3. Thus, the gate charge of power transistor M_P can be promptly sourced or sunk, i.e., the power transistor can respond efficiently. Each op amp consumes only 3.5 μA.

In addition to the capacitive coupling circuit, we also propose a dynamic bias circuit. The dynamic bias circuit can speed up the discharge of transistor M_2 according to the transient output of the capacitive coupling circuit, thereby reducing the response time of the power transistor. In contrast, the circuit in [8] uses a fixed bias voltage, which limits the response time of the power transistor, resulting in a larger variation of the output voltage unless a larger bias current has been used. The inclusion of the dynamic bias circuit enables the power transistor to respond quickly to an abrupt increase in load, thereby reducing the variation of the output voltage and expediting the recovery of output voltage. The detailed operation of the dynamic bias circuit is given in Section II-D.

Fig. 4 shows that, when V_{OUT} suddenly drops, the capacitive coupling of V_{OUT} causes the gate voltage of transistors M_{B1} and M_{T1} to drop. This, in turn, increases the output voltage of two differential amplifiers, decreasing the V_{SG} of transistor M_4 and

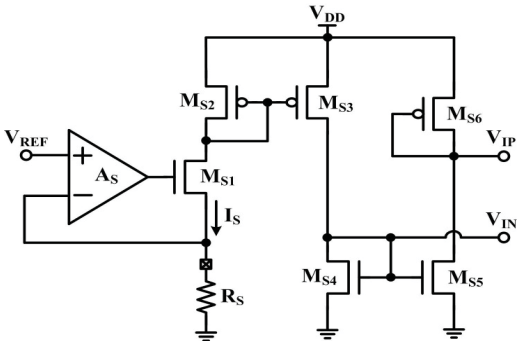

Fig. 6. Bias generation circuit.

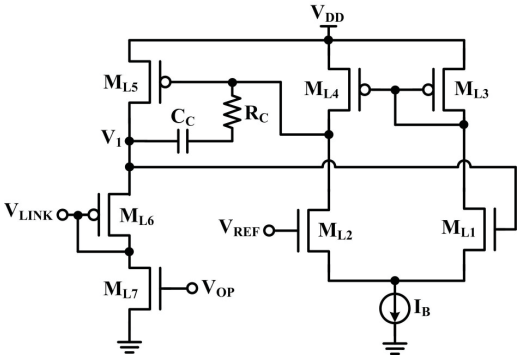

Fig. 7. Linking voltage generation circuit.

increasing the V_{GS} of transistor M_3. The current flowing through transistor M_3 becomes higher. As the V_{SG} of transistor M_4 decreases, the current flowing through transistor M_4 decreases. This instantly removes current from C_{PAR_IN}, causing the gate voltage of transistor M_P to drop quickly. When the V_{SG} of transistor M_P increases, it increases the current flowing through transistor M_P. This, in turn, charges the output parasitic capacitance (C_{PAR_OUT}) and pulls V_{OUT} back to the original steady state. In Fig. 5, when V_{OUT} suddenly rises, the capacitive coupling of V_{OUT} causes the gate voltage of transistors M_{B1} and M_{T1} to rise. This decreases the output voltage of two differential amplifiers, increasing the V_{SG} of transistor M_4 and decreasing the V_{GS} of transistor M_3. In this case, the current flowing through transistor M_3 decreases, and the current flowing through transistor M_4 increases. Thus, some current flowing through transistor M_4 charges C_{PAR_IN}, which increases the gate voltage of transistor MP. In this way, the V_{SG} of transistor MP decreases, which decreases the current flowing through transistor MP. Thus, C_{PAR_OUT} discharges, making V_{OUT} to pull down and return to the original steady voltage. In order to reduce the overshoot, increasing the gate voltage of the power transistor M_P is more effective than discharging LDO output by transistor M_1.

The bias generation circuit for V_{IP} and V_{IN} of Figs. 4 and 5 is shown in Fig. 6. The op amps in the proposed LDO regulator require additional bias voltages (V_{IP} and V_{IN}), while the circuit of [8] also requires two additional bias voltages.

C. Proposed Linking Voltage Generation Circuit (LVGC)

Fig. 7 shows that V_{REF} locking V_1 makes $V_1 = V_{REF}$ by connecting op amp in the unity-gain feedback configuration. The op amp provides one stage of high gain and one stage of low gain. The closed-loop gain is $A_f \approx g_{mL1}(r_{oL4}//r_{oL2})(2g_{mL5}/g_{mL6}) =$ 46 dB. The gain, which is larger than that of [8], is sufficient to force V_1 to nearly equal V_{REF}. The LVGC is designed to make the currents flowing through transistor M_{L6} and M_1 to be the same. The size of transistor M_{L6} equals the size of transistor M_1,

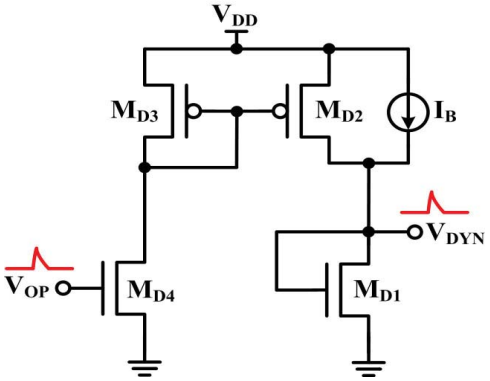

Fig. 8. Dynamic bias circuit.

ensuring that $V_{SG(ML6)} = V_{SG(M1)}$. Therefore, the output voltage $V_{OUT} = V_1 = V_{REF}$. Meanwhile, the bias current is designed as $I_{ML7} = I_{ML6} = I_{M1}$ by selecting the size of transistor M_3 to be twice that of M_{L7}.

D. Proposed Dynamic Bias Circuit

The design principle of the dynamic bias circuit is to make V_{DYN} change with V_{OP}, as shown in Fig. 8. The primary purpose of the dynamic bias circuit is to momentarily change the bias current of the feedback loop of the main circuit when voltage spikes appear at the LDO output in order to quickly charge or discharge gate parasitic capacitance (C_{PAR_IN}) of the power transistor. A sudden drop in V_{OUT} increases V_{OP}, which decreases the drain voltage of transistor M_{D4}. A decrease in the drain and gate voltage of transistor M_{D3} decreases the gate voltage of transistor M_{D2}. Because the V_{SG} of transistor M_{D2} is larger, the current flowing through it becomes larger as well, which causes V_{DYN} to increase instantly. A drop in V_{OUT} causes an increase in V_{DYN}. A sudden drop at the gate of power transistor (M_P) increases the V_{SG} of the power transistor as well as the current flowing through it. This enables a more rapid pull-up of V_{OUT}, returning it to a steady voltage. The addition of the dynamic bias circuit makes the whole circuit respond even faster with better performance.

E. Enhancement of Transient Responses

In Fig. 3, the high-pass network comprises resistor R_T (R_B) and capacitor C_T (C_B). The values of both C_T and C_B are 2 pF and the values of both R_T and R_B are 400 kΩ. Thus, the corner frequency of the high-pass network is 199 kHz. When the load current of the LDO regulator is 100 mA, the crossover frequency of the main feedback loop is 500 kHz. The corner frequency of the high-pass network must be designed to be less than the crossover frequency of the LDO feedback loop. V_{OUT} needs to vary at least 5 mV within 5 μs, so the fast transient circuit and the dynamic bias circuit can be efficiently triggered to respond to and reduce the output spikes.

Fig. 9 shows the measurement results of the load transient responses when $V_{DD} = 1.3$ V, $V_{OUT} = 1.1$ V, and $I_{OUT} = 1-100$ mA. There are three parts in Fig. 9. The top one is the load transient response of the LDO with the proposed circuit, and the middle one is that of the LDO without the proposed circuit. The bottom one shows that I_{OUT} changes between 1 and 100 mA. Both the rise and fall time of the load current range from 1 to 100 mA is 200 ns. The proposed dynamic hybrid biasing improves the undershoot of the output voltage from 480 to 117 mV, while the recovery time is improved from 6 to 1.4 μs. The overshoot is improved from 173 to 28 mV. The proposed approach effectively extends the bandwidth of the feedback loop, and ensures high-speed transient response to signal change.

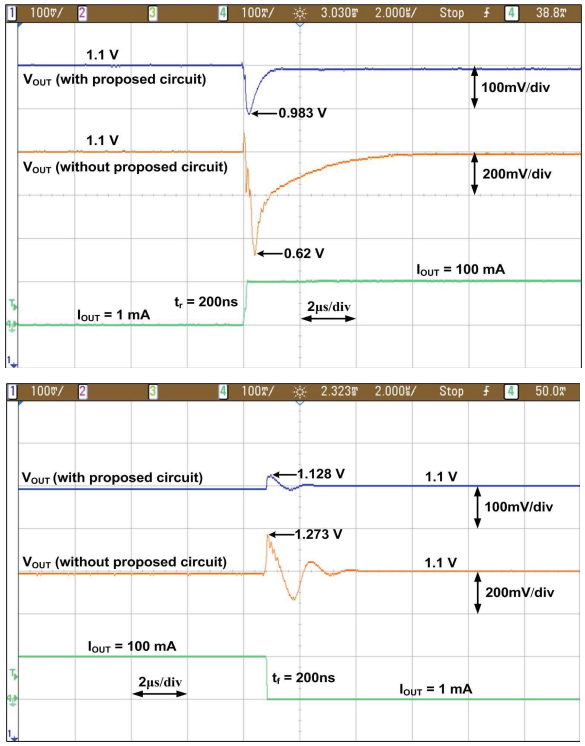

Fig. 9. Comparison of two LDO structures with and without the proposed fast transient circuit, at V_{DD} = 1.3 V, V_{OUT} = 1.1 V, $I_{OUT(MAX)}$ = 100 mA, $I_{OUT(MIN)}$ = 1 mA.

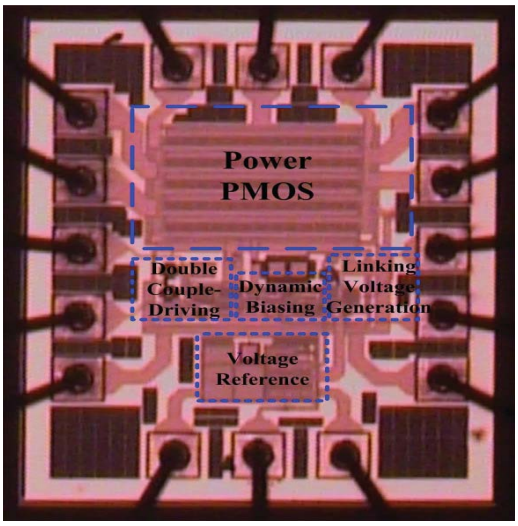

Fig. 10. Die photograph of the proposed LDO voltage regulator.

III. Experimental Results

The proposed LDO regulator was fabricated using the 0.35-μm mixed-signal CMOS 2P4M process. The design of our regulator uses only 3.3 V MOS transistors; therefore, the maximum operation voltage is 3.3 V. Fig. 10 shows the die photograph of the prototype voltage regulator. Fig. 11 shows the input–output voltage characteristics of LDO regulator at I_{OUT} = 100 mA, the dropout region, and line regulation performance. The size of the power transistor is 26 000 μm/0.35 μm to provide high output current. The dropout voltage is 180 mV. Fig. 12 shows the measured line transient response. The supply voltage switches between 1.3 and 2.3 V with 100 mA output current, and voltage spike is 20 mV. Fig. 13 shows the measured load transient response without an off-chip output capacitor. The output current varies from 0 to

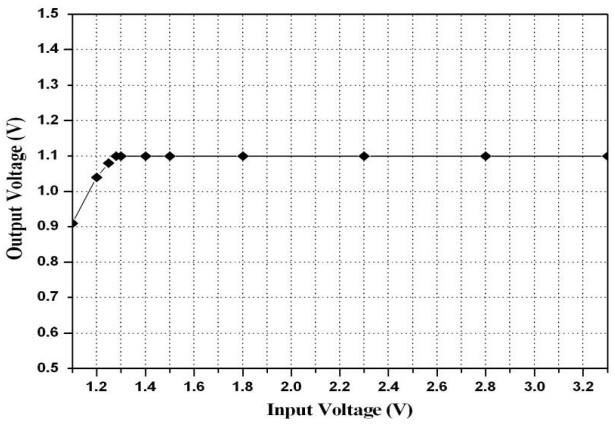

Fig. 11. Input–output characteristics of the regulated voltage.

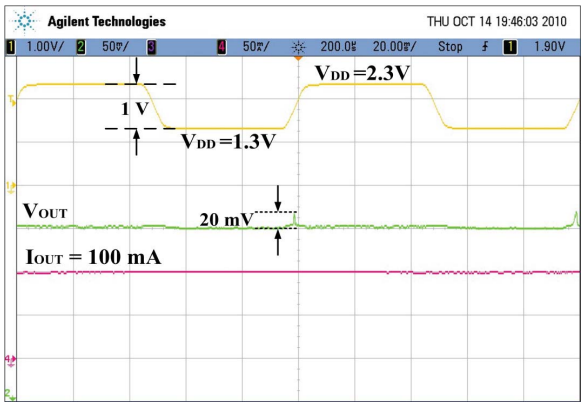

Fig. 12. Line transient measurement result of the proposed LDO voltage regulator without an off-chip output capacitor.

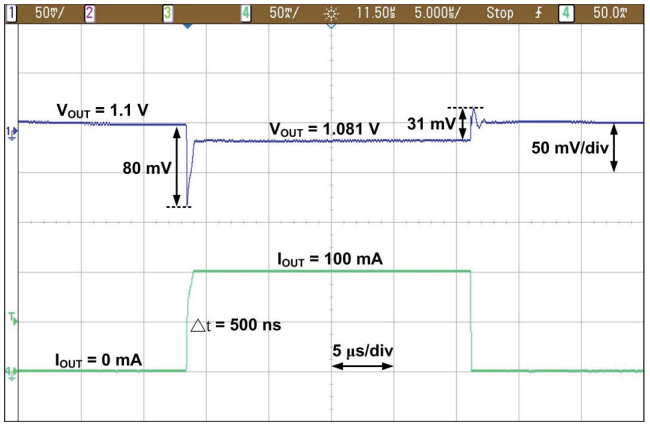

Fig. 13. Load transient measurement result of the proposed LDO voltage regulator without an off-chip output capacitor.

100 mA at 1.3 V supply voltage, while the rise time and fall time of the load current are 5 ns/mA. These measurement results show that the load transient voltage spike is only 80 mV.

The quiescent current of 25 μA was measured with a load current I_{OUT} = 100 mA. All bias current flows into the ground; therefore, we simply measure the current flowing into the ground pin to obtain the quiescent current. The current efficiency was obtained from (1). Fig. 14 shows the current efficiency as a function of load current

$$\eta_I = \frac{I_{OUT}}{I_{GND} + I_{OUT}} = \frac{100\ \text{mA}}{25\ \mu\text{A} + 100\ \text{mA}} = 99.97\%. \quad (1)$$

Performance comparison between some previously reported LDOs and the proposed LDO is summarized in Table I. The figure of merit

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOS

	[2]	[4]	[8]	[10]	This Brief
Technology (μm)	0.5	0.35	0.35	0.09	0.35
Supply Voltage (V)	1.4–4.2	2.0	0.95–1.4	1.2	1.28–3.3
$I_{OUT,MAX}$(mA)	100	200	100	100	100
V_{OUT}(V)	1.21	1.8	1.2	0.9	1.1
I_q	45 μA	20 μA	43 μA	6000 μA	25 μA
$V_{dropout}$(V)	0.2	0.2	0.2	0.3	0.18
ΔV_{OUT}(mV)	120 (ΔI_{OUT} = 100 mA)	54 ΔI_{OUT} = 200 mA	70 (ΔI_{OUT} = 99 mA)	90 (ΔI_{OUT} = 100 mA)	80 (ΔI_{OUT} = 100 mA)
Current efficiency	99.95%	98.8%	99.95%	94.3%	99.97%
Current Capacitor	100 nF	1 μF	0–100 pF	600 pF	0–100 pF
FOM_1 (ps)	59	27	0.03	32	0.02
$T_{R(measure)}$ (μ s)	2.5	15.4	3	0.00054	0.75
FOM_2 (ns)	1.125	1.54	1.29	0.032	0.187
Active area	0.263 mm^2	0.264 mm^2	0.155 mm^2	0.098 mm^2	0.126 mm^2

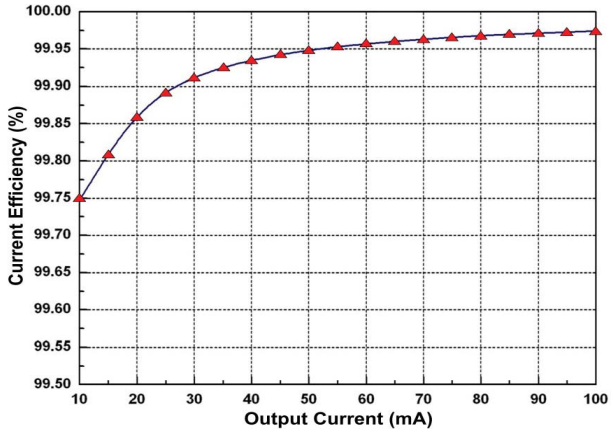

Fig. 14. Current efficiency as a function of load current.

(FOM), given in (2) [10], is adopted in Table I

$$\mathrm{FOM}_1 = T_R \frac{I_q}{I_{\mathrm{OUT,MAX}}} = \frac{C_{\mathrm{OUT}} \cdot \Delta V_{\mathrm{OUT}}}{I_{\mathrm{OUT,MAX}}} \frac{I_q}{I_{\mathrm{OUT,MAX}}}. \quad (2)$$

To show an FOM directly obtained from the measurement data, a measured response time ($T_{\mathrm{R(measure)}}$) from load transient responses is taken into account. Another FOM is defined as

$$FOM_2 = T_{\mathrm{R(measure)}} \frac{I_q}{I_{\mathrm{OUT,MAX}}}. \quad (3)$$

Although our FOM_2 is larger than that of [10], the latter actually has an on-chip output capacitance of 600 pF, which has effectively reduced the measured response time. Therefore, to compare the performance with [10], FOM_1 seems to be a fair index. In addition, our measurement condition for the load transient response ranges from 0 to 100 mA, while the measurement condition in [8] ranges from 1 to 100 mA. The output impedance changes abruptly for load currents ranging from 0 to 100 mA; however, the output impedance does not change a great deal for load currents ranging from 1 to 100 mA. In other words, the measurement conditions for load transient response are far stricter in this case than in [8]. Therefore, the proposed LDO regulator is superior both in static and transient characteristics to the LDO regulator in [8]. By using 0.35-μm CMOS technology, the chip area of the proposed design is smaller than that in both [4] and [8].

IV. CONCLUSION

This brief presented an LDO voltage regulator without the output capacitor that achieves fast transient responses by hybrid dynamic biasing. The dynamic biasing in the proposed fast transient circuit is activated through capacitive coupling. The fast transient through hybrid dynamic biasing circuit senses the LDO output change so as to increase the bias current instantly. The output voltage spike of the LDO with the proposed circuit decreases to 80 mV when the output current changes from 0 to 100 mA and 20 mV when a supply voltage of 1 V input step is applied to the circuit.

The proposed LDO regulator is stable for output current in the complete range of 0–100 mA and does not require any off-chip output capacitor. The proposed circuit improves both the overshoot and the undershoot of the LDO regulator. The FOM of this LDO compares favorably with that of other published designs.

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Digital Error Corrector for Phase Lead-Compensated Buck Converter in DVS Applications

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***Abstract*— Modern low-power system on a chip needs direct current converter with dynamic voltage scaling (DVS) ability for core power supply. The converter output should be accurate voltage across the full load current and voltage scaling range. An integrated buck converter for DVS application is proposed in this brief. Voltage mode phase lead compensation is implemented in the converter, with much smaller passive components than conventional type-III compensation. To improve accuracy, the output voltage error accompanied with load current and reference voltage caused by finite loop gain in analog control loop is corrected by the digital error corrector. The output voltage is compared by two comparators whose threshold voltage is about 10 mV above and below the reference voltage, respectively. The duty cycle is slightly adjusted by finite state machine according to outputs of the two comparators. Experimental results show that the converter is well regulated over an output range of 0.7–1.8 V, with step voltage of 25 mV. When load current suddenly changes between 170 and 500 mA, the overshoot and undershoot voltage are 32 and 50 mV, respectively. Load regulation is maintained about 1% throughout the full load range. The voltage error is within ±10 mV in the voltage scaling range.**

***Index Terms*— Buck converter, digital error corrector, phase lead compensation, voltage mode control.**

I. Introduction

Low-power design techniques have become increasingly important for modern system on chips (SoCs). The dynamic voltage and frequency scaling (DVFS) technique controls the supply voltage and operation frequency of each module in SoC in response to workload demands, leading to substantial power saving while maintaining system performance. Direct current (dc–dc) converter with dynamic voltage scaling (DVS) ability acts as a hardware platform in a typical DVFS system. It is one of the hot topics in current research [1]–[4]. Compared to traditional dc-dc converters, the converter in the DVFS system should have several extra characteristics [1], [2]. Efforts have been made to achieve fast voltage scaling response, by maximum current charging or hysteretic control [2]–[4]. Moreover, voltage accuracy over full load current and voltage scaling range is an important specification, because smaller design margin is allowed, leading to further power saving while eliminating any slack periods caused by egregious low power supply. Accurate output needs high gain error amplifier (EA) and power devices with low resistance. The type-III compensator is often implemented in buck converter for high loop gain, but large off-chip capacitors and resistors limit its implementation in integrated power converters. Though recent advances in research are successful for monolithically integrate type-III compensator by pseudotype-III compensation [5] or extending loop bandwidth [6], the passive components still occupy large area to generate low-frequency pole, or the loop bandwidth is limited [6]. In contrast, the phase lead compensator (PLC) stabilizes buck converter by only one high-frequency zero, so the area is tremendously reduced with comparable bandwidth with type-III compensation [7]. However, the primary drawback of the PLC is that the loop gain is severely curtailed. Thus, its application in DVFS systems is limited.

This brief details the design of a novel error correction method presented in [8]. The digital error corrector (DEC) is implemented in a phase lead-compensated buck converter. Extra digitally controlled offset voltage is introduced to cancel output error because of low loop gain and parasitical resistors. This brief is organized as follows. In Section II, the error correction scheme is proposed and the detailed circuit implementation is introduced. Section III shows and discusses experimental performance, and Section IV summarizes this brief.

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II. Implementation of Buck Converter With DEC

The simplified block diagram of the proposed buck converter with the proposed DEC is illustrated in Fig. 1. Output voltage $V_{\rm OUT}$ is fed back to the PLC, and the operational transconductance amplifier (OTA) GM converts voltage error between $V_{\rm REF}$ and V_C into differential current in R_1 and R_2, respectively. The differential current is compared with sawtooth current $I_{\rm SAW}$ by comparator Comp to generate pulse-width modulation (PWM) signal. $I_{\rm SAW}$ and global clock signal CLK are provided by OSC. Power devices MP and MN are controlled and driven by RS latch and driver. There are two comparators designed accompanied with GM whose outputs are Comp_H and Comp_L, respectively. The threshold voltages to trigger Comp_H and Comp_L are defined as $V_{\rm OUT,\ MAX}$ and $V_{\rm OUT,\ MIN}$, respectively. The proposed DEC introduces digitally controlled current source at node V_1 to adjust duty cycle slightly according to Comp_H and Comp_L, until $V_{\rm OUT}$ is between $V_{\rm OUT,\ MAX}$ and $V_{\rm OUT,\ MIN}$. Then there is digitally controlled input offset voltage of EA introduced by DEC. The original output voltage error due to low loop gain is compensated by the offset voltage. Thus the regulation and output accuracy are enhanced.

A. Analog Control Loop

The schematic of control blocks in Fig. 1, such as PLC, GM comparators, and $I_{\rm SAW}$ generation, is shown in Fig. 2. PLC is realized by operational amplifier OP, resistors R_{C1}, R_{C2}, and capacitor C_C. GM is designed on the basis of symmetrical OTA. Voltage error between V_C and $V_{\rm REF}$ is converted into current error in R_1 and R_2. $I_{\rm SAW}$ generated by $I_{\rm SAW}$ generation block flows out from node V_2 and output current of DEC flows from node V_1. The two comparators are current comparators, and $\rm IB_1$ and $\rm IB_2$ are designed to make $V_{\rm OUT,\ MAX}$ about 10 mV higher than $V_{\rm REF}$ and $V_{\rm OUT,\ MIN}$ about 10 mV lower.