A 10-b 125-MHz CMOS Digital-to-Analog Converter (DAC) with Threshold-Voltage Compensated Current Sources

Shu-Yuan Chin and Chung-Yu Wu

Abstract—**This paper describes a 10-b high-speed COMS DAC fabricated by 0.8-μm double-poly double-metal CMOS technology. In the DAC, a new current source called the threshold-voltage compensated current source is used in the two-stage current array to reduce the linearity error caused by inevitable current variations of the current sources. In the two-stage weighted current array, only 32 master and 32 slave unit current sources are required. Thus silicon area and stray capacitance can be reduced significantly. Experimental results show that a conversion rate of 125 MHz is achievable with differential and integral linearity errors of 0.21 LSB and 0.23 LSB, respectively. The power consumption is 150 mW for a single 5-V power supply. The rise/fall time is 3 ns and the full-scale settling time to $\pm 1/2$ LSB is within 8 ns. The chip area is 1.8 mm $\times$ 1.0 mm.**

I. Introduction

HIGH-SPEED and high-resolution digital-to-analog converters (DAC's) are key components in scanning graphic systems, computer systems, digital TV, high-definition TV, etc. In these systems, the DAC's with the resolution higher than 8-b and the operating frequency higher than 65 MHz are required. Realizing such DAC's in COMS has many advantages such as low cost, low power consumption, and good I/O compatibility with both COMS and TTL circuitry. Moreover, CMOS DAC's have good compatibility with memories and digital processing systems so that they can be integrated on the same chip.

Recently, many high-speed CMOS DAC's have been designed using either weighted current array [1]–[4] or current cell matrix [5]–[7]. These current-switching DAC's allow fast and accurate settling. However, parameter gradients over a wafer and mutual mismatches of current sources result in large variations on the performance of the fabricated DAC's. Thus the resolution of these DAC's is often restricted to 8 b. In [8]–[10] special layout arrangement and switching sequence are used to improve the linearity of current matrix so that 10-b resolution is achievable. Most of them [9]–[10] require careful combinations on the interconnection netwrok of $2^n - 1$ equally sized MOS current sources for a n-b DAC. Thus both wiring and switching complexity and silicon area are increased significantly for a high-bit video DAC. Large silicon area also makes the mismatching and threshold variations among the current sources worse and worse. In [11], another 10-b DAC is proposed which uses resister strings with a wide-band output buffer to drive low-resistance load. Although the passive components of the DAC can achieve a good linearity, the design of the wide-band, high-drive, and high-speed output buffer is often difficult to be achieved. This limits the maximum operating frequency of the DAC.

In this paper, a 10-b 125-MHz DAC fabricated in 0.8-μm double-poly double-metal CMOS process is designed by using new current sources called the threshold-voltage compensated current sources. These threshold-voltage compensated current soruces use the local matching technique to overcome the problem of linearity errors caused by threshold-voltage gradients over a wafer. Special switching sequence is not necessary since these current sources do not need global matching. The structure of the proposed DAC is based upon the weighted current sources that can drive a 50-Ω doubly terminated cable without an output buffer. In this structure, 5-b master stage and 5-b slave stage current arrays can be adopted to reduce the number of current sources as well as the amount of parasitic capacitances. Thus only 32 master and 32 slave current sources are required for the 10-b DAC with two-stage current array structure. Because the current level of each master current source is 32 times of that of the slave current source, it is much more difficult to maintain the linearity error of each master current source to be within $\pm 1/2$ LSB over a wafer. However, the tight matching requirement among the current sources in the master stage can be achieved by the threshold-voltage compensated current sources. No special decoding of the digital input data is used. Thus complicated decoding circuitry can be avoided.

In Section II, circuit structures, operation principles, and design considerations of two-stage current array DAC and threshold-voltage compensated current sources are presented and analyzed. In Section III, the measurement results are described. Section IV gives conclusions.

II. Chip Design

A. Two-Stage Architecture

The circuit diagram of a conventional weighted-current-source DAC is shown in Fig. 1 [2]. Weighted cascode current sources are switched between output load and dummy load, according to the value of the input bits which controls the

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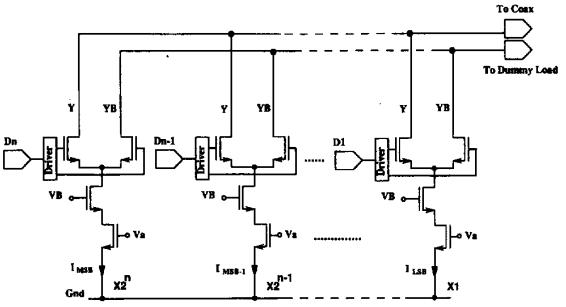


Fig. 1. Conventional weighted-current-source DAC architecture.

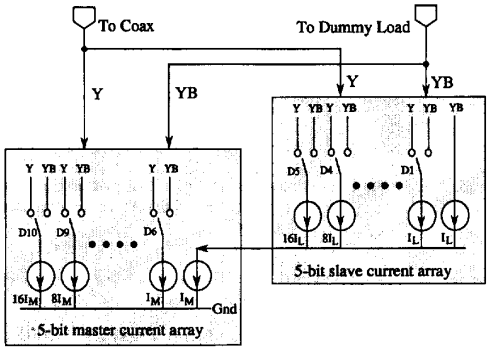


Fig. 2. The block diagram of the two-stage DAC.

output voltages of the drivers to drive the source-coupled current switches. The switch circuit can keep a constant current flowing at the coupled source node and thus fast settling of output can be achieved. The configuration of Fig. 1 requires n binary weighted current sources for a n-b DAC. Taking the binary-weighted size of the current sources into account, the total equivalent unit current source number is $2^n - 1$. To increase the matching accuracy, a special wiring method or switching sequence is also required [2]–[11]. Thus both wiring complexity and silicon area are increased significantly for a high-resolution video D/A conversion. For example, 1023 equivalent unit current sources are required for a 10-b resolution. Large silicon area also makes the inevitable mismatches among the current sources more serious.

Fig. 2 shows the block diagram of a 10-b two-stage current array DAC. In this approach, a primary or master current array is used for the 5 MSB's, whereas a secondary or slave current array is used for the 5 LSB's. In this structure, only 32 master and 32 slave equivalent unit current sources are required for a 10-b DAC. The unit current of each master (slave) current array is the same and denoted as $I_M(I_L)$. The binary-weighted number of unit current sources are connected together to form the binary-weighted current source for each bit. One of the master current source is used to drive the overall slave current array which further partitions the master current into the slave binary-weighted bit currents with the unit current I_L.

The above master–slave current array configuration is usually used in the design of high-speed bipolar DAC's with 8-b

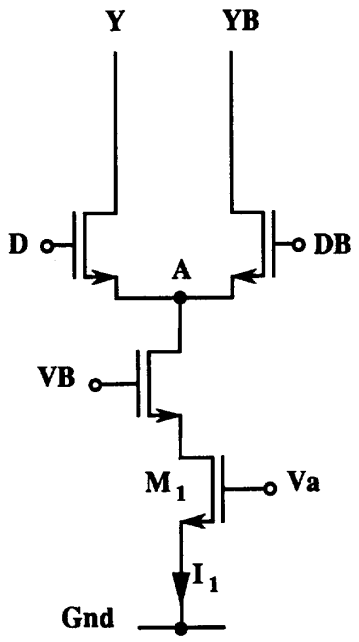


Fig. 3. Conventional switched current source.

or higher resolution. It greatly reduces the number of current sources and thus simplifies the connection among these current sources and makes more efficient use of the chip area [3]–[4]. The amount of stray capacitance at the common source node is small and the recovery time of the voltage at this node during the switching transition can be reduced to achieve a fast conversion. However, it is much more difficult to maintain the linearity accuracy of each master current source to be within $\pm 1/2$ LSB since the current level in each master current source is 32 times of that in the corresponding slave current source. This problem is not severe in bipolar IC's since the bipolar device parameter variations are more tolerable than that of CMOS. That is why this configuration is often used to realize a high-resolution video DAC in bipolar process. Even though this configuration is also used to realize CMOS video DAC [5]–[8], the slave current array is not more than 3 b. Since the threshold-voltage compensated current sources can achieve good linearity over the wafer, they are used in the two 5-b stage current arrays to realize 10-b video CMOS D/A conversion.

B. Threshold-Voltage Compensated Current Sources

Fig. 3 shows a conventional switched current source. If the Early effect is neglected, the source current I_1 can be expressed as:

$$I_1 = K\frac{W_1}{L_1}(\mathrm{Va} - V\mathrm{th}_1)^2 \tag{1}$$

$$K = \frac{\mu n \mathrm{Co}}{2}$$

where μn is the surface mobility, Co is the channel oxide capacitance per unit area, $W(L)$ is the channel width(length),

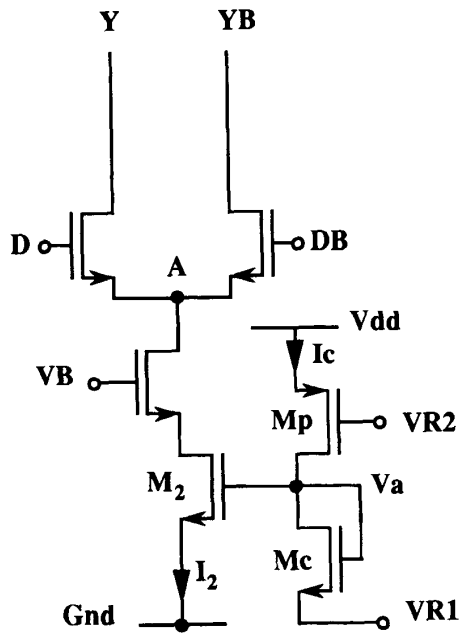


Fig. 4. Switched current source with threshold-voltage compensation.

and $V\text{th}$ is the MOS threshold voltage. In the conventional video DAC with higher than 8-b resolution, a large number of current sources and large chip area are required. The total current is several mA. In this case, the current sources could be hundreds of micrometers apart on the chip and thus the variation of the threshold voltages could be as large as 80 mV due to the oxide thinning effect [2].

The threshold-voltage compensated current source shown in Fig. 4 is proposed to reduce the linearity error caused by the threshold-voltage variations over a wafer. In this circuit, the cascode structure is also used to increase the output impedance of the current source and thus suppress the current variations due to the voltage fluctuations across the current source. Neglecting the Early effect, the source current I_2 can be written as:

$$I_2 = K\frac{W_2}{L_2}(\text{Va} - V\text{th}_2)^2 = K\frac{W_2}{L_2}(\text{VR}_1 + \Delta V + V\text{th}_c - V\text{th}_2)^2 \qquad (2)$$

where

$$\Delta V = \text{Va} - \text{VR}_1 - V\text{th}_c.$$

In this case, the source current is varied with the difference of $V\text{th}_2$ and $V\text{th}_c$ rather than $V\text{th}_2$. As long as the transistors M_2 and M_c are locally matched, $V\text{th}_c - V\text{th}_2$ and the current I_2 is independent of the threshold voltages. Thus the undesirable current variations of the current sources can be reduced significantly. Even if the threshold-voltage mismatch exists, the variation of $V\text{th}_c - V\text{th}_2$ is still much smaller than VR_1, so that the variation of I_2 is also very small.

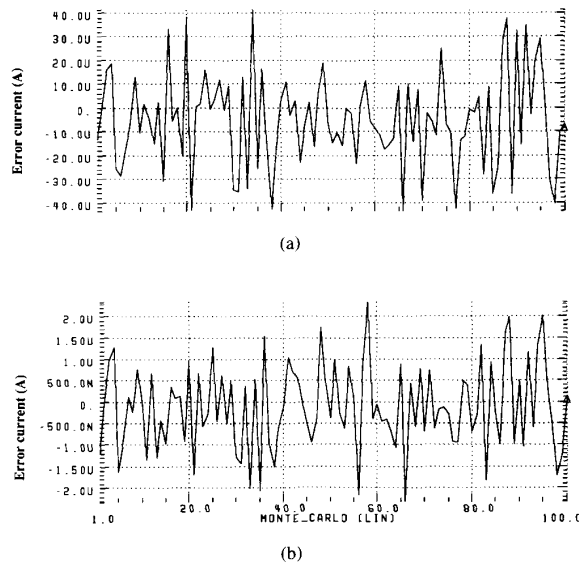


Fig. 5. SPICE Monte-Carlo simulation results for (a) conventional weighted current sources, (b) current sources with threshold-voltage compensation.

ΔV in (2) is dependent upon the value of I_c, which is generated by the nonideal current source Mp. Thus ΔV can be expressed as a function of I_c. Using the expression, (2) can be rewritten as

$$I_2 = K\frac{W_2}{L_2}\left(\text{VR}_1 + V\text{th}_c - V\text{th}_2 + \sqrt{\frac{L_c I_c}{KW_c}}\right)^2. \qquad (3)$$

As seen from (3), VR_1 should be as high as possible and I_c should be as small as possible to reduce the variation of I_2 due to I_c. The W/L ratio of the transistor Mp should be very small and the bias VR_2 should be very high to let $I_c \ll I_2$. Thus the variation of I_c causes only a small change of I_2. In order to keep the variation of I_c as small as possible, all of the PMOS transistors (Mps) in each 5-b current array should be locally matched.

SPICE Monte-Carlo simulation results for both conventional current sources and new current sources with threshold-voltage compensation are shown in Fig. 5. It can be seen from Fig. 5 that the proposed new current source circuits can reduce the current variations from ± 40 μA to ± 2 μA when the threshold voltage variation of NMOS devices is within ± 0.1 V and that of PMOS devices is within ± 20 mV with a Gaussian distribution. Thus this new circuit can achieve 20 times better matching than the conventional current sources.

C. Two-Stage Weighted-Current-Source DAC

Using the two-stage current array configuration and threshold-voltage compensated current sources, the weighted-current-source DAC can be designed as shown in Fig. 6. Note that the LSB current array is connected in cascode to the first current source of the MSB current array. Although the switched current sources in the LSB current array do not use the cascode structure of Fig. 4, they are actually cascoded with

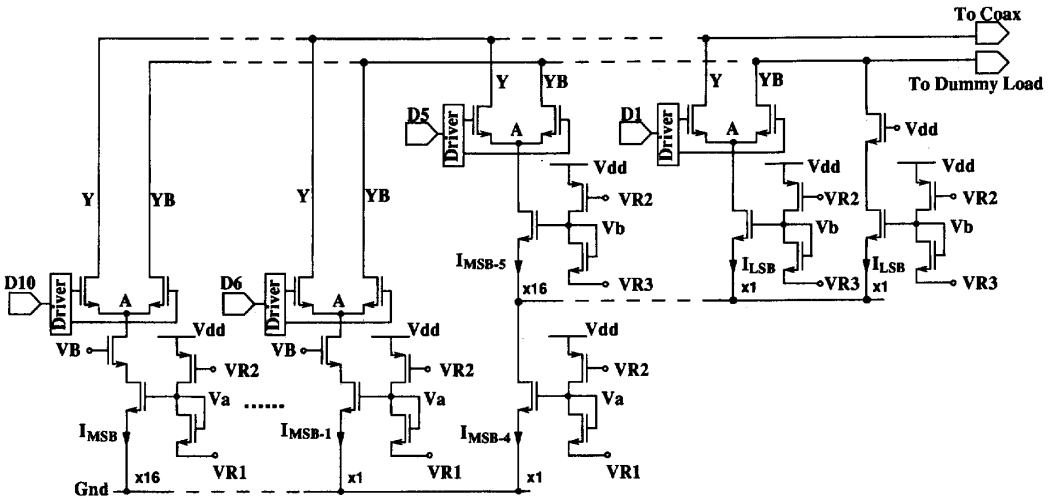


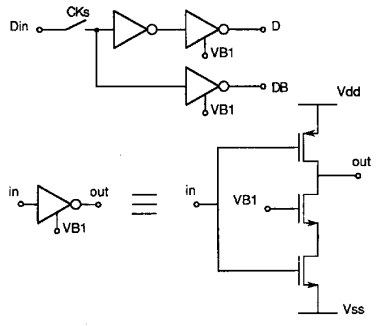
Fig. 6. Two-stage weighted-current-source DAC with threshold-voltage compensated current sources.

the first current source in the MSB current array and have a high output impedance as the cascode structure of Fig. 4.

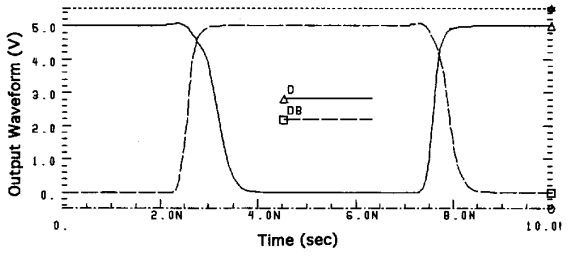
Two methods can be used to obtain a fast settling time. First, the stray capacitance at the common source node of the differential current switches should be kept small to shorten the recovery time of the voltage at the common source node of the differential current switches during transition. This can be easily achieved in this two-stage current array DAC since the two-stage structure requires only 32 master and 32 slave equivalent unit current sources for a 10-b resolution. Secondly, the differential current switches can not be turned off simultaneously to prevent from large glitch energy which causes long time period to charge the common source node of the differential current switches and discharge the output node of the DAC. If the differential current switches are turned off simultaneously, the common source node of the differential current switches will be rapidly discharged toward ground and the output node of the DAC will be charged toward power supply voltage. Thus in the following operation, a very long time is required to recharge the common source node of the differential current switches and discharge the output node of the DAC to their optimum operation points. This increases the settling time of the DAC.

To reduce the glitch energy and increase the settling speed, all input digital signals must be input at the same time. The cross point of rising/falling waveforms in the input drivers is also very important. If the cross point of rising/falling waveforms in the input driver is high enough, the differential current switches will not turn off at the same time. In this design, the logic threshold voltages of input drivers must be designed to be higher than 4 V to overlap the output waveforms at higher voltage. Thus the time period when the differential current switches are both turned off can be eliminated and that when both switches are heavily turned on can be strictly reduced.

In this DAC, a three-MOS inverter as shown in Fig. 7(a) is used as the input driver to increase the logic threshold and



(a)



(b)

Fig. 7. (a) The circuit; (b) the SPICE simulated output waveforms of the input driver with high logic-threshold.

generate overlapped output waveforms shown in Fig. 7(b). The SPICE simulated output waveforms of input drivers show that the rising/falling cross voltage is higher than 4 V.

D. Chip Implementation

Since the total output current as high as 15- to 25-mA is required to drive the total output load of 10- to 20-pF and achieve fast settling, the line voltage drop along the power

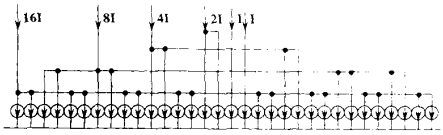
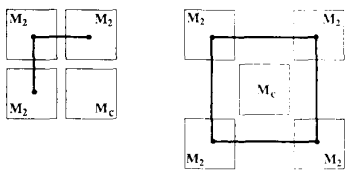


Fig. 8. Symmetrical layout configuration of each 5-b current array.



(a) (b)

Fig. 9. Different layout arrangement of the devices M_2 and M_c in each current source: (a) 4-cell unit; (b) 5-cell unit.

supply line and ground line could be large enough to cause a gradient error. Therefore, large width of power supply line and ground line is required to reduce the voltage drop. In each 5-b current array, symmetrical layout configuration shown in Fig. 8 is used to reduce the linearity error caused by the undesirable current variations of the 32 unit current sources. To reduce the noise caused by digital circuitry, analog power lines and digital power lines are both separated. The substrate of digital circuitry is biased by the analog power supply rather than the digital power supply to prevent the digital noise from passing through the substrate and coupling to the analog circuitry.

Two kinds of layout methods for the devices M_2 and M_c in each threshold-voltage compensated current source are tested in this chip. Fig. 9(a) shows a 4-cell unit layout of the current source. In this topology, the transistor M_2 is separated into three pieces which are put together with the threshold-voltage compensated transistor M_c to form a compact square. Similarly, Fig. 9(b) shows a 5-cell unit layout of the threshold-voltage compensated current source. In this topology, the transistor M_2 is separated into four pieces which are put around the threshold-voltage compensated transistor M_c to form a directional-symmetric layout.

In order to obtain a better matching among each threshold-voltage compensated current source of Fig. 4, all the transistors except Mp are put together in layout to form an unit. All the transistors Mps in the current array are also put together in layout to achieve a good local match. Each source current (I_c) of Mp is locally generated and delivered to each threshold-voltage compensated current source.

III. Experimental Results

Fig. 10 shows the chip photograph of two new DAC's. The chips were fabricated in 0.8-μm double-poly double-metal CMOS technology. The DAC located on the upper part of the chip adopts the threshold-voltage compensated current sources with 4-cell unit layout whereas the DAC located on the lower part of the chip adopts the threshold-voltage compensated current sources with 5-cell unit layout.

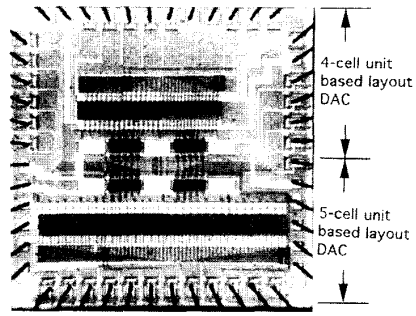


Fig. 10. Photograph of the DAC's.

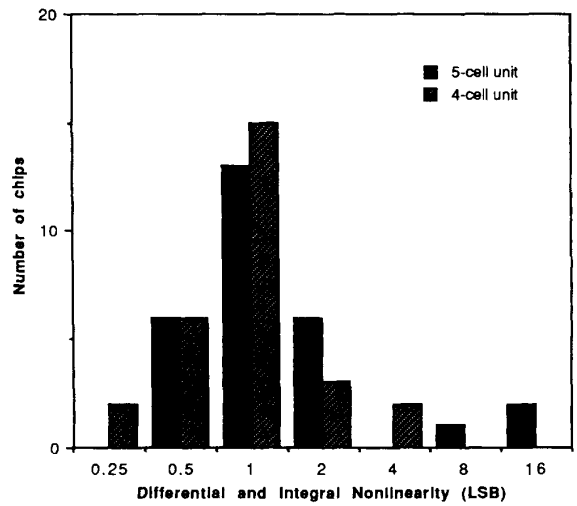


Fig. 11. The nonlinearity histogram of the proposed DAC's with two kinds of layout methods.

TABLE I
Differential and Integral Linearity Distribution of Two Kinds of Layout Methods for Each Current Source

Linearity Error	4-Cell Unit(%)	5-Cell Unit(%)
< 1/2 LSB	28.6	21.4
< 1 LSB	82.1	67.9
< 2 LSB	93.9	89.3

The fabricated DAC's are measured with 20-pF output load (including the bonding pad loading) in parallel with a 50-Ω doubly terminated cable. A 25-Ω resistor is used at the dummy output. The reference voltages VR_1, VR_2 and VR_3 are set to 1.5 V, 4.2 V, and 2.6 V, respectively. Forty dies have been tested and the nonlinearity histogram of the proposed DAC's with two kinds of layout methods is shown in Fig. 11. The yield is shown in Table I. It is obvious that the DAC with the threshold-voltage compensated current sources of 4-cell unit layout has a better linearity than that with the threshold-

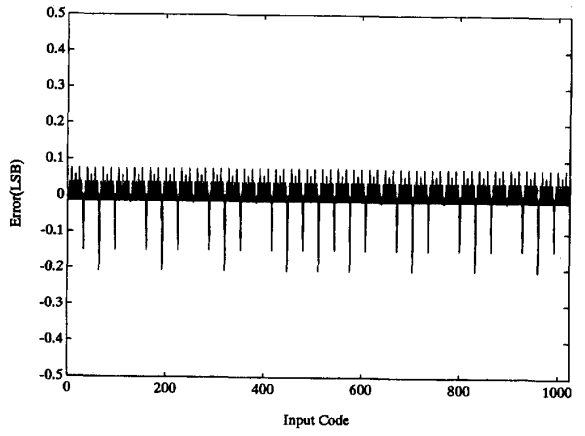


Fig. 12. Differential linearity error of the DAC.

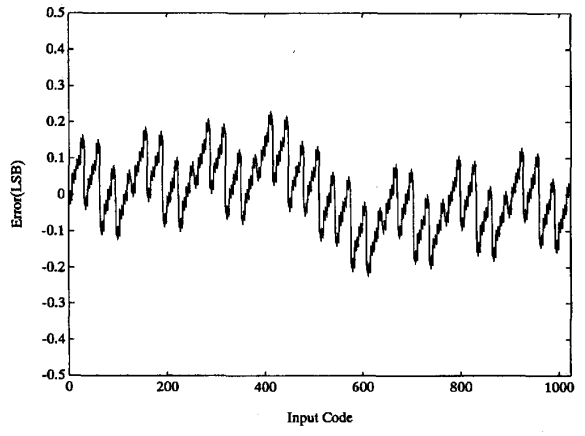


Fig. 13. Integral linearity error of the DAC.

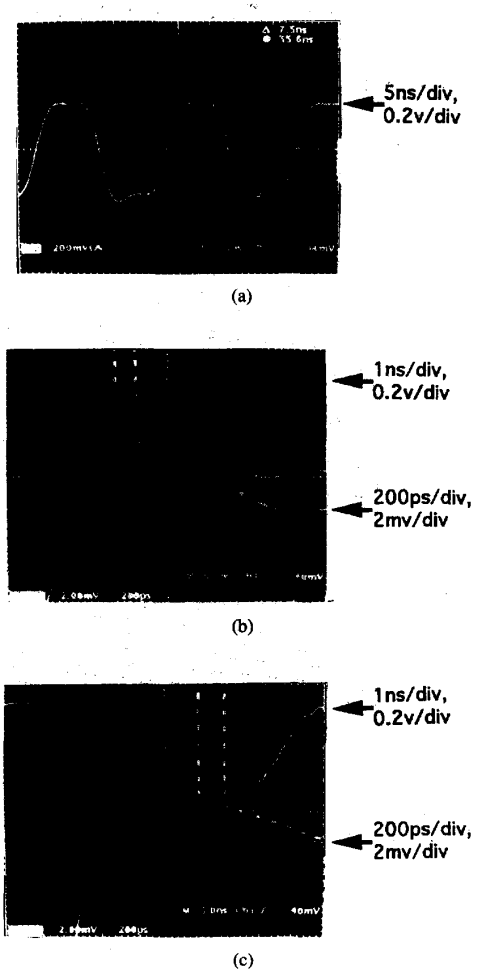


Fig. 14. Full-scale transitions of the fabricated DAC in (a) full-swing operation; (b) zooming on the rising edge; (c) zooming on the falling edge.

voltage compensated current sources of 5-cell unit layout. This means compact layout for each current source is more effective than directional-symmetric layout in reducing the linearity error. Thus the reduction of the directional mismatch is less important than that of the mismatch due to separate distance.

The measurement results shown in Fig. 12 to 15 are done for the DAC which adopts threshold-voltage compensated current sources with 4-cell unit layout since it has a better linearity than another one. Being seen from Fig. 12 and 13, the differential linearity error of 0.21 LSB and the integral linearity error of 0.23 LSB can be attained. Thus the fabricated DAC has 11-b accuracy. Fig. 14 shows the full-scale transition and the zooming on rising and falling edges. It can be seen that the 10–90% rise/fall time is 3 ns and the full-scale settling time to $\pm 1/2$ LSB is within 8 ns. They are almost independent of the rise/fall times of the digital input signals. The maximum glitch energy (the transition between 0111111111 and 1000000000) shown in Fig. 15 is 40 ps.V. Fig. 16 shows the measured output spectrum of the DAC with an input frequency of 3.9 MHz at 125 MHz conversion rate. Further reduction could be realized by using glitchless techniques reported in the literature [9]. The overall signal-to-noise ratio and distortion is obviously dominated by the first and fourth harmonic distortion at 56 dB below signal level. The chip area (without pads) is 1.8 mm $\times$ 1.0 mm. The power consumption is 150 mW. The major characteristics of the fabricated DAC are concluded in Table II.

TABLE II
CHARACTERISTICS OF THE DAC

Resolution	10 bits
Differential Nonlinearity	0.21 LSB
Integral Nonlinearity	0.23 LSB
Conversion rate	125 MS/s
Settling Time (±1/2 LSB)	< 8 ns
Rise/Fall time (10-90%)	3 ns
Glitch Energy	40 psV
Power Dissipation	150 mWatts
Supply Voltage	5V
Process	0.8um CMOS
Chip Size (without pads)	1.8mm × 1.0mm

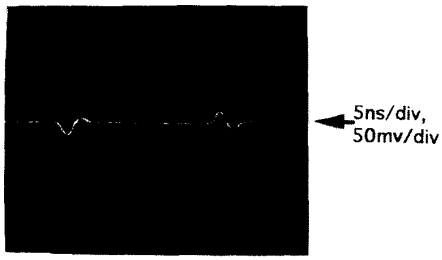


Fig. 15. Photograph of the measured glitch energy of the DAC.

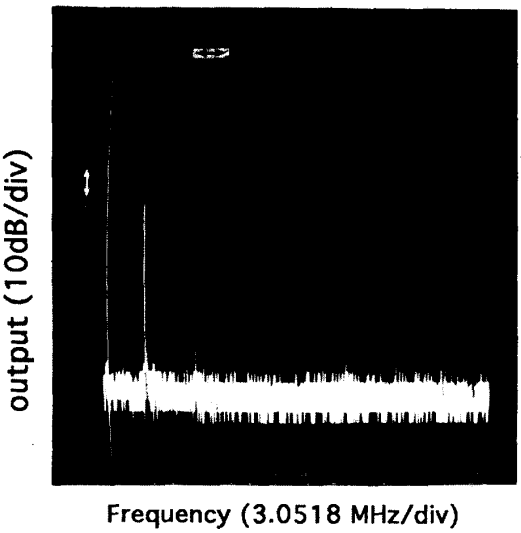


Fig. 16. The measured output spectrum of the DAC with an input frequency of 3.9 MHz at 125 MHz conversion rate.

IV. Conclusion

A 10-b video CMOS DAC has been successfully designed and tested in a 0.8-μm double-poly double-metal CMOS process. Using two-stage current array structure, only 32 master and 32 slave unit current sources are required for a 10-b resolution. The tight matching requirement of the two-stage current array DAC is achieved by adopting the threshold-voltage compensated current sources. In this DAC, the chip area, wiring complexity, and parasitic capacitance can be reduced significantly whereas 10-b resolution and 125-MHz conversion rate can be readily obtained.

The threshold-voltage compensated current source proposed in this work can also be applied in many other IC design to reduce the inevitable threshold-voltage variations over a wafer. These applications will be addressed in the future.

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