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# Efficiency Enhancement of PEDOT:PSS/Si Hybrid Solar Cells by Using Nanostructured Radial Junction and Antireflective Surface

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**ABSTRACT:** We demonstrate the implementation of a hybrid solar cell that comprises a surface nanostructured n-type Si and poly(3,4-ethylenedioxythiophene):poly-(styrenesulfonate). The Si surface before deposition of the organic layer was nanostructured by using CsCl self-assembled nanoparticles as a hard mask and dry etching to form radial junction architectures and enhance light diffusion and absorption. Apart from the textured Si surface, processing parameters such as from metal-electrode shadow ratio, spin-coating rate, and surfactant addition were properly adjusted to improve overall cell performance. Our hybrid solar cells



achieve the best performance under optimized cell parameters with a power conversion efficiency of 8.84% and short-circuit current density of  $30.5 \text{ mA/cm}^2$ . This combined technique provides a simple, scalable, and cost-effective process for fabricating hybrid solar cells.

KEYWORDS: nanostructure, hybrid solar cell, cesium chloride, conductive polymer, light trapping, antireflective

## 1. INTRODUCTION

Crystalline Si has dominated photovoltaic markets for years because of its abundant material supply, nontoxicity, and high efficiency. However, the growth of the Si photovoltaic industry has been limited because of expensive fabrication processes and materials. Conventional Si solar cells have p-n junctions for the efficient separation of light-generated charge carriers. The p-n junction is normally formed by furnace diffusion, which is expensive and requires very high temperatures ( $\sim 1000$  °C). Organic solar cells that are created with conjugated polymers, which can be fabricated with inexpensive materials by using low temperature solution processes, and have the potential to lower costs; however, the efficiency of organic solar cells is lower than Si-based devices. Therefore, hybrid solar cells that combine Si and conjugated polymers at low temperatures provide a possible alternative technology to simplify fabrication processes and reduce costs.<sup>1-17</sup>

A conjugated polymer called poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PE-DOT:PSS) is the most widely used organic material for hybrid devices. PEDOT:PSS is transparent, is conductive (1000 S/cm), and can produce a Schottky junction with Si.<sup>12-17</sup> Illuminative light is absorbed in n-type Si, and a hole transport layer in PEDOT:PSS can extract holes generated in the Si substrate out of the device. Thus, the efficiency of the hybrid PEDOT:PSS/Si solar cell is comparable to a conventional Si p-n junction solar cell in principle.

To reduce the cost of photovoltaic devices further, significant efforts have been made in reducing the thickness of the Si substrate, which requires considerable improvement in light absorption. The use of nanoscale surface structures which are more useful for thin-film devices than traditional microscale texturing for crystalline Si solar cells is a promising method to enhance light absorption.<sup>11,12</sup> Nanoscale surface structures such as nanowire,<sup>10–12,14–17,20</sup> nanorod,<sup>21</sup> and nanocone<sup>13,22</sup> not only provide enhanced absorption properties by antireflective and light scattering effects but also offers a large junction area for charge separation and radial junction architecture. Radial junction-array solar cells allow efficient charge transport and high light-harvesting capabilities because of the decoupling of light absorption and charge-carrier collection directions.<sup>10–17,20–22</sup> Nanoscale surface structures have been widely applied as antireflective coatings<sup>23,24</sup> for crystalline Si solar cells,<sup>20,21</sup> thin-film solar cells,<sup>22</sup> organic solar cells,<sup>25</sup> and hybrid solar cells<sup>10–17</sup> because of their significant advantages.

Nanostructures can be fabricated by using various techniques that involve lithography and etching. Versatile techniques such as self-assembly lithography<sup>26–30</sup> have recently emerged as promising candidates for fabricating nanostructures and reducing costs. Thin films consisting of self-assembled islands have been used as etching masks for the fabrication of surface nanostructures. These materials used in island films, which are typically metals, can be easily formed over large area.<sup>26–28</sup> Compared with metals, cesium chloride (CsCl) self-assembly

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Figure 1. Current density-voltage (J-V) characteristics of the devices with different shadow ratio of front metal electrode.

has been recently used to fabricate structures with larger distributions by controlling film thickness and relative humidity and by developing time.<sup>29,30</sup> CsCl can be easily removed with water; thus, this material does not leave behind any contaminants. However, one should note that the gaps between nanostructures should be controllable to allow polymers to infiltrate and form thin films on the Si surface.<sup>13</sup>

In this study, we demonstrate a hybrid solar cell that comprises a nanostructured n-type Si surface and PEDOT:PSS. The surface structure of Si was engineered by combining CsCl self-assembly and dry etching to form radial junction and antireflective architectures for light absorption enhancement.

#### 2. EXPERIMENTAL SECTION

2.1. Fabrication of Si Nanostructure by Using CsCl Self-Assembly and Reactive Ion Etching (RIE). Nanostructures were fabricated on n-type, polished (100) oriented Si wafers with 500  $\mu$ m thicknesses and 1  $\Omega$ -cm to 20  $\Omega$ -cm resistivity. First, a thin layer of CsCl was deposited by thermal evaporation. The wafers were then exposed to moisture to allow hemispherical CsCl islands to form by self-assembly. The size, shape, and density of the self-assembly can be adjusted by controlling the evaporated film thickness, exposure time of the film in air, and relative humidity of air. Two nanostructured samples were fabricated in this experiment, namely, NS1 and NS2, which had 20 and 10 nm CsCl layer thickness, 50 and 10 min exposure times to air, and 12% and 40% relative humidity, respectively. Thereafter, these structures were transferred on Si by using CF<sub>4</sub> RIE for 2 min at 30 sccm, 20 mTorr, and 100 W. Finally, the samples were washed by deionized water to remove residual CsCl and cleaned by oxygen plasma.

**2.2. Hybrid Solar Cell Fabrication.** The Si substrate after initial cleaning was dipped in dilute hydrofluoric (HF) acid (2%) to remove native SiO<sub>2</sub>. Immediately after HF cleaning and drying, a 100 nm thick Al layer was deposited on the backside for cathode contact by using the sputter system. A highly conductive polymer solution was then prepared by mixing PEDOT:PSS (PH1000, Clevios) solution with 5 wt % dimethyl sulfoxide (DMSO) as a secondary dopant to increase conductivity. PEDOT:PSS was deposited onto the Si substrates by spin coating followed by thermal annealing at 120 °C for 10 min. Finally, the front anode contact was fabricated with a 60 nm thick Ag grid by electron beam evaporation through a steel foil shadow mask.

#### 3. RESULTS AND DISCUSSION

To compare the performance of the hybrid solar cell with and without surface nanostructures, we first fabricated hybrid solar cells on a flat surface and optimized the efficiency with process parameters. The thickness of the organic PEDOT:PSS layer was controlled by the spin-coating rates. Under spin-coating rates of 1000, 3000, 5000, and 7000 rpm, the thicknesses of the PEDOT:PSS layer were 140, 70, 50, and 40 nm, respectively. Although the PEDOT:PSS layer is sufficiently conductive for forming a Schottky junction with Si and transporting lightgenerated holes out of the Si substrate, the conductivity of the PEDOT:PSS layer is insufficient as a top electrode. Therefore, we employed a finger-grid thin film of Ag as the top anode. Figure 1 shows the current density-voltage (J-V) characteristics of the devices with different front metal-electrode shadow ratios. The photocurrent of the solar cells was analyzed by using a solar simulator under air-mass 1.5 global (AM 1.5G) illumination conditions (100 mW/cm<sup>2</sup>, 25  $^{\circ}$ C). The three tested devices have the same electrode-finger width of 100  $\mu$ m. The thickness of the PEDOT:PSS layer was set to 70 nm, which produced the best performance for all three devices. Devices with shadow ratios of 4%, 8%, and 18% were controlled by using different finger periods of 2, 1, and 0.5 mm, respectively. The short-circuit current density  $(I_{sc})$  decreases when the light absorption decreases with increasing shadow ratios. The fill factor (FF) improves from 54.9% (with a shadow ratio of 4%) to 61.9% (with a shadow ratio of 8%) and 69.1% (with a shadow ratio of 18%). The improvement in FF is attributed to the decrease in series resistance from 5.2  $\Omega \cdot cm^2$  to 3.1  $\Omega \cdot cm^2$  and 2.4  $\Omega \cdot cm^2$  with increasing shadow ratios from 4% to 18%. The device with the highest top electrode density shows the best power conversion efficiency (PCE) of 6.59% because of improvements in carrier collection even though the  $J_{sc}$  decreases slightly. Therefore, all samples were fabricated by using top electrodes with shadow ratios of 18% throughout the experiment.

Nanostructures on the surface of the n-type Si substrate were fabricated by using CsCl self-assembly and dry etching. The Si substrate was then etched by RIE dry etching by using the CsCl



Figure 2.  $45^{\circ}$  tilted side-view SEM images of (a) NS1 and (b) NS2. The inset is the top view of the structure. All scale bars are 500 nm. (c) Reflectance spectra of different nanostructured profiles. The flat surface is also displayed in parallel for comparison.



Figure 3. J-V characteristics of the devices with different spin-coating rates on NS1 surface structure.



Figure 4. (a-d) 45° tilted side-view SEM images of different spin-coating speeds: (a) 1000 rpm, (b) 3000 rpm, (c) 5000 rpm, and (d) 7000 rpm. All scale bars are 500 nm. (e) J-V characteristics of the devices with different spin-coating rates on NS2 surface structure.

islands as a hard mask. To achieve high light absorption and conformal polymer spin coating, the nanostructures on the Si surface should be smaller than the wavelength of incident light.<sup>18,19</sup> The formation of a tapered nanostructure profile is

preferred.<sup>13,25</sup> The pillar structures, which is referred as the NS1 structure in this paper, has a 100 to 200 nm diameter and 100 nm depth (scanning electron microscopy (SEM) image, Figure 2a). The reflectance spectra of the Si substrates with



Figure 5. (a) EQE and (b) reflectance spectra of the hybrid solar cells fabricated with 3000, 5000, and 7000 rpm on NS2 surface structure, and the flat surface device with 3000 rpm is also displayed in parallel for comparison. (c) Enhancement ratios in EQE and light absorption between the flat device and device made at a spin-coating rate of 7000 rpm.

nanostructured surfaces were measured by using a UV/visible/ NIR spectrophotometer with an integrating sphere for 300 to 1100 nm wavelengths. Figure 2c compares the reflectance spectra of samples with nanostructured profiles and flatsurfaced Si substrates. The flat-surfaced Si substrate shows a reflection above 30% throughout the entire spectra. The NS1 nanostructure reduces the reflectance by approximately 25% to 40%; the reflectance is lower than 10% for wavelengths longer than 450 nm. The average reflectance of the NS1 structure at a wavelength range of 300 to 1100 nm is 8.5%, which is lower than the flat-surfaced Si substrate (39.5%). The NS1 structure provides antireflective and light trapping effects to reduce the surface reflection and increase the absorption of the Si substrate.

Figure 3 shows the J-V characteristics of the devices with different spin-coating rates of PEDOT:PSS in the NS1 structure.  $J_{sc}$  was enhanced to above 25 mA/cm<sup>2</sup> because of increased light absorption compared with samples without nanostructures. However, the open-circuit voltage ( $V_{oc}$ ) and FF of these devices decrease compared with flat-surfaced devices. The decrease of  $V_{oc}$  is attributed to the increasing interface area and void between the polymer and Si, thus leading to increased surface recombination.<sup>13,14,17</sup> The lower FF is caused by the nonuniform polymer coating with voids and surface defects (Figure 2a). The best PCE performance of devices with NS1 surface structures is only 5.21%, which is lower than that of flat-

surfaced samples. This result is caused by the deterioration of FF (54.9%) and  $V_{\rm oc}$  (373 mV) even with increasing  $J_{\rm sc}$  (25.4 mA/cm<sup>2</sup>).

To improve the interface between the polymer and Si, we further modified the surface structure of NS1. Figure 2b shows the SEM image, which is referred to as the NS2 structure, with diameters from 100 to 150 nm and a depth of 100 nm in this study. By controlling the CsCl self-assembly process, the NS2 structure achieves a tapered shape and smooth walls, which are preferred for conformal polymer—surface coverage via spin coating. Surface reflection was also investigated to compare the NS2 structure and flat-surfaced Si substrate (Figure 2c). The reflectance of the NS2 structure is lower than 10% for wavelengths longer than 450 nm. The average reflectance of the NS2 structure in the wavelength range of 300 to 1100 nm is 9.6%, which is close to that of the NS1 structure.

We used spin coating with different speeds to deposit the polymer and adjust the PEDOT:PSS/Si interface. Figure 4a–d shows the SEM images of the PEDOT:PSS morphology coated on the surface of the NS2 structure at speeds of 1000, 3000, 5000, and 7000 rpm. Under a low spin-coating rate, the polymer formed a flat thin film with numerous voids between the polymer and Si (Figure 4a). The surface coverage of the polymer improves with increasing spin-coating rate. We were able to deposit the most conformal polymer film over the Si nanostructure under a spin-coating rate of 7000 rpm (Figure



Figure 6. J-V characteristics of the devices with and without Triton X-100 wetting agent.

4d). Figure 4e shows the J-V characteristics of the four devices with different spin-coating rates. Under the slowest speed, the device shows the lowest  $V_{oc}$  (391 mV) because the polymer is unable to fully infiltrate into the space between the Si nanostructures and form a continuous junction, thus leading to increased carrier recombination.<sup>13,14,17</sup> Furthermore, the top surface is now smoother, thus reducing the antireflective effect.  $J_{sc}$  reaches 21.8 mA/cm<sup>2</sup>, which is a slight increase compared with that of flat-surface device. The PCE was only 5.60%, which is lower than devices without surface nanostructures. The performance of solar cells gradually improves with increasing spin-coating rates. For devices at 3000 and 5000 rpm,  $V_{\rm oc}$ increases to 401 mV and 417 mV, respectively. J<sub>sc</sub> increases above 27.5 mA/cm<sup>2</sup> because of the significant improvements in surface properties. The device fabricated at a spin-coating rate of 7000 rpm shows the most conformal surface morphology and provides the best results with  $V_{oc}$  at 424 mV,  $J_{sc}$  at 30.6 mA/cm<sup>2</sup>, and PCE at 8.70%. The FFs of all four devices are within a close range (65% to 70%), which is similar to devices without nanostructures. This result indicates that the parameters used for processing the NS2 structure are optimal for processing highly efficient hybrid solar cells.

Figure 5a shows the measured external quantum efficiency (EQE) spectra of the hybrid solar cells fabricated with spincoating rates of 3000, 5000, and 7000 rpm by using the NS2 surface structure. A device built on a flat surface with a spincoating rate of 3000 rpm is displayed in parallel for comparison. The flat-surfaced device shows a maximum EQE of 68% at 440 nm. However, this EQE rapidly decreases with increasing wavelength because the longer wavelength light is absorbed far below the surface than that of the shorter wavelength light. Carriers generated deep in the substrate require a longer diffusion path in order to reach the junction for carrier separation. Therefore, this results in low separation efficiency and low EQE due to higher carrier recombination rates. Devices with nanostructured surfaces exhibit improved EQE performance throughout the entire wavelength range. This enhancement in EQE is even more significant at longer wavelengths and is attributed to the antireflective effect and the

decoupling of light absorption and charge-carrier collection directions, thus allowing efficient charge transport and high light-harvesting capabilities. To make our argument more clear, the optical reflectance spectra of the nanostructured and flat surface Si after coating with the PEDOT:PSS are shown in Figure 5b. When comparing the EQE and reflectance spectra side by side, it is clear that antireflection effect indeed is the predominant reason for the EQE enhancement. The device made at the spin-coating rate of 7000 rpm achieves the most conformal morphology, exhibiting an EQE above 70% over a wide wavelength range (i.e., between 400 and 850 nm). This particular device also displays the lowest reflectance throughout the entire wavelength range (Figure 5b). In Figure 5c we show the enhancement ratios in EQE and light absorption between the flat device and device made at a spin-coating rate of 7000 rpm. Note that the enhancement ratio in EQE is significantly higher than that of the light absorption at longer wavelengths. This indicates that the efficiency improvement is not only due to antireflective effect but also attributed to higher carrier collection efficiency at longer wavelengths. The enhanced carrier collection efficiency at long wavelength can be explained by the following reason. The scattering from the surface nanostructures increases the optical path length inside the silicon and also makes the light propagate laterally. This results to the enhanced absorption of long wavelength photons near the surface (light trapping effect) than that of the flat surface.<sup>13,21</sup> Therefore, the device with nanostructures shows enhanced response at the longer wavelengths of the spectrum. This result indicates that the antireflective effect is no longer sensitive to the wavelength of incoming light. Surface nanostructures, along with the light trapping effect at long wavelengths, lead to the electron-hole pair generation near the surface that is easier to collect, thus resulting in high EQE.

Although our hybrid solar cells fabricated at 7000 rpm on the NS2 surface structure show efficient PCE because of the high  $J_{scr}$  the  $V_{oc}$  values from the aforementioned devices are still lower than that of other reports.<sup>13–16</sup> The decrease in  $V_{oc}$  can be attributed to following reasons: (a) the low grade silicon wafers (with shorter carrier lifetimes) used in the experiments,

(b) the increased interface area between the polymer and  $Si_{,}^{13}$  and (c) the air voids between the interfaces. (b) and (c) both lead to high surface recombination.

The Si surface becomes hydrophobic after HF cleaning, thus reducing the adhesion of polymer on Si. We attempted to improve the adhesion of the polymer on Si by using a wetting agent (i.e., Triton X-100).<sup>16</sup> Figure 6 shows the J-V characteristics of the two devices that have additional spin-coatings of 1% and 0.5% Triton X-100 at 7000 rpm before PEDOT:PSS deposition. Compared with a device without a wetting agent, the  $J_{\rm sc}$  of the devices with wetting agents are almost unchanged; however,  $V_{\rm oc}$  was slightly increased because the improvement of adhesion, and the FF was slightly reduced due to the nonconductive material involved, resulting in higher resistance. The PCE of the device treated with a 0.5% Triton X-100 wetting agent further improves from 8.70% to 8.84%.

We summarize the performances of devices made on NS2 structures and a flat surface in Table 1. Our best results show an

# Table 1. Photovoltaic Properties of the Hybrid Si flat andNS2 Nanostructure Solar Cells

	$V_{ m oc} \ ({ m mV})$	$J_{\rm sc}$ (mA/cm <sup>2</sup> )	FF (%)	PCE (%)	$\stackrel{R_{ m series}}{(\Omega \cdot  m cm^2)}$
flat	496	19.3	69.1	6.59	2.36
1000 rpm	391	21.8	65.6	5.60	1.09
3000 rpm	401	27.6	70.3	7.78	0.65
5000 rpm	417	27.5	70.0	8.01	0.64
7000 rpm	424	30.6	67.1	8.70	0.42
1% X-100	461	30.3	57.4	8.03	1.65
0.5% X-100	442	30.5	65.5	8.84	1.21

increase in  $J_{\rm sc}$  and the conversion efficiency by 58% and 34.1% (from 6.59% to 8.84%) with optimized solar cell structures. We believe that improvements in  $V_{\rm oc}$  by using better metal contact and reducing surface recombination can advance the performance of polymer/silicon hybrid solar cells further.

#### 4. CONCLUSIONS

We demonstrated the implementation of a PEDOT:PSS/Si solar cell that has a PCE of 8.84% and  $J_{sc}$  of 30.5 mA/cm<sup>2</sup>. The nanostructures on the Si surface that was fabricated by using CsCl self-assembly and dry etching provide enhanced absorption and radial junction architecture. The front metalelectrode shadow ratio, spin-coating rate, and surfactant addition were also adjusted properly to achieve the best device performance. Nanostructures created by using CsCl selfassembly and dry-etching not only have the general advantages of self-assembly such as low cost and high throughput where an entire wafer can be patterned at a time but also possess unique superior qualities: wide tunable/controllable range of diameter and spacing by varying film thickness, relative humidity, and developing time. Furthermore, CsCl can be easily removed with water so that it does not leave behind any contaminants. Other than that, surface nanostructures cause high light absorption; thus, the device requires only a thin Si substrate, which can further reduce the cost of the solar cells. This combined technique provides a simple, scalable, and cost-effective process for the fabrication of efficient hybrid solar cells.

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#### **Author Contributions**

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

# Notes

The authors declare no competing financial interest.

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