Low-Temperature Polycrystalline-Silicon Tunneling Thin-Film Transistors With MILC

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***Abstract*— It is known that metal-induced lateral crystallization (MILC) thin-film transistors (TFTs) exhibit higher on-state current, steeper subthreshold slope, and lower minimum leakage than solid-phase-crystallization TFTs. In this letter, we propose a tunneling TFT (T-TFT) fabricated by MILC method for the first time. The MILC T-TFTs demonstrate a lower subthreshold swing, ∼232 mV/decade, than the other T-TFTs and a high ON/OFF ratio $>10^6$ at $V_{DS} = 1$ V without any hydrogen-related plasma treatment. These improvements can be due to the reduction of defects at grain boundaries and the channel direction parallel to grains. The polycrystalline silicon T-TFTs fabricated in this letter show a great promise for low standby power circuits, drivers of active-matrix liquid crystal displays, and 3-D integrated circuits applications in the future.**

***Index Terms*— Metal-induced lateral crystallization (MILC), poly-Si thin-film transistor (poly-Si TFTs), tunneling field-effect-transistor (TFET).**

I. Introduction

RECENTLY, tunneling field-effect-transistors (TFETs) have received considerable attention for their potential to replace conventional metal–oxide–semiconductor field-effect transistors (MOSFETs) for future low-power applications [1], [2]. Through band-to-band-tunneling (BTBT) carrier transport mechanism, T-FETs can achieve a steep subthreshold slope, below 60 mV/decade at room temperature [2], [3]. When applying negative gate bias on an n-type T-FET, the off-state leakage is well suppressed due to a large barrier for both tunneling and thermionic emission. As the gate bias increases, an electron inversion layer can be induced, which narrows the tunneling barrier between the source/channel regions and allows BTBT.

For single crystalline Si (sc-Si) TFETs, the drive current is generally much lower than that of conventional MOSFETs due to their relatively high bandgap and consequent low tunneling probability [4]. Even for TFETs with a double-gate structure and 4 GPa of stress, the on-current is still an order of magnitude lower than that of low-power MOSFETs [5].

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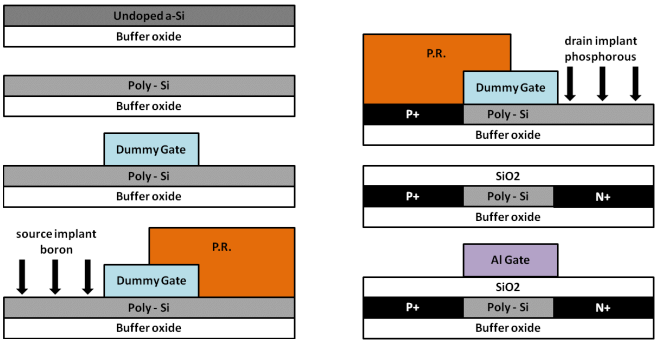

Fig. 1. Key process flows of the T-TFTs.

As technology requirements increase, there is a dramatic increase in the number of publications discussing the various designs to improve the drive current by means of using low bandgap materials, heterojunction channels [2], novel structures [6], and pocket implantation with dopant-segregation technique at the source region [3]. The issues with respect to theories, models, and process innovations of sc-Si TFETs have received considerable attention in the literature. In contrast, there are few studies of polycrystalline-Si tunneling TFTs (T-TFTs), which have only focused on the devices crystallized by excimer-laser annealing (ELA) [7], [8] or by the sequential lateral solidification (SLS) growth technique [9].

To further improve the tunneling current and to obtain a steeper subthreshold slope of the devices, T-TFTs and conventional TFTs fabricated with metal-induced lateral crystallization (MILC) method on the same wafer are demonstrated and characterized in this letter for the first time. The enhanced on-state performance is obtained due to trap-assisted tunneling and field emission from traps [10]. An ON/OFF ratio of six orders and a record low subthreshold swing of T-TFT are achieved without hydrogen-related plasma treatment.

II. Experimental Methods

The process flow of the T-TFT is shown in Fig. 1. A *p*-type Si wafer capped with a 550-nm wet oxide layer is used as a starting substrate. A 70-nm-thick amorphous-Si layer is deposited by low-pressure chemical vapor deposition at 500 °C as channel film. A 5-nm Ni film is then deposited by an electron-beam evaporation system and patterned by a liftoff process. The remaining Ni film is used as a seed layer for the MILC process. The channel film is crystallized at 550 °C in N_2 ambient for 24 h by the MILC method.

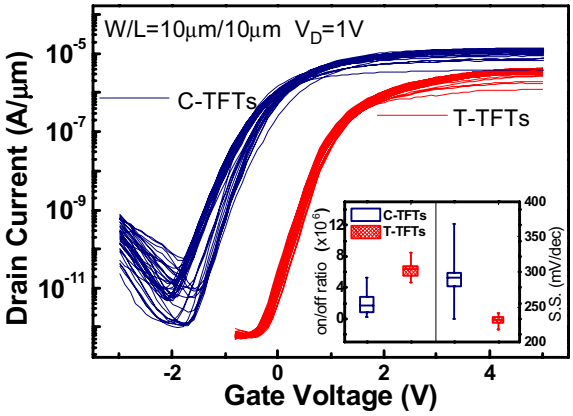

Fig. 2. Transfer characteristics of T-TFTs and C-TFTs.

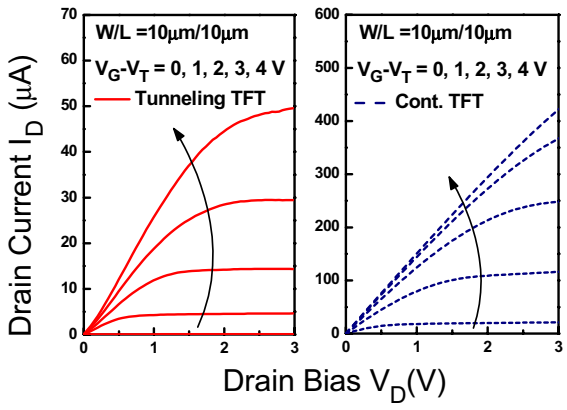

Fig. 3. Output characteristics of (left) T-TFTs and (right) C-TFTs.

The active region is defined by an i-line stepper and patterned by anisotropic selective dry etching. A 200-nm SiO_2 dummy gate is formed to block unnecessary implanted dopant from the channel region beneath the oxide dummy gate. The T-TFTs are implanted using boron and phosphorous with a dose of 5×10^{15} cm^{-2} as source and drain, and are annealed at 600 °C in N_2 ambient to activate the dopants after dummy gate removal. Simultaneously, a control TFT (C-TFT) is fabricated on the same wafer with only phosphorous doping. A 30-nm gate oxide is then deposited by electron-beam evaporation. Afterward, aluminum metallization is used as source/drain contact and gate electrode. The cross-sectional view of the T-TFT is shown in Fig. 1.

III. Results and Discussion

The transfer characteristics of 40 T-TFTs and 40 C-TFTs are shown in Fig. 2. The T-TFTs show a tight distribution while the C-TFTs show a diverse one. A significant improvement in off-state leakage is obtained because of the large barrier for field emission. Although a subthreshold swing of sub-60 mV/decade is not observed, the T-TFTs reached its record low subthreshold slope (232 mV/decade). The comparisons of the device parameters for different T-TFTs [7]–[9] are listed in Table I. The SS degradation is primarily due to trap-assisted tunneling and is confirmed by activation energy extraction. To further improve the subthreshold characteristics, geometry optimization must be carried out to enhance the efficiency of BTBT. This may include introducing a gate-on-source-only structure [6], [11] or dual-gate electron-hole-bilayer operation [12].

Fig. 3 shows the output characteristics of the T- and C-TFTs, respectively. The drive current of the T-TFTs is about an order lower than the C-TFTs owing to the relatively large band-gap of silicon and the low tunneling effective mass, which lowers the tunneling efficiency, as mentioned above [4]. The on-state current of a general sc-Si TFET is well below that of a sc-Si MOSFET. The current drive of sc-TFETs is usually approximately two to three orders lower than that of the MOSFETs. The current drive of T-TFTs is only an order lower than that of C-TFTs due to the trap-assisted tunneling and field emissions from

	This Work		Ref. [7]	Ref. [8]	Ref. [9]
Method of Crystallization	MILC T-TFT	MILC C-TFT	ELA T-TFT	ELA T-TFT	SLS T-TFT
Channel Length (μm)	10	10	0.2	1	5
Channel Film Thickness (nm)	70	70	100	20	50
Average S.S. (mV/dec.)	232	297	> 2500	~ 400	> 3000
I_{OFF} (pA/μm)	0.59 V_{DS}=1V	10.82 V_{DS}=1V	< 10 V_{DS}=3.2V	< 0.1 V_{DS}= 3V	< 3 V_{DS}= -4V
On/Off Ratio	6.1×10^6 V_{DS}=1V	3.6×10^6 V_{DS}=1V	~ 10^6 V_{DS}=3.2V	> 10^9 V_{DS}= 3V	~ 10^6 V_{DS}= -4V

TABLE I
Comparison of Several Important Parameters of the T-TFTS With Previous Studies

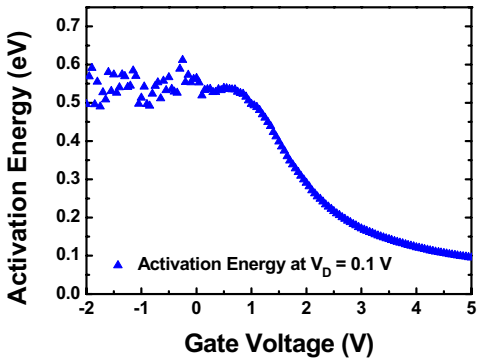

Fig. 4. Activation energy of the T-TFT versus the gate bias.

traps. Residual nickel atoms are trapped at the needle-like grain boundaries and became deep level states after MILC processing [13].

To differentiate other conduction mechanisms from BTBT, temperature-dependent transfer characteristics are measured at $V_D = 0.1$ V, and the activation energies are then extracted. Fig. 4 shows the activation energy of the T-TFTs at $V_D = 0.1$ V plotted against V_G. Three different gate bias ranges can be distinguished corresponding to different transport mechanisms. When applying negative gate voltage, the T-TFTs are operated in the off-state. Several possible mechanisms

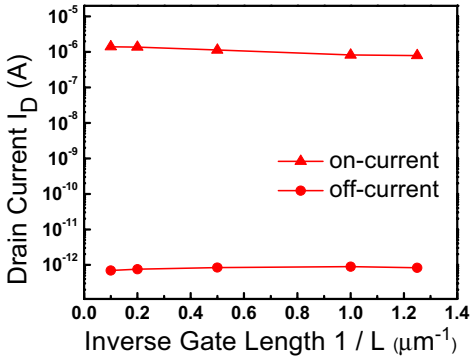

Fig. 5. ON/OFF current as a function of the gate length at $V_D = 0.1$ V. Channel width is 10 μm.

exist for the leakage current: thermionic emission over source-drain builtin potential, Shockley–Read–Hall generation in the heavily doped region, and reverse tunneling at the drain region. The activation energy is ~0.55 eV in the negative gate bias region. These values are approximately half the values of the silicon bandgap, which indicated that Shockley–Read–Hall generation dominates [14]. As gate bias increased, the activation energy decreased slowly and finally reached 0.10 eV at $V_G = 5$ V. The relation between tunneling current and electric field can be described as follows:

$$J_{BTBT} = \left(\frac{\sqrt{2m^*}q^3 E_s V_s}{8\pi^2 \hbar^2 E_g^{0.5}}\right) exp\left(\frac{-4\sqrt{2m^*}E_g^{1.5}}{3qE_s\hbar}\right)$$

where m^* is the reduced effective mass, E_g is the bandgap of silicon, $\hbar$ is the reduced Planck constant, and E_S and V_S are the maximum field and reverse bias at the junction, respectively [4]. According to this model, the BTBT current is associated with the bandgap and the effective mass. The rather small temperature-induced bandgap narrowing of silicon contributes to weak temperature dependence of the BTBT current and leads to an activation energy of only 0.10 eV [14]. It must be further noted that an activation energy of 0.3–0.5 eV is extracted at the subthreshold region. These values are commonly due to trap assisted tunneling and emission from traps [14], which may be also responsible for the degradation of the subthreshold slope. This result suggests that the T-TFTs should be optimized by a gate with stronger electrostatic control and/or a tunneling junction aligned with the applied field.

The dependence of the ON/OFF current on the channel length can be seen in Fig. 5. The drive current and off-leakage for sc-Si TFET are nearly independent of the gate length [4]. The invariant drive current is also found in T-TFTs because tunneling current dominates at on-state. On the other hand, the off-leakage remains ~0.1 pA/μm from $L = 10$ μ to 0.8 μm, corresponding to the reverse bias diffusion leakage of a p-i-n diode. Therefore, a large ON/OFF ratio can be well sustained even after length scaling.

IV. Conclusion

In conclusion, poly-Si T-TFTs were fabricated and characterized successfully for the first time. The T-TFTs with MILC channels showed high tunneling current, low off-leakage, steep subthreshold swing, and large ON/OFF ratio. A sub-60-mV/decade subthreshold slope was not achieved owing to trap-assisted tunneling, which was examined with the activation energy. To improve the subthreshold characteristics, the T-TFTs should be geometrically and electrically optimized to enhance the efficiency of BTBT. These devices will be suitable for the application in low standby power circuits, as drivers of active-matrix liquid crystal displays, and as 3-D integrated circuits in the future.

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