Channel Thickness Effect on High-Frequency Performance of Poly-Si Thin-Film Transistors

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***Abstract*— In this letter, we present the high-frequency performances of polycrystalline silicon (poly-Si) thin-film transistors (TFTs) with a nominal gate length of 0.22 μm. Owing to the short gate length and adoption of salicide process, cutoff frequency (f_T) of 17 GHz and maximum oscillation frequency of ~21 GHz are obtained. The result suggests that the poly-Si TFT technology is applicable to RF integrated circuits up to 2 GHz. In addition, we also investigate the effects of channel thickness on the high-frequency characteristics of poly-Si TFTs. We find that the variation of f_T with channel thickness is mainly due to the change in transconductance.**

***Index Terms*— Channel thickness, gate length, radio frequency, thin-film transistors (TFTs), transconductance.**

I. Introduction

POLYCRYSTALLINE silicon (poly-Si) thin-film transistors (TFTs) were extensively studied for applications to large area and 3-D electronics [1]–[4]. Nonetheless, a few researches were reported on studying the high-frequency characteristics of poly-Si TFTs [5]–[7], owing to their relatively low mobility as compared with the bulk Si counterparts, as well as the rather large device size even in state-of-the-art manufacturing (e.g., channel length >3 μm). With low-temperature processes, the electron mobility of poly-Si TFT can reach 260 $cm^2/V{\cdot}s$ [8]. In addition, by properly shrinking the dimensions of TFTs, the device's RF performance is expected to improve significantly. From 2-D numerical simulation, the cutoff frequency of poly-Si TFTs can be as high as 40 GHz when the gate length is scaled down to 0.2 μm [9]. It demonstrates that the poly-Si TFT technology is feasible for low-cost RFIC applications such as RF identification and RF modules integrated on display panel. In this letter, we experimentally explore the high-frequency characteristics of poly-Si TFTs with different channel layer thicknesses. Cutoff frequency (f_T) of 17 GHz and maximum oscillation frequency (f_{max}) of ~21 GHz are achieved, which are much higher than those reported in [5]–[7]. In addition, we also analyze the variations of f_T and f_{max} with channel thickness in terms of the transconductance, gate capacitance, and channel resistance.

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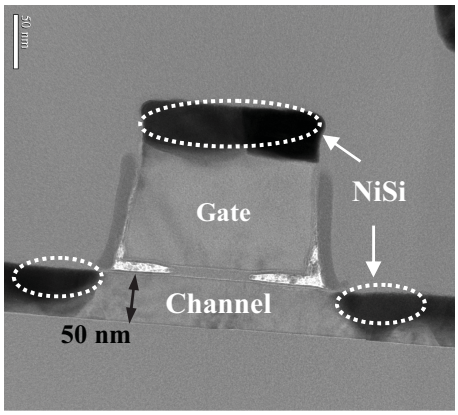
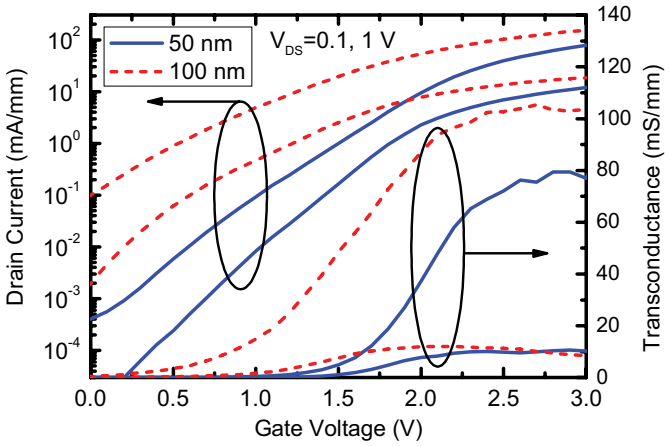


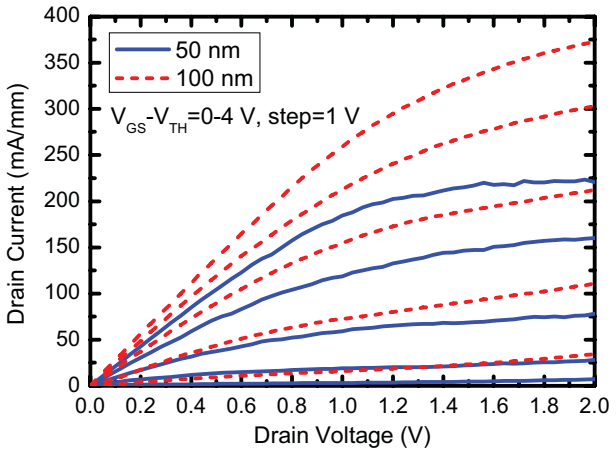
Fig. 1. Cross-sectional TEM image of an *n*-type poly-Si TFT.

II. Device Fabrication

First of all, a wet oxide with thickness of 1 μm is formed on a 6-in silicon substrate as the buried oxide. An amorphous silicon (α-Si) layer is then deposited with low-pressure chemical vapor deposition to serve as the channel layer. The channel thickness is either 50 or 100 nm. Solid-phase crystallization (SPC) method, which is performed at 600 °C in N_2 ambient for 24 h, is then used to transform the film from α-Si into poly-Si to promote the electron mobility. After forming the active region, a 10-nm tetraethyl orthosilicate (TEOS) oxide and a 100-nm *in situ* n^+ poly-Si are deposited as the gate dielectric and gate electrode, respectively. Afterward, the gate is defined by a photolithographic step and etched by reactive ion etching. Sidewall spacers are formed with an 8-nm TEOS oxide layer and a 15-nm nitride layer. To reduce the parasitic source and drain (S/D) resistances, a 15-nm nickel layer is first deposited and consecutively annealed to form NiSi on the gate and S/D regions. Afterward, S/D regions are doped by a self-aligned P_{31}^+ ion implant at 10 keV. A vacuum anneal at 600 °C for 30 min for activation took place at this stage. The implant-to-silicide technique is used to minimize the dopant diffusion from S/D region into the channel. Finally, a standard back-end process is performed to form metal connections. The cross-sectional transmission electron microscopy (TEM) image of an *n*-type poly-Si TFT is shown Fig. 1. The gate length is ~0.22 μm.



(a)



(b)

Fig. 2. (a) Transfer and (b) output characteristics of poly-Si TFTs with channel thicknesses of 50 and 100 nm.

III. Results and Discussion

The dc characteristics of n-type poly-Si TFTs with nominal gate length of 0.22 μm are shown in Fig. 2. The threshold voltages and subthreshold slopes at drain voltage $V_{DS} = 0.1$ V are 1.75 V and 240 mV/decade, respectively, for the device with 50-nm channel thickness, while they are 1.28 V and 270 mV/decade for the device with 100-nm channel thickness. Better gate controllability and less short-channel effect in devices with thinner channel layer are primarily due to the reduction in junction depth [10]. In contrast, the device with thicker channel layer exhibits higher drain current and transconductance. One of the reasons is its higher effective channel mobility (76 $cm^2/V{\cdot}s$) compared with the thin-channel device (64 $cm^2/V{\cdot}s$). In poly-Si, the grain boundaries can form charge trapping sites that are capable of creating a potential barrier, leading to the reduction of the effective channel mobility. The charge trap densities of thin and thick channels, extracted by Levinson's grain boundary trapping model [11], are 6.8×10^{12} and 4.3×10^{12} cm^{-2}, respectively. Lower charge trap density in thick-channel device is probably due to the larger grain size than that in thin-channel device after the SPC process [12]. From the SEM analyses performed on samples treated with Secco etching (data not shown), the grain sizes are ~25 and 45 nm, respectively, for 50- and 100-nm-thick films. Another possible reason for the higher current drivability in thick-channel device is its lower S/D resistance. Through plotting the on resistance measured from the linear region of output characteristics versus gate length, we can extract the S/D resistance roughly [13]. The extracted S/D resistances of thin- and thick-channel devices are ~2.4 and 1.8 $\Omega{\cdot}$mm, respectively. Though the NiSi depths are similar in devices with different channel thicknesses, the fully silicided S/D region in 50-nm channel device (from TEM image) would suffer from additional current crowding effect [14], [15] and thus increase the S/D resistance. Our results suggest that, to obtain better current drivability and RF performance, the channel thickness needs to be increased. It should be, however, careful to keep the leakage current at a reasonable level when increasing the channel thickness. To address this issue, excimer laser annealing method [16] can be used instead of the SPC scheme to improve the crystallinity of the poly-Si and accordingly reduce the leakage of the fabricated devices.

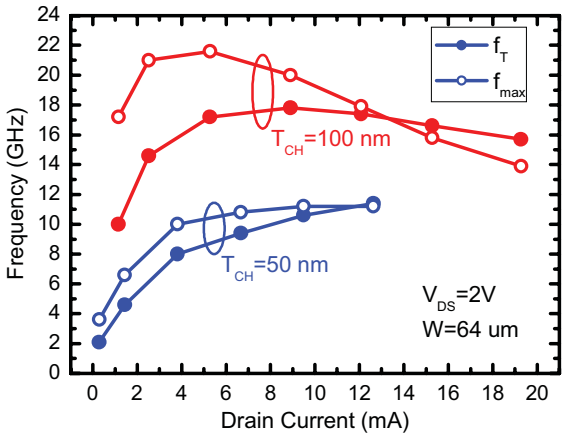


Fig. 3. Cutoff frequency and maximum oscillation frequency of poly-Si TFTs with different channel thicknesses (T_{CH}).

To examine the high-frequency performances of poly-Si TFTs, S-parameters are measured on chip from 100 MHz to 20 GHz. The devices under test have a multifinger gate configuration featuring eight fingers with a total width of 64 μm. The nominal gate length is 0.22 μm. After de-embedding the parasitic pad effects from measured S-parameters, the ac current gain (H_{21}) and unilateral power gain (U) are calculated to extract f_T and $f_{\max}$, respectively. As shown in Fig. 3, the device with 100-nm channel layer exhibits higher f_T and $f_{\max}$ compared with those with 50-nm channel layer. In addition, the peak f_T and $f_{\max}$ are obtained at a lower drain current for thick-channel device, showing that the dc power dissipation could be lower in the thick-channel device. Therefore, better high-frequency performances could be achieved in poly-Si TFTs with a thicker channel layer. The peak f_T and $f_{\max}$ are 17 and 21 GHz, respectively, for devices with a channel thickness of 100 nm, implying that the poly-Si TFT technology has a potential for RF applications up to 2 GHz.

Generally, the cutoff frequency is given by $g_m/2\pi(C_{gs} + C_{gd})$, where g_m is the transconductance, C_{gs} is the gate-source capacitance and C_{gd} is the gate-drain capacitance. Thus, we extract g_m, C_{gs}, and C_{gd} from two-port admittance

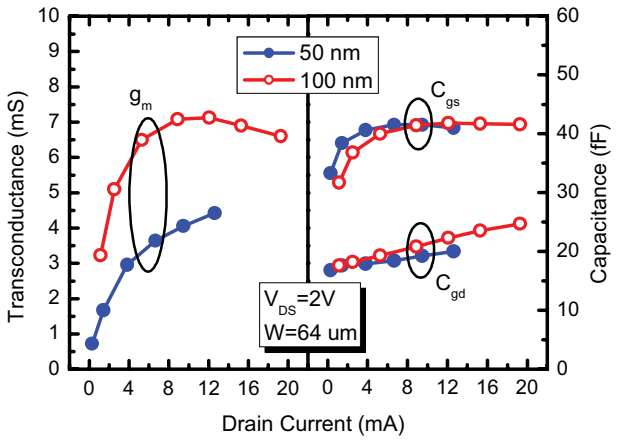


Fig. 4. Extracted transconductance and gate capacitances of poly-Si TFTs with different channel thicknesses.

parameters [17] to study the dependence of f_T on channel thickness. The results are shown in Fig. 4. The transconductance of poly-Si TFT increases with increasing channel layer thickness, whereas the gate capacitances are nearly unchanged. Hence, the variation of f_T with channel thickness is mainly due to the change in g_m. The enhancement of peak f_T is 56% when the channel thickness is changed from 50 to 100 nm, closing to the peak g_m enhancement (∼61%). In Fig. 3, we also observe that the maximum oscillation frequency is higher than the cutoff frequency at low drain currents for both devices. It, however, decreases more rapidly with increasing gate biases and eventually becomes lower than the cutoff frequency at high drain currents. This is because C_{gd} increases and the channel resistance decreases gradually with increasing gate biases.

IV. Conclusion

High-frequency characteristics of poly-Si TFTs with different channel thicknesses were investigated. With short gate length (∼0.22 μm) and salicide process, high current drivability and transconductance were obtained. Because the device with a thicker channel exhibited larger grain size, its drain current and transconductance were higher than those of thin-channel devices. Better high-frequency performance was also achieved for the device with thicker channel layer owing to the higher transconductance. Finally, the poly-Si TFT with a channel thickness of 100 nm exhibited cutoff frequency of 17 GHz and maximum oscillation frequency of ∼21 GHz, suggesting that the poly-Si TFT technology was applicable to RF integrated circuits up to 2 GHz.

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