Advanced TSV-Based Crystal Resonator Devices Using 3-D Integration Scheme With Hermetic Sealing

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***Abstract*— An advanced crystal resonator device scheme using Cu through-silicon via (TSV), 3-D integration, and Si packaging technologies is successfully demonstrated. In addition to robust structural quality, the crystal resonator packaging has excellent electrical characteristics of low leakage current and reliability against harsh environment for MIL-STD-883 hermetic encapsulation. Using 3-D integration technologies and Si packaging, the proposed TSV-based crystal resonator device possesses the manufacturability potential while conventional ones using a metal lid or ceramic enclosure.**

***Index Terms*— 3-D integration, crystal resonator through-silicon via (TSV).**

I. Introduction

THREE-dimensional integration technology provides a platform for multifunctional integration and has been developed to extend Moore's law over the past few years. This technology scheme possesses advantages such as small form factor, high performance, and low power consumption [1], [2]. In addition, 3-D integration is the candidate to facilitate the concept of more than Moore, which includes heterogeneous integration, making the possible connection among different substrates, materials, and functions [3].

Conventional crystal resonator devices are packaged in metal or ceramic vacuum enclosures over the active area of the quartz blank to avoid mechanical attack and protect against moisture and contamination [4]. With these technologies, current crystal resonator can be fabricated with a size of 16 × 2.0 mm The challenges of advanced quartz crystal devices including high manufacturing and material cost and difficulty of scaling down, however, make the development of advanced smaller products (1.2 × 1.0 mm) difficult.

As 3-D integration provides the heterogeneous integration scheme by vertical stacking and through-silicon via (TSV) interconnection with lower power consumption [5]. In this letter we demonstrate TSV-based crystal resonator devices with hermetic sealing and investigate the corresponding electrical characteristics and reliability. Using 3-D integration technologies, this TSV-based crystal resonator device scheme can be an attractive option for future crystal resonator products.

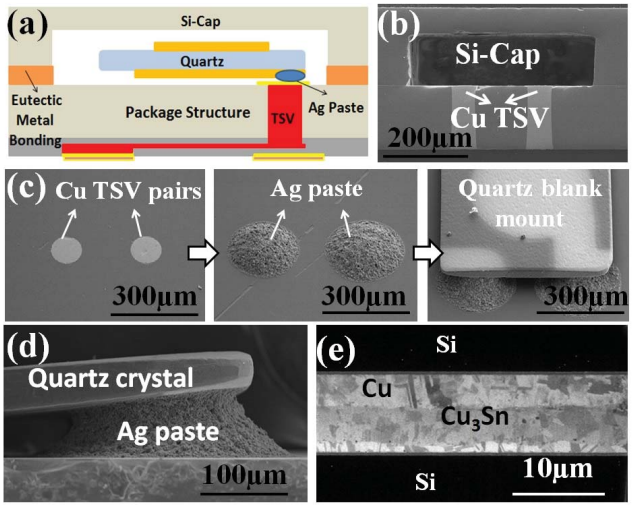

Fig. 1. (a) Schematic diagram of crystal resonator device and package structure. (b) Cross-sectional scanning electron microscopic (SEM) view of package structure. (c) Quartz blank mount process. (d) SEM image of Ag paste between crystal quartz and Cu TSV on Si wafer. (e) Transmission electron microscopic image of bonded interface.

II. Process and Integration Demonstration

The schematic diagram of crystal resonator device (1.2 × 1.0 mm) using 3-D integration technologies is shown in Fig. l(a). A 200 μm-deep cavity in the top Si thinned 300-μm wafer is fabricated by inductive coupled plasma deep reactive-ion etching (DRIE) method Through Cu/Sn bonding, the Si cap wafer is bonded to the thinned bottom 250-μm substrate with Cu TSV, as shown in Fig. l(b). The Cu TSVs with 100-μm diameter and 250-μm depth are formed by DRIE Bosch process, 500-nm oxide liner from plasma enhanced chemical vapor deposition, 15-nm TiN barrier/300-nm Cu seed layer deposition, and Cu electrochemical deposition (ECD) with Cu CMP process for overburden removal.

After Cu TSV fabrication redistribution metal level is fabricated on the backside, whereas on the front side 4-μm Cu

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and 2-μm Sn are sequentially deposited by ECD to form metal structure for later bonding process. Then, 100-μm-height Ag paste from TXC Corporation is applied on Cu TSV to attach crystal quartz and then cured at 200 °C for 2 h in vacuum, which is the so-called quartz blank mount process, as shown in Fig. 1(c) and (d). The Ag paste is not only to support and conduct the quartz blank with TSV but also to absorb and reduce the thermal stress near TSV surface because of the flexibility of Ag paste.

To protect the quartz blank from mechanical attack and mass loading effect, the Si cap wafer is Cu/Sn thermal-compression bonded at 300 °C for 30 min with 1.91-MPa bond pressure under vacuum. During bonding, the intermetallic compound of Cu_6Sn_5 is first formed, followed by the formation of the Cu-rich Cu_3Sn from the interdiffusion of Cu and Cu_6Sn_5 [6]. As shown in Fig. 1(e) with EDX analysis results, Cu_3Sn phase is formed without the presence of voids or seams in the bonding joints showing good bonding integrity in this integration scheme. In addition, the absence of Sn phase suggests that Sn is completely consumed by the formation of intermetallic compound during the thermo-compression process, only Cu/Cu_3Sn left with high melting point.

With the above integration scheme, crystal resonator devices using 1.2 × 1.0 mm package size is successfully fabricated with Cu TSV for the connection of the signal electrode on the quartz blank and is well protected mechanically and hermetically by Cu/Sn eutectic bonding.

III. Electrical Investigation of Cu TSV and Crystal Resonator Package

Fig. 2(a) and (b) shows the IEC441-1 measurement method [International Electrotechnical Commission (IEC)] and the Butterworth-Van Dyke equivalent circuit for measurement of crystal resonator devices, including TSV and crystal quartz. Quartz center frequency of 47892311.2 Hz is used for electrical investigation.

The components of C_1, L_1, and R_1 represent the mechanical behavior of the crystal element, whereas C_0 represents the electrical behavior of the crystal element and package [7]. The shunt capacitance (C) for TSV-based crystal resonator device package by IEC444-1 method is shown in Fig. 2(c). The value of shunt capacitance (C) can be measured at the frequency <1 MHz. Practically, C_0 includes not only the static capacitance of plated quartz blank, but also the capacitance of Ag conductive and the capacitance of housing itself. The average shunt capacitance of TSVbased package is ~2 pF and reasonable for real applications.

The measurement results of motional resistance (R_1) of crystal resonator devices from conventional ceramic package and TSV based silicon package are shown in Fig. 2(d). These results also represent the real resistive and mechanical losses from the crystal resonator and the whole package. The average motional resistance is 280 Ω for TSV-based crystal resonator package and 1.4 kΩ for ceramic package, respectively. With the smaller mechanical and energy loss than the conventional ceramic package, the TSV-based crystal resonator device shows the potential in the advanced applications.

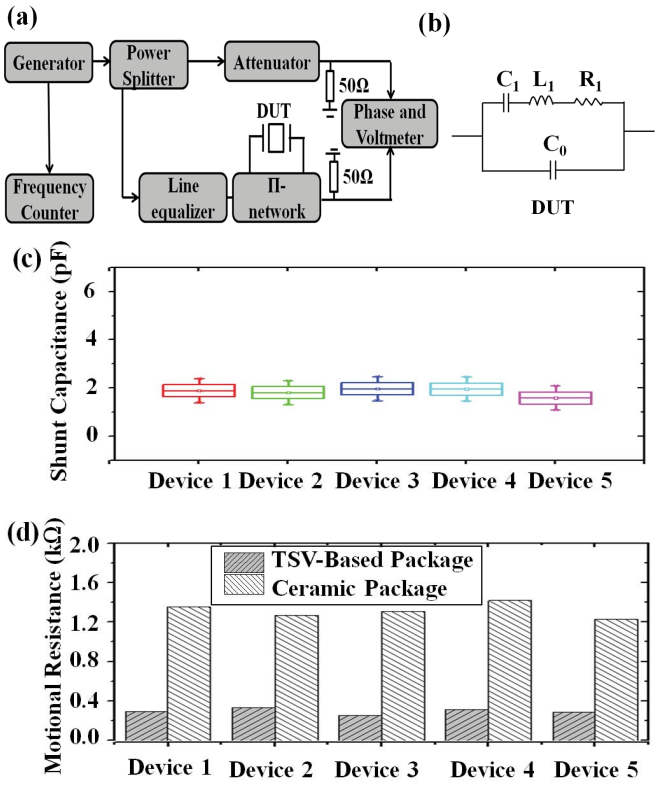


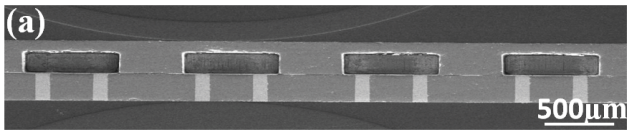
Fig. 2. (a) IEC441-1 measurement method. (b) Butterworth-Van Dyke equivalent circuit for crystal resonators. (c) Capacitance measurement results of TSV-based crystal resonator device package. (d) Resistance measurement results of TSV-based and ceramic crystal resonator package.

IV. Hermetic and Reliability Investigation

The wafer-level integration of the TSV-based Si substrate and the Si cap wafer is successfully shown in Fig. 3(a) MIL-STD-883 hermetic encapsulation test is applied on the whole package with TSVs to evaluate the thermal reliability of Cu/Sn joints and the electrical stability of TSV-based package. Crystal resonator devices are placed in a chamber filled with helium gas at 0.5 MPa for at least 2 h (helium bombing). As shown in Fig. 3(b), the novel TSV-based package passes the MIL-STD-883 hermetic encapsulation test after different thermal flow processes (8.5×10^{-9} to 1×10^{-8} Pa m^3/s by a He leak detector) [8], which shows the Cu/Sn bonded structure with good bonding quality against temperature variation.

Electrical leakage performances of TSV-based crystal resonator device before and after the serial thermal process flow are shown in Fig. 3(c), showing that the leakage currents of TSV-based device are <0.1 nA from 15 to −15 V. The results also show that the crystal resonator device using 3-D integration technologies under the large difference of coefficient of thermal expansion between Cu and Si still exhibits an excellent electrical performance.

In addition the reliability of TSV-based crystal resonator device is investigated at 45 °C and 100% relative humidity, which are the criteria for current resonator devices. Fig. 3(d) shows the leakage currents of TSV-based crystal resonator device are <0.1 nA before and after 2 h in this humidity



(b)

Thermal Flow Process	Hermetic Encapsulation Test
Before Thermal Flow	Pass
Curing Oven & Annealing	Pass
Aging & Reflow	Pass

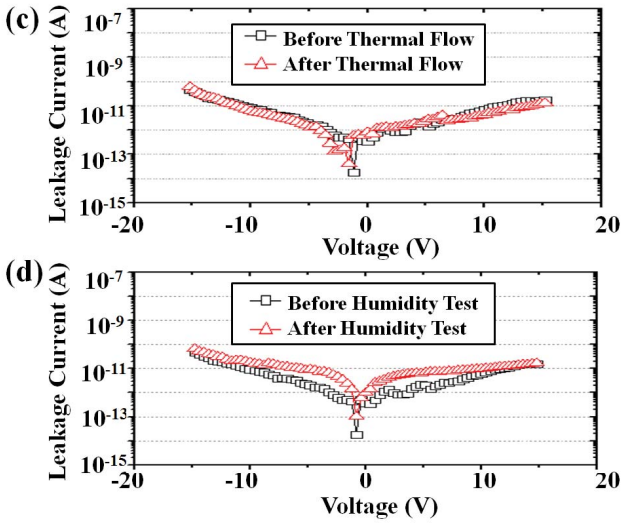


Fig. 3. (a) Cross-sectional image of wafer-level bonded Si cap and TSV-based structure. (b) Results of MIL-STD-883 hermetic encapsulation test with thermal flow processes; electrical leakage characteristics of TSV-based crystal resonator device. (c) Before and after thermal flow process. (d) Before and after humidity process.

environment The stable electrical characteristic results show that the TSV-based crystal resonator device has good electrical reliability against moisture and corrosion.

Overall, this TSV-based crystal resonator package using 3-D integration is developed and investigated on its electrical, hermetic characteristics and reliability. In addition, with the robust strength without the leakage path, the TSV-based crystal resonator devices using 3-D integration has the potential for future advanced products.

V. Conclusion

We demonstrated crystal resonator devices using Cu TSV, hermetically bonding, wafer thinning, and Si packaging. The framework of design was different from the conventional one. With the optimum design and fabrication parameters, excellent electrical and mechanical performances can be achieved in this small TSV-based crystal resonator device for the advanced product requirement based on 3-D integration technologies.

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