AIP Applied Physics Letters

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Citation: Applied Physics Letters **103**, 053515 (2013); doi: 10.1063/1.4812669
View online: http://dx.doi.org/10.1063/1.4812669
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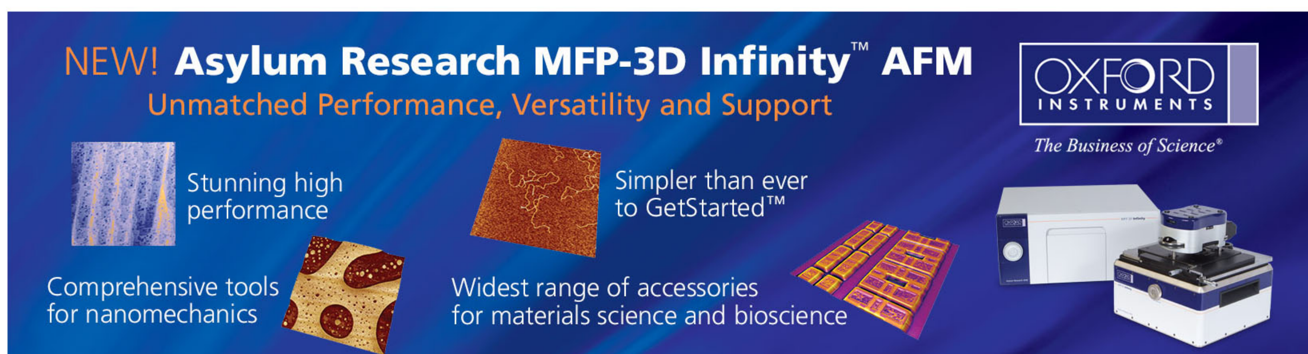

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Effects of crystallization mechanism on the electrical characteristics of green continuous-wave-laser-crystallized polycrystalline silicon thin film transistors

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(Received 6 March 2013; accepted 16 June 2013; published online 2 August 2013)

Thin film transistors (TFTs) with amorphous silicon films crystallized via continuous-wave green laser at a wavelength of 532 nm exhibit very different electrical characteristics in various crystallization regions, corresponding to the Gaussian energy density distribution of the laser beam. In the center region subjected to the highest energy density, the full melting scheme led to the best crystallinity of the polycrystalline silicon film, resulting in the highest field-effect mobility of 500 $cm^2 V^{-1} s^{-1}$. In contrast, the edge region that resulted in solid phase crystallization exhibited the worst mobility of 48 $cm^2 V^{-1} s^{-1}$ for the polycrystalline silicon TFTs. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4812669]

Recently, low-temperature polycrystalline silicon technology has attracted increasing attention for applications in high-performance active-matrix liquid crystallized displays (AMLCDs)[1,2] and three-dimensional integrated circuits (*3D-ICs*).

Various grain enhancement technologies, including solid-phase crystallization (SPC),[3] metal induced crystallization (MIC),[4] excimer laser crystallization (ELC),[5–10] and continuous-wave (CW) laser crystallization,[11–18] have been proposed to crystallize amorphous silicon (α-Si) thin films as polycrystalline silicon films at temperatures as low as 600 °C for non-alkali glass substrates. Among these technologies, SPC presents a lot of defects, and the process time was about 24 h at 600 °C. Compared to SPC, MIC was able to reduce process time and temperature, but the polycrystalline silicon films suffered from metal contamination issues. Furthermore, laser crystallization method could produce large-grain polycrystalline silicon film at room temperature, but ELC encounters the polycrystalline silicon grain uniformity problem. Diode-pumped solid-state (DPSS) CW green laser crystallization has been reported to be capable of achieving extremely large polycrystalline silicon grains and a wide laser processing window using a simple process. However, few studies exist in the literature concerning the crystallization mechanism and the resulting transfer characteristics of the polycrystalline silicon thin film transistors (TFTs) using CW laser.

In this letter, a single-scan CW laser beam is utilized to irradiate the α-Si films, and the resulting polycrystalline silicon TFTs exhibit very different electrical characteristics at different irradiation positions. The crystallization mechanism of the α-Si films using CW laser annealing was discussed and proposed.

Initially, a 200 nm-thick α-Si layer was deposited on the quartz wafer. Moreover, the highly hydrogen concentration of α-Si films will ablate from explosive hydrogen evolution during laser irradiation;[19,20] therefore, α-Si layer was deposited by low pressure chemical vapor deposition (LPCVD) system at 550 °C and 350 mTorr with 120 sccm of silane. After the standard RCA cleaning process, the active α-Si layers for the TFTs were then crystallized using the DPSS CW green laser with a wavelength of 532 nm at room temperature. The laser scanning speed and power were 40 mm/s and 3.2 W, respectively. The spot size of the laser beam was 400 μm $\times$ 300 μm with a Gaussian distribution. After laser irradiation, the polycrystalline silicon TFTs whose active regions correspond to different power distributions were then patterned. The device channel was parallel to the scanning direction. Subsequently, a 100 nm-thick TEOS gate oxide and *in situ* phosphorus doped polycrystalline silicon layer with a thickness of 200 nm were sequentially deposited by LPCVD at 550 °C and 350 mTorr. The *in situ* doped polycrystalline silicon layer was then patterned as the gate electrode, followed by self-aligned source/drain phosphorous ion implantation at 40 keV with a dose of 5×10^{15} cm^{-2}. Then, a passivation oxide layer was deposited, and the dopant activation was simultaneously carried out by a thermal annealing for 8 h at 600 °C in furnace with 500 sccm of nitrogen. Finally, the contact hole opening and metallization were completed to fabricate the proposed TFTs.

Fig. 1(a) shows the optical microscopy (OM) image of the single-scan CW laser-beam-crystallized polycrystalline silicon film. From the OM image, the polycrystalline silicon thin film after the laser annealing was dividing into three major regions, the center, transition, and edge regions. The SEM images corresponding to the center, transition, and edge regions are shown in Figs. 1(b)–1(d), accordingly. The structures were found to be in their respective regions, since the energy density of the laser beam appeared to be Gaussian distributed, which were 2 μm $\times$ 20 μm, 1 μm $\times$ 1 μm, and 50 nm $\times$ 50 nm for the center, transition, and edge regions, respectively. In addition, the grain shapes changed from small equiaxial shapes to medium polygonal and large longitudinal morphologies.

To further study the crystallinity of the laser-crystallized polycrystalline silicon films in these three regions, the Raman

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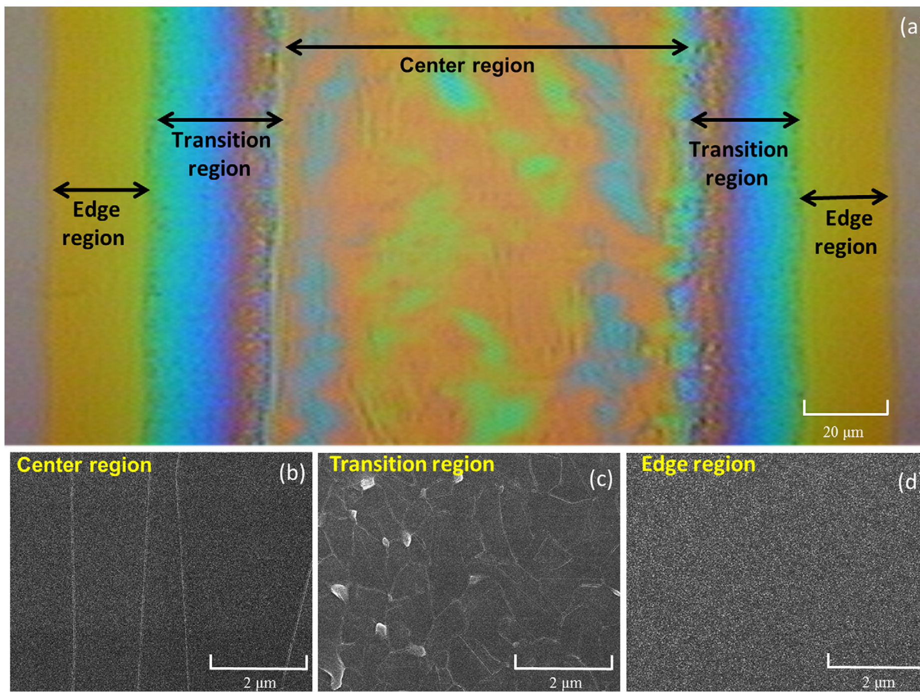

FIG. 1. (a) The OM image of the single-scan CW laser beam crystallized polycrystalline silicon film. Plan-view SEM images of the secco-etched for (b) the center region, (c) the transition region, and (d) the edge region, respectively.

spectra were measured as shown in Fig. 2. The Raman peaks and f*ull width at half maximum* (FWHM) in the center, transition, and edge regions were 513.73 cm^{-1}/5.99 cm^{-1}, 515.23 cm^{-1}/6.66 cm^{-1}, and 519.02 cm^{-1}/7.36 cm^{-1}, correspondingly. Since a smaller FWHM of the Raman peak reflects better crystallization of the silicon film, the polycrystalline silicon crystallinity in the center region was the best among these three regions. In contrast, the edge region exhibited the worst crystallinity and smallest grain size. In addition, the negative Raman peak frequency shift ($\Delta\omega$) indicated that the tensile thermal stress concentrated in the grains and relaxed at the grain boundary after CW laser crystallization.[21,22] Therefore, the full melting subjected to the highest tensile stress, $\Delta\omega$, was $-6.9\,cm^{-1}$ in the center region. On the contrary, the edge region had a low energy density and encountered large grain boundary; hence, much of the thermal stress has been relaxed; $\Delta\omega$ was $-1.2\,cm^{-1}$.

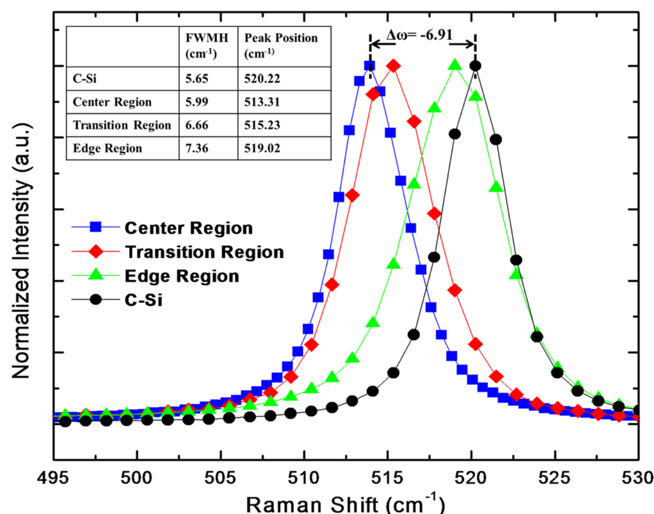

FIG. 2. Raman spectra measured at the three regions of CW laser crystallization polycrystalline silicon and single-crystal Si.

A schematic illustration of the crystallization mechanism is plotted in Fig. 3 for the α-Si films irradiated with the single-scan CW laser. Because the CW laser beam appeared to be Gaussian-shaped, it is possible to define the three-level laser energy density. For the edge region, the lowest energy density led to SPC, which resulted in a small grain size and the worst crystallinity. In contrast, the fully liquid-phase crystallization in the center region exhibited the largest grain size and the best crystallinity. It was also found that at the transition region between the two major regions where partial liquid-phase crystallization occurred, large polygonal grains were also observed.

In the center region with higher energy density, the crystallization direction was the same as the scanning direction because of the strong scanning-direction temperature gradient in the liquid-solid interface. Thus, the post-annealing region acted as the seeds and started to crystallize the α-Si thin film from the center region to the current melting region. In the transition region between the edge and center regions, the grain growth was from partial melting growth (PMG) to super-lateral growth-like (SLG-like)[23,24] from the lower to

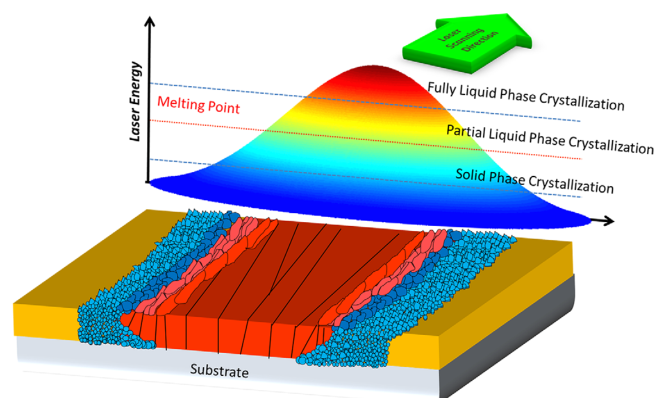

FIG. 3. The laser energy profile for the crystallization of α-Si thin films.

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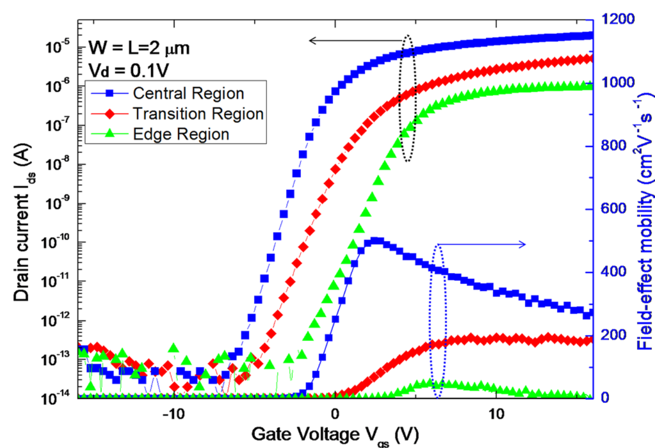

FIG. 4. The transfer characteristics of thin film transistors for center region, transition region, and edge region with width of 2 μm and length of 2 μm.

the higher laser energy position. The un-melted grains at the bottom part of the silicon film acted as the seeds; thus, the grains grew from the bottom to the top of the silicon film. In addition, the SLG-like region near the center region not only crystallized from the bottom seed but also started from the post-annealing region. Therefore, the grains changed from small equiaxial shapes to medium polygonal morphologies from the PMG region to the SLG-like region. In the edge region with lower energy density, the laser energy was below the melting point of silicon, and the silicon films transformed from the amorphous phase to a small-grain polycrystalline silicon phase by the SPC mechanism.

The electrical characteristics of the polycrystalline silicon TFTs in the center, transition, and edge regions are shown in Fig. 4. In the center region, the polycrystalline silicon TFTs achieved the best electrical characteristics in terms of field-effect mobility and on/off ratio, which were $500\,cm^2\,V^{-1}\,s^{-1}$ and 2.45×10^9, correspondingly. The polycrystalline silicon TFTs in the transition region attained the field-effect mobility and an on/off ratio of $278\,cm^2\,V^{-1}\,s^{-1}$ and 7×10^8, accordingly. In contrast, the polycrystalline silicon TFTs in the edge region exhibited the worst electrical characteristics in terms of field-effect mobility and on/off ratio, which were $48\,cm^2\,V^{-1}\,s^{-1}$ and 3.49×10^6, respectively. These performance results were attributed to the largest grain size and the best crystallinity in the center region. The grain size of polycrystalline silicon thin films and the electrical characteristics of resulted devices with various crystallization technologies were compared (Table I). Obviously, the results indicated that the polycrystalline silicon TFTs fabricated via CW laser crystallization possessed the largest grain size and, therefore, achieved the highest device performance than other crystallization technologies. However, the edge and transition regions of that were still small grains and the worse crystallinity, causing the large variation in device performance. Therefore, the high-quality large-area polycrystalline silicon film by multi-scan method is necessary to reduce the disparity of TFTs.

TABLE I. The comparisons of grain size and electrical characteristic **with** different crystallization methods.

Crystallization method	Grain size	Field-effect mobility ($cm^2\,V^{-1}\,s^{-1}$)	I_{on}/I_{off}
CW laser crystallization (this work)	$2\,\mu m \times 20\,\mu m$	500	2.45×10^9
ELC[8]	$\sim 1\,\mu m$	119	8.5×10^8
SPC[3]	$0.15\,\mu m$	19.3	1.36×10^{-6}
MIC[4]	$\sim 1\,\mu m$	~ 100	$\sim 10^{-7}$

In summary, the effects of crystallization mechanism on the electrical characteristics of green continuous-wave-laser-crystallized polycrystalline silicon TFTs were investigated. Under the laser power at 3.2 W and the laser spot size of $400\,\mu m \times 300\,\mu m$ with a Gaussian distribution, the resulting polycrystalline silicon thin film could be classified into three regions: the center, transition, and edge regions. From the SEM and Raman spectra, the polycrystalline silicon film in the center region subjected to the largest laser energy density could achieve the largest grain size of $2\,\mu m \times 20\,\mu m$ due to fully liquid-phase crystallization along the scanning direction. In contrast, the polycrystalline silicon film in the edge region with the lowest laser energy density displayed the smallest grain size owing to the SPC mechanism. In the transition region, the crystallization mechanism varied from PMG to SLG-like corresponding to the laser energy changing from lower to higher. Consequently, the TFT in the center region achieved an excellent field-effect mobility of $500\,cm^2\,V^{-1}\,s^{-1}$ and a higher on/off current ratio of 2.45×10^9 as compared with $48\,cm^2\,V^{-1}\,s^{-1}$ and 3.49×10^6, respectively, in the edge region. Because of the high quality polycrystalline silicon film and superior device performance in the center region, the proposed devices using CW laser crystallization are suitable for future applications in high-performance AMLCDs and 3D-ICs.

This work was supported by the National Science Council of the Republic of China under Grant No. NSC 99-2221-E-009-168-MY3 and in part by the Nano Facility Center of National Chiao Tung University and National Nano Device Laboratories (NDL) for the technical support.

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