Bipolar Ni/TiO_2/HfO_2/Ni RRAM With Multilevel States and Self-Rectifying Characteristics

Chung-Wei Hsu, Tuo-Hung Hou, Mei-Chin Chen, I-Ting Wang, and Chun-Li Lo

***Abstract*— To be compatible with 3-D vertical crossbar arrays, a TiO_2/HfO_2 bilayer resistive-switching memory (RRAM) cell sandwiched between Ni electrodes is developed. The proposed device has numerous highly desired features for the implementation of 3-D vertical RRAM, including: 1) stable bipolar resistive switching; 2) forming free; 3) self-compliance; 4) self-rectification; 5) multiple resistance states; and 6) room-temperature process. The resistive switching and current rectification are attributed to oxygen vacancy migration in HfO_2 and potential barrier modulation of the asymmetric TiO_2/HfO_2 tunnel barrier. The rectification ratio up to 10^3 is capable of realizing a single-crossbar array up to 16 Mb for future high-density storage class memory applications.**

***Index Terms*— 3-D memory, crossbar array, resistive-switching memory (RRAM), self-rectification.**

I. Introduction

CROSSBAR resistive-switching memory (RRAM) with a minimum cell size of $4F^2$ has attracted much attention recently because of its ultrahigh density and ultimate scaling potential. In crossbar RRAM arrays, to mitigate crosstalk from undesired sneak current through adjacent cells at read and write operations, numerous two-terminal selection devices with either unidirectional or bidirectional nonlinear current–voltage ($I - V$) characteristics were proposed to integrate with the memory devices in series [1], [2]. Nevertheless, the heterogeneous integration of two individual selection and memory devices inevitably increases process complexity and undermines the advantage of the simple structure of RRAM. Furthermore, several bit cost scalable 3-D vertical NAND flash architectures were proposed to provide extremely high bit density at extremely low cost [3]. A similar 3-D vertical RRAM architecture [4], [5] has to be developed to compete with 3-D vertical NAND flash for future storage class memory (SCM) applications [6]. The potential advantages of 3-D vertical RRAM over 3-D vertical NAND flash include better memory performance, ease of fabrication, and removal of vertical transistors inside the core array. Stacking two individual selection and memory devices is, however, extremely challenging in 3-D vertical RRAM because the metal electrodes between two devices cannot be easily patterned at the vertical sidewall. Therefore, it is of great interest to develop a nonlinear RRAM device requiring no external selection device for low-cost 3-D vertical crossbar RRAM [7], as shown in Fig. 1(a).

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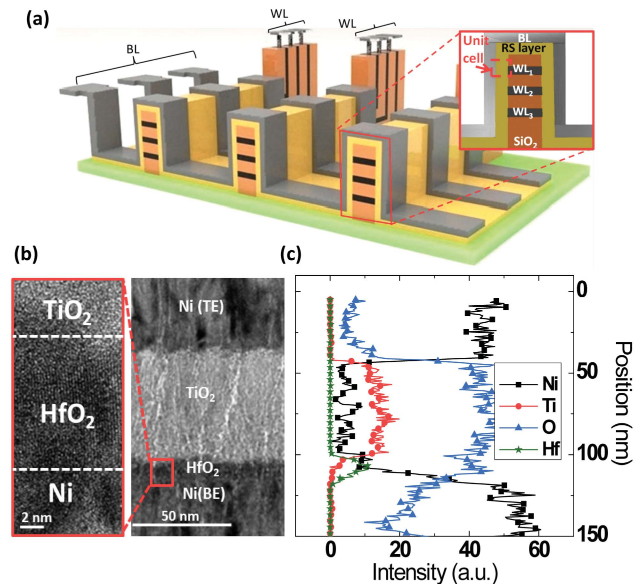

Fig. 1. (a) Illustration of a 3-D vertical crossbar RRAM array. (b) Cross-sectional TEM image of the Ni/TiO_2/HfO_2/Ni stack and the enlarged image of the HfO_2 layer. Both TiO_2 and HfO_2 appeared polycrystalline. (c) Corresponding EDX profiling of the Ni/TiO_2/HfO_2/Ni stack.

In this letter, a bipolar Ni/TiO_2/HfO_2/Ni RRAM device with multilevel resistance states and self-rectifying characteristics is reported. The rectification ratio (RR), defined by the current ratio at ± 2 V of the low-resistance state (LRS), is as high as three orders of magnitude. Oxygen vacancy migration under bipolar electric field and the corresponding tunnel barrier modulation in HfO_2 are speculated to be responsible for the multilevel bipolar resistive switching (BRS) requiring no initial forming and current compliance. The current rectification is attributed to the asymmetric TiO_2/HfO_2 tunnel barrier. Finally, a numerical array analysis shows that the proposed device is promising to implement a single-crossbar array up to 16 Mb using an all-line pull-up (all-LPU) read scheme.

II. Experimental Procedures

A 100-nm Ni layer is deposited on heavily doped n-type Si wafers as a shared bottom electrode using sputtering. A 10-nm HfO_2 layer and a 60-nm TiO_2 layer are deposited sequentially on the bottom electrode using reactive magnetron

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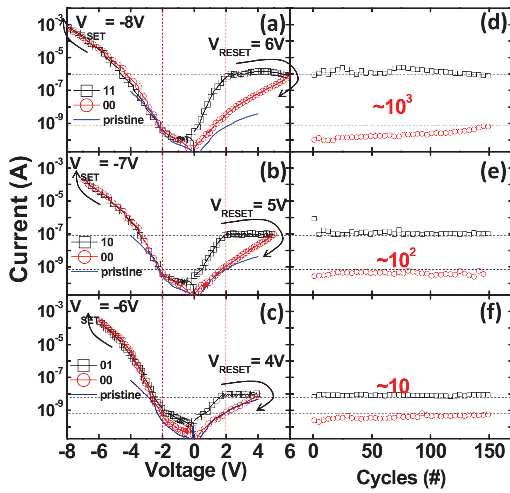

Fig. 2. Typical BRS characteristics of Ni/TiO_2/HfO_2/Ni memory cells between (a) 00 and 11 states, (b) 00 and 10 states, and (c) 00 and 01 states, controlled by different SET/RESET voltages. The $I - V$ curve of the pristine device before RS is also plotted for comparison. The corresponding rectification ratios at ± 2 V during 150 consecutive BRS cycles are plotted in (d)–(f).

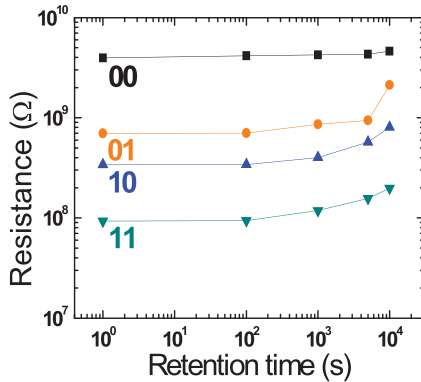

Fig. 3. Retention characteristics of four resistance states (00, 01, 10, and 11) measured at room temperature. The resistance values are read at 0.5 V.

DC sputtering and 6″ Hf and Ti metal targets, respectively. The O_2:Ar gas flow ratio is 1:5 and 1:2 for HfO_2 and TiO_2, respectively. Finally, Ni top electrodes with a thickness of 100 nm and an area of 10^4 μm^2 are deposited using sputtering and a shadow mask. The entire fabrication is conducted at room temperature without thermal treatment. Fig. 1(b) shows the cross-sectional transmission electron microscopy (TEM) image of the Ni/TiO_2/HfO_2/Ni stack, showing the polycrystalline TiO_2 and HfO_2 layers. Fig. 1(c) shows the corresponding elemental profiling using energy-dispersive X-ray spectroscopy (EDX). All devices are measured by applying voltages to the top electrodes while the bottom electrode is grounded.

III. Results and Discussion

Fig. 2(a)–(c) shows typical BRS characteristics of the Ni/TiO_2/HfO_2/Ni memory cells. The as-fabricated devices are initially at a high-resistance state (HRS), 00 state, and may be SET/RESET between multiple LRS (01, 10, and 11 states) and the 00 state using negative SET and positive RESET

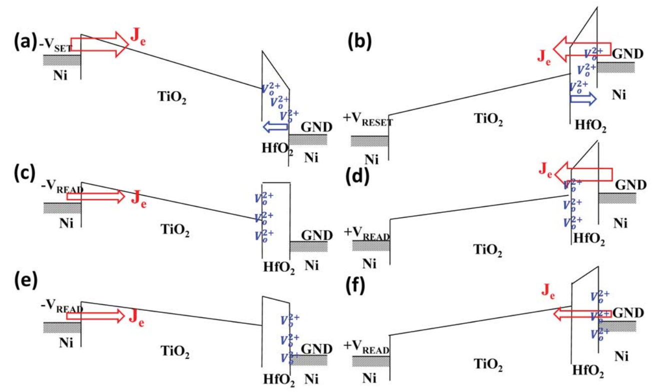

Fig. 4. Band diagrams of the Ni/TiO_2/HfO_2/Ni memory cells at (a) SET, (b) RESET, (c) LRS READ at negative bias, (d) LRS READ at positive bias, (e) HRS READ at negative bias, and (f) HRS READ at positive bias. Migration of oxygen vacancies (V_o^{2+}) in HfO_2 is driven by bipolar electric field at SET /RESET and modulated potential barriers at READ. Current conduction is dominated by the TiO_2 and HfO_2 barriers at negative and positive READ. The band diagrams shown here are used for qualitative explanation only. The quantitative band diagrams depend on the exact material permittivity and V_o^{2+} distribution.

voltages without current compliance. The gradual SET/RESET process allows desired resistance states to be controlled using appropriate SET voltages ranging from -6 to -8 V and RESET voltages ranging from 4 to 6 V. Furthermore, the resistance readout can only be acquired at positive bias. The $I - V$ curves of the 01, 10, and 11 states overlapped with the 00 state at negative bias, and exhibit a turn-on voltage around -2 V. Therefore, the rectifying $I - V$ within ± 2 V at the 01, 10, and 11 states is similar to that in one diode-one resistor (1D1R) cells [1]. Unlike the narrow programming margin of unipolar resistive switching and the requirement of external diode devices in 1D1R cells, this self-rectifying cell, however, utilized stable BRS with large programming margin because of the opposite polarities of SET/RESET voltages. Larger RR helps to suppress parasitic sneak current in crossbar arrays and improves read margin. Fig. 2(d)–(f) shows stable RR ranging from 10^3 to 10 depending on the LRS during 150 consecutive BRS cycles. Fig. 3 shows that LRS (01, 10, and 11 states) had worse retention than HRS (00), but those LRS with lower resistance values are less prone to retention degradation.

Separate single-layer devices of Ni/60-nm TiO_2/Pt and Ni/10 nm HfO_2/Pt are also fabricated for comparison. The Pt bottom electrode is chosen as an inert electrode to prevent the additional complication from the interaction between the bottom electrode and the oxide films. BRS is only found at the Ni/10-nm HfO_2/Pt device (not shown here), suggesting that the BRS in Ni/TiO_2/HfO_2/Ni possibly originated from oxygen vacancy (V_o^{2+}) migration in HfO_2. A similar model based on oxygen ion migration was also proposed to explain BRS in another TiN/Ti/TiO_x/ HfO_x/TiN cell [8]. Because of the lack of electrical forming and high overshoot current, Ni cation migration from the Ni electrodes [9] is believed to have a negligible effect on the observed BRS. Although further investigations in the future would be necessary for thorough understanding, a plausible model is proposed to qualitatively explain the self-rectifying $I - V$ and the multiple resistance

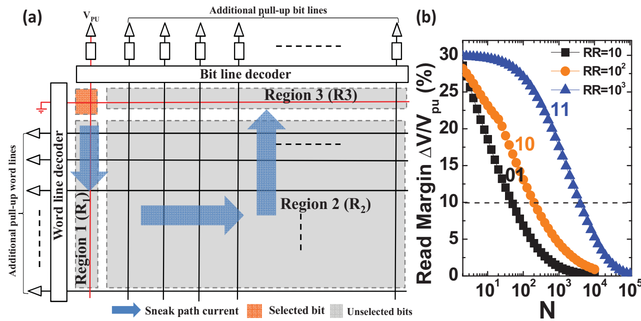

Fig. 5. (a) Schematic view of a N × N crossbar RRAM array using the all-LPU read scheme. Unselected bits at the sneak current path are divided into three regions. (b) Simulation of the normalized read margin between three LRS (11, 10, and 01 states) and HRS (00) as a function of the number of bit (word) lines N.

states. Fig. 4 shows the band diagrams of the $Ni/TiO_2/HfO_2/Ni$ cell at SET, RESET, and READ conditions. The V_o^{2+} in HfO_2 migrates toward the TiO_2/HfO_2 interface at SET [Fig. 4(a)] and toward the HfO_2/Ni interface at RESET [Fig. 4(b)]. When reading at a low negative voltage [Fig. 4(c) and (e)], the electron injection from the top Ni electrode is limited by the Schottky barrier of Ni/TiO_2 and thick TiO_2, similar to the previously reported $Ni/TiO_2/Ni$ bipolar selector [2], and the different V_o^{2+} profiles in HfO_2 at LRS/HRS had only limited effects on the current readout. When reading at a low positive voltage [Fig. 4(d) and (f)], the electron injection from the bottom Ni electrode into HfO_2 encounter a much higher but thinner barrier. Therefore, tunneling current through the thin HfO_2 layer became significant. The positively charged V_o^{2+} piling up at the TiO_2/HfO_2 interface significantly modulates the potential barrier and results in higher tunneling current at LRS. An effective asymmetric tunnel barrier, such as the thick TiO_2/thin HfO_2 bilayers with narrow/wide bandgaps, is known to greatly enhance $I - V$ asymmetry [10]. Furthermore, the V_o^{2+} profiles might be adjusted by the magnitude of SET/RESET voltages to create multiple resistance states. The worse LRS retention and unstable V_o^{2+} at the TiO_2/HfO_2 interface might be related to the strong oxidative capability of Ti and the preferred TiO_2 formation. Because those LRS with lower resistance (higher V_o^{2+} concentration at the interface) show improved retention, increasing the V_o^{2+} concentration in HfO_2 during deposition might stabilize V_o^{2+} at the interface in the future.

To evaluate the potential of the proposed self-rectifying cell for high-density SCM applications, a numerical array analysis on a $N \times N$ crossbar array with a line resistance of 2.5 Ω/□, as shown in Fig. 5(a), is performed using SPICE [11] and the all-LPU read scheme, where a positive pull-up voltage (V_{pu}) of 2 V is applied to all bit/word lines except the selected word line connecting to the ground. In analogy to the 1D1R crossbar array, those unselected cells biased at negative voltages has significantly higher resistance to suppress sneak current. Fig. 5(b) shows the calculated read margin as a function of RR ranging from 10^3 to 10 at ±2 V for the 11, 10, and 01 states. To unambiguously distinguish 11, 10, and 01 states from the HRS 00 state, the maximum array size is estimated to be 16 Mb, 40 kb, and 2.5 kb, respectively, with at least a 10% read margin. Furthermore, the V/2 and V/3 write schemes may be applied for SET/RESET operations, respectively, to suppress write disturb [11]. An additional write analysis (not shown here) confirms that the line resistance has a negligible effect on voltage delivery and the sneak current at write is less than the program current of the selected cell at the maximum array sizes predicted by the read analysis. The results suggest that the RR of 10^3 at the 11 state is sufficient to implement high-density single-level RRAM chips, while overhead of peripheral circuits and chip area efficiency have to be considered using all levels because of the smaller array size.

IV. Conclusion

A self-rectifying BRS memory with controllable multilevel resistance states was fabricated at room temperature using a $Ni/TiO_2/HfO_2/Ni$ structure. The BRS and current rectification were attributed to oxygen vacancy migration in HfO_2 and potential barrier modulation of the asymmetric TiO_2/HfO_2 tunnel barrier. The self-rectifying device suppressed sneak current and improved read margin in crossbar arrays similar to the 1D1R cells. Furthermore, the forming-free and self-compliance characteristics greatly reduced the complexity of peripheral circuit design. To realize the full potential of the proposed device in 3-D vertical RRAM arrays and SCM applications, LRS retention was the primary area for improvement. Device scalability and further reduction of operational voltages and set current to be compatible with peripheral circuits should also be investigated in the future.

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