Characteristics of Gate-All-Around Junctionless Poly-Si TFTs With an Ultrathin Channel

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***Abstract*— This letter demonstrates for the first time junctionless (JL) gate-all-around (GAA) poly-Si thin-film transistors (TFTs) with ultrathin channels (2 nm). The subthreshold swing is 61 mV/decade and the ON/OFF current ratio is close to 10^8 because of the excellent gate controllability and ultrathin channel. The JL-GAA TFTs have a low drain-induced barrier lowering value of 6 mV/V, indicating greater suppression of the short-channel effect than in JL-planar TFTs. The cumulative distribution of electrical parameters in JL-GAA is small. Therefore, the proposed JL-GAA TFTs of excellent device characteristics along with simple fabrication are highly promising for future system-on-panel and system-on-chip applications.**

***Index Terms*— Gate-all-around (GAA), junctionless (JL), thin-film transistor, ultrathin channel.**

I. Introduction

RECENTLY, junctionless (JL) silicon nanowire (NW) devices with high doping concentrations in their channel and source/drain (S/D) regions have attracted much interest, overcoming the technological difficulties in the formation of ultrasteep S/D profiles using conventional devices, which suffer from the short-channel effect and parasitic series resistance [1]–[3]. Such JL features are also demonstrated with polycrystalline silicon (poly-Si) thin-film transistors (TFTs) [4], [5], which are suitable for monolithic 3-D vertically stacked integrated circuits and to continue the applicability of Moore's law [6]. The adoption of NW geometries as the JL channel must be small enough to fully turn off the channel. Gate-all-around (GAA) architecture is extremely suitable for JL NWs devices, because the gates can effectively control the electrostatic potential in the ultrathin channel region. In addition, large grains in the poly-Si channel are associated with superior performance, including a steep subthreshold swing (SS), a high ON-state current, owing to the accompanying reduction in defects [7].

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Hence, this letter investigates the poly-Si channel of JL TFTs utilizing dry oxidation to form the ultrathin channel instead of directly depositing the thin-film as the poly-Si channel in JL TFTs [4], [5] of small grain size suffered from the performance degradation mentioned above. The channel with nano-belt structure is also adopted to reduce the sensitivity of threshold voltage (V_{TH}) variations with fabrication parameters, i.e., if one of the channel dimensions is small enough, the variations of the other dimension do not impact too much V_{TH} [8]. The device with GAA structure is compared with that with planar structure. The transfer characteristics, output characteristics, and statistical device-to-device variations of electrical parameters are also performed for two types of devices. The JL-GAA TFTs with excellent device performances along with simple fabrication are highly promising for future system-on-panel (SOP) and system-on-chip applications.

II. Device Structure and Fabrication

The process for producing 2-nm-thick poly-Si nano-belt channel is fabricated by initially growing a 400-nm-thick thermal silicon dioxide layer on 6-in silicon wafers. Subsequently a 40-nm-thick undoped amorphous silicon (a-Si) layer is deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Then, the a-Si layer is solid-phase recrystallized (SPC) and formed large grain size at 600 °C for 24 h in nitrogen ambient. The SPC layer is implanted with 16-keV phosphorous ions at a dose of 1×10^{14} cm^{-2}, followed by furnace annealing at 600 °C for 4 h. The SPC film is thinned down to 28 nm. The active layers, serving as channel, are defined by electron beam lithography and then mesa-etched by time-controlled wet etching of the buried oxide to release the poly-Si bodies. Subsequently, a 13-nm-thick dry oxide, consuming ∼13-nm-thick poly-Si on both sides of the channel to form 2-nm-thick channel and 6-nm-thick nitride by LPCVD are deposited as the gate oxide layer. The 250-nm-thick *in-situ* doped n+ poly-Si is deposited as a gate electrode, and patterned by electron beam and reactive ion etching. A 200-nm-thick SiO_2 passivation layer is deposited. Finally, a 300-nm-thick Al-Si-Cu metallization is performed and sintered at 400 °C for 30 min.

III. Results and Discussion

Fig. 1(a) shows the device structure of JL devices. Fig. 1(b) shows the cross-sectional transmission electron microscopic (TEM) images of channel region for JL-GAA with ten strips of NW and JL-planar TFTs; the figure clearly shows that the

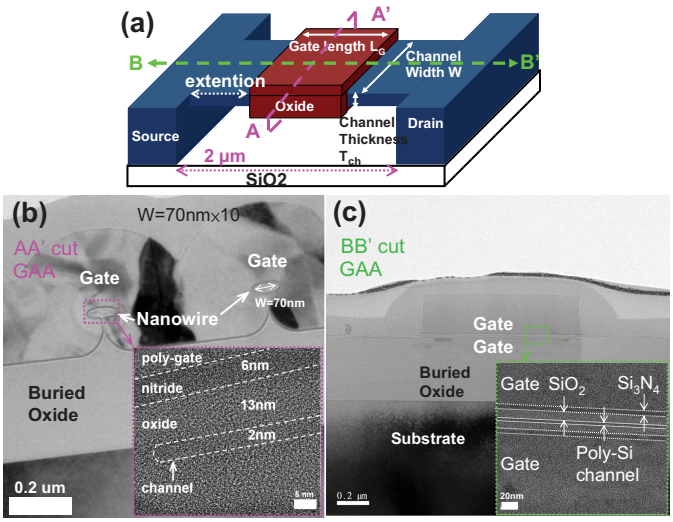

Fig. 1. (a) Device structure for JL-GAA TFTs. Cross-sectional TEM images of GAA structure (b) along the AA′ direction with 2-nm channel thickness and (c) along the BB′ direction with L_G = 1 μm.

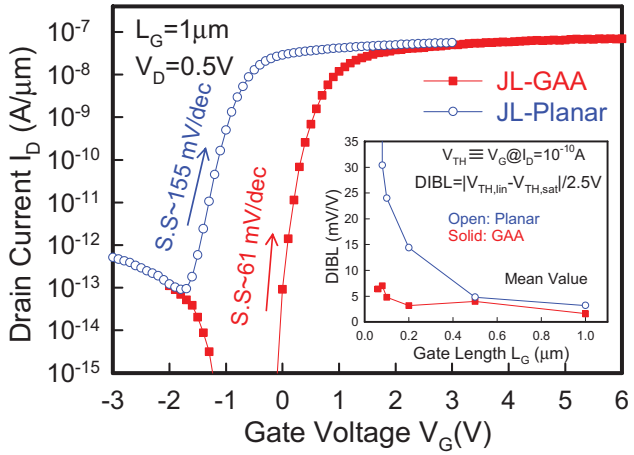

Fig. 2. Transfer I_D–V_G characteristics of JL-GAA and JL-Planar TFTs. Inset: DIBL characteristics of both devices.

nanosheet channel of 2 nm is surrounded by the gate electrode and large grain size as the poly-Si channel is expected to achieve superior performance. The dimensions of each NW are 2-nm high × 70-nm wide. The JL-planar device serves as the control, and the channel dimensions are 15-nm high × 0.95-μm wide. The silicon nitride that is used as a gate insulator reduces the equivalent oxide thickness, achieving a low leakage current and a steep SS [9]. Fig. 1(c) shows TEM images along the BB′ direction in a 70-nm-wide NW. The contrast of figure is not sharp, as TEM sample production is difficult in a very narrow and little bended NW. The length of extension region is 0.5 μm at gate lengths (L_G) of 1 μm. Fig. 2 shows plots of the transfer I_D–V_G characteristics of JL-GAA and JL-planar TFTs. The devices show no hysteresis effect in the forward and backward gate-voltage sweep. The on-current (I_{ON}) is defined as the drain current at V_G = 3 V for JL-planar TFTs and at V_G = 6 V for JL-GAA TFTs. The off-current (I_{OFF}) is defined as the lowest drain current. The ON/OFF current ratio and SS of the JL-planar are 10^6 and

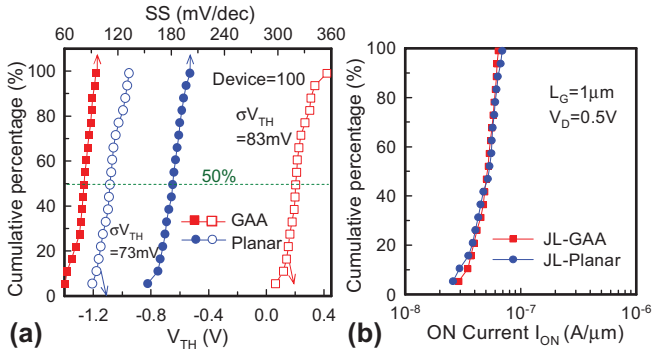

Fig. 3. Cumulative distributions of (a) V_{TH}, SS and (b) ON-current for JL-GAA and JL-Planar with L_G = 1 μm.

155 mV/decade, respectively, at T = 300 K. For JL-GAA TFTs, the ON/OFF current ratio and SS are over 10^7 and ∼61 mV/decade, respectively. As compared with JL-planar, the JL-GAA device has a obvious reduction of OFF-state leakage current and an SS value that is close to the theoretical value of 60 mV/decade, owing to the gate controllability through GAA structure and ultrathin channel. The gate current of JL-GAA in subthreshold region is verified (∼10^{-13}A) to avoid affecting drain current. The apparent V_{TH} shift between planar and GAA devices stems from different channel volume and quantum confinement effects at small dimensions [8], [10]. The V_{TH} of quantitative calculations including quantum effect can fit experimental results [11]. However, the fitted parameter of channel doping is 10^{18} cm^{-3}, lower than expected value of 10^{19} cm^{-3}. We speculate that this might be dose loss of channel doping because of interface segregation between channel and gate oxide [12], [13].

In addition, it is suggested that the raised S/D would be preferred to further improve on-current in the future. The inset in Fig. 2 shows drain-induced barrier lowering (DIBL) values with different L_G ranging from 1 to 0.06 μm. The V_{TH} is defined as the gate voltage at I_D = 10^{-10}A. The DIBL is defined as the difference between the V_{TH} at V_{DS} = 0.5 V and V_{DS} = 3 V, normalized by the difference between these drain voltage ΔV_{DS}. A nearly negligible DIBL of 6 mV/V is obtained at L_G = 60 nm for JL-GAA TFTs, achieving a superior short-channel control.

In Fig. 3(a) and (b), cumulative distributions of V_{TH}, SS, and I_{ON} in two types of devices are shown; the statistical device-to-device variations of electrical parameters for JL-GAA TFTs are similar to JL-planar ones. The median values of V_{TH} and SS (GAA: V_{TH} = 0.2 V, SS = 79 mV/decade; planar: V_{TH} = −1.1 V, SS = 181 mV/decade) are extracted from cumulative distributions at 50%. Fig. 4 shows plots of the I_D–V_D curves at various $|V_G - V_{TH}|$; The V_{TH} of about −1.1 and 0.2 V for JL-planar and JL-GAA TFTs is chosen for I_D–V_D comparsion. GAA and planar TFTs have similar saturation current level. The increment in the saturation current is decreased as $V_G - V_{TH}$ is increased, which may be because of the series resistance and surface scattering at higher gate voltage. The absence of float-body or kink effect elucidates low impact-ionization rate (IIR) of electrons at V_D = 20 V.

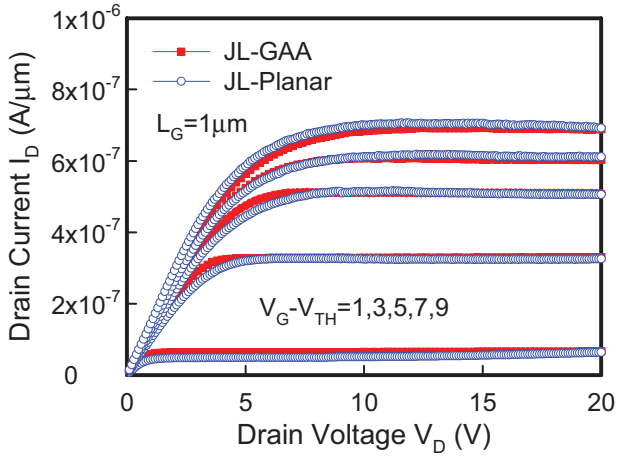

Fig. 4. I_D-V_D curves of devices with various $|V_G-V_{TH}|$ values for JL-GAA and JL-Planar TFTs.

TABLE I
COMPARISON OF KEY PARAMETERS FOR JUNCTIONLESS TFTS

Junctionless TFT	This letter	Ref. [4]	Ref. [5]	Ref. [14]
Cross-section	Nano belt	Rough rectangular	Flat rectangular	Flat rectangular
Channel structure	N-SPC JL-GAA	N-SPC JL-GAA	N-SPC JL-planar	N-SPC JL-planar
NH_3 plasma	W/O	W/O	W/O	W/1hrs
W/L (μm/μm)	0.7 × 10/1	0.07 × 2/1	10/5	0.7/1
V_{TH} (V)	0.2	–0.3	∼ –0.3	–1.2
EOT (nm)	17	15	8	8
T_{ch} (nm)	2	12	10	10
S.S. (mV/dec.)	61	199	240	141
I_{ON}/I_{OFF} (V_G:V_D)	> 10^7 (3 V;0.5 V)	> 10^6 (5 V;1 V)	> 10^7 (3 V;0.1 V)	> 10^6 (3 V;0.5 V)

The main reason for the findings may be that a conventional device has a PN junction between its channel and its drain region, such that the voltage drop is easily concentrated across the drain-side junction. In contrast, the voltage distribution in the channel is uniform in JL devices to alleviate IIR. Table I shows comparison of electrical parameters of JL-GAA TFTs to other research. Our JL-GAA TFTs show better SS and ON/OFF current ratio because of large poly-Si grain size, ultrathin channel, and GAA structure.

IV. CONCLUSION

The JL-GAA TFTs with 2-nm-thick nano-belt channel were successfully fabricated and characterized. This process was simple and compatible with existing CMOS processes. Such a GAA JL feature simplified the S/D engineering. The JL-GAA TFTs had excellent electrical characteristics, such as low I_{OFF}, record SS, negligible DIBL, small device-to-device variation, and absence of kink effect at high drain voltage. Hence, such a JL-GAA with nano-belt channel explored its potential for TFTs in SOP and 3-D stacked applications.

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