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Design of buck-type current source inverter fed brushless DC motor drive and its application to position sensorless control with square-wave current

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Abstract: Owing to the widely used brushless DC motors (BDCMs) in high-efficiency applications, many position sensorless control methods based on voltage source inverters had been developed in the literature. Recently, current source inverters (CSIs) are receiving more and more attention because of their inherent short-circuit protection characteristics. But no position sensorless control for buck-type CSI with square-wave current had been found in the literature. In this study, the buck-type CSI-fed BDCM drive is designed and its application to the square-current position sensorless control is first proposed. The provided simulation and experimental results verify the effectiveness of the proposed CSI-based position sensorless control.

1 Introduction

Owing to the permanent-magnetic rotor field, brushless DC motors (BDCMs) possess higher efficiency than the popular induction motors. Therefore more and more BDCMs are used in various high-efficiency variable-speed applications, such as fan motors [1, 2], compressor motors [3, 4], vehicle motor [5–7] and home applications [8].

In the normal square-wave current operations of BDCMs, the discrete rotor position should be monitored by position sensors to yield adequate current commutations [9]. The six-switch voltage source inverter (VSI) fed BDCM is plotted in Fig. 1 where the feedback position signals are used to synthesise the switching signals. The DC voltage amplitude can be equivalently varied via the pulse width modulation (PWM) ratio by the speed controller. In order to avoid short-circuit condition, both switches in the same leg could not conduct in the same time. A 120° conduction (six-step) method [3–9] and 150° conduction (12-step) method [1, 2] are two commutation schemes for six-switch VSI. Additionally, various VSI topologies can also be found in [10, 11].

Although VSIs are widely used in motor drives, reliability concerns have been raised on the motor because of the high dv/dt that comes from the PWM output voltage. Voltage surges resulting from these rapid voltage transitions can cause motor insulation degradation, bearing failure because of erosion caused by the resulting shaft leakage current, and unacceptable electromagnetic interference effects on the control circuits, as well as acoustic noise in the motor.

In addition, the concern about the reliability of the electrolytic capacitor has forced user to use costly and bulky film capacitors [12]. Moreover, the possible shoot-through problem in VSI has always been a concern associated with system reliability.

The other topology is the current source inverter (CSI). CSI uses an inductor as the energy storage component, and thus avoids many drawbacks of VSI. It also has an inherent advantage of the shoot-through short-circuit protection capability, and no PWM voltage in the motor terminals. The bulky inductor has longer lifetime than the capacitors.

In fact, CSI topology had been widely used in high-power application. The common thyristor-based load commutated inverter (LCI) topology has been reported for BDCM drive [10]. Four quadrant operation and current sensorless control over most of the operating speed range are good features of this topology. However, thyristor-based CSI is suitable for the high-power utility-connected industry applications, but it is not suitable for kilowatt (kW)-level residential applications, such as electric vehicles and variable-speed air conditioners.

Recently, more and more researches are focused on insulated gate bipolar transistor (IGBT)-based CSI drive for the automotive applications [5–7]. The common IGBT-based CSI for BDCM is plotted in Fig. 2 where the current source is controlled by the speed controller. In order to provide current conducting path, at least one of the three upper switches and at least one of the three lower switches need to turn on at the same time. The series-connected diodes need to withstand the negative voltages. Three AC capacitors are connected between the CSI and BDCM, and they provide the current flowing path during the current commutations [5–7].

For square-wave current commutations in BDCM drive, the hall position sensors are required to provide the position information. However, the hall sensors may be faulted and may not be used in high-temperature environment, such as refrigerant compressors.

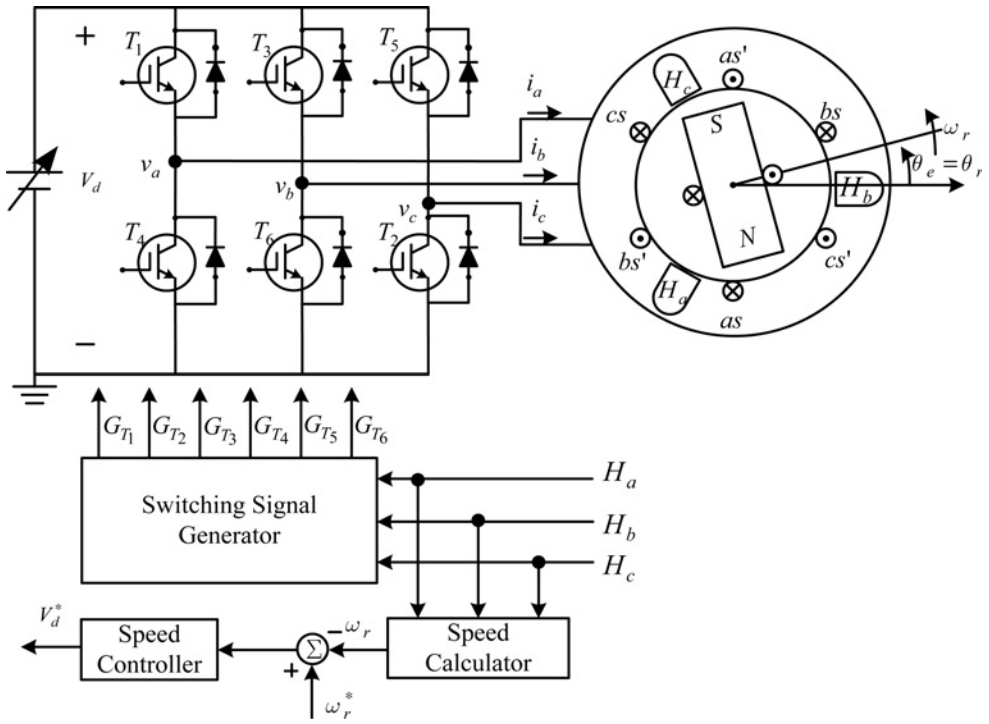

Fig. 1 *Conventional VSI-fed BDCMs*

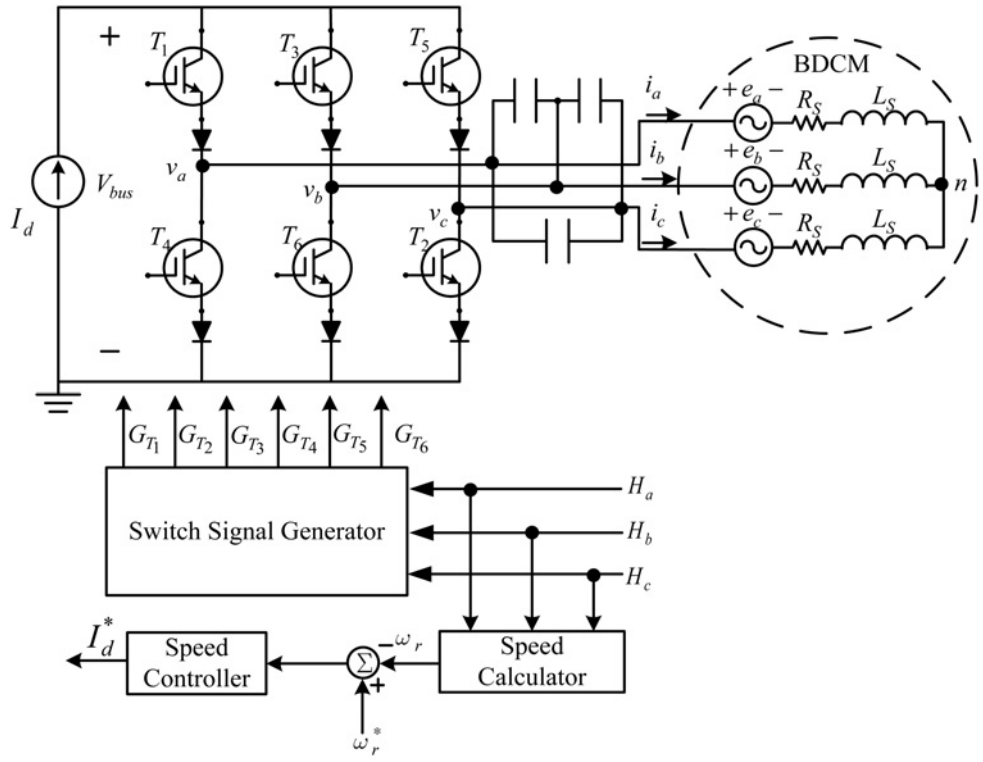

Fig. 2 *Ideal CSI-fed BDCM*

It is difficult to make clear comparison between CSI and VSI. For potential applications, such as electric vehicles, system reliability is an important issue. It is clear that the life time of the bulky electrolytic capacitor is shorter than the bulky inductor. To further improve the reliability of the CSI-based drive, position sensorless control is required to be able to ride through sensor-fault conditions.

Owing to the concern of system reliability for BDCM operations, many position sensorless control methods for VSI had been developed in the literature and most of them are based on the back-electromotive force (EMF) detecting methods [1–5, 11, 13–16]. The method in [11] was developed for a four-switch VSI topology and the others are developed for the common six-switch VSI topology. The current-mode

sensorless control in [13] should be seen as a VSI-based method because that the terminal voltages had significant PWM voltage transitions.

In VSI-based sensorless control methods, only zero-crossing points of the phase back-EMFs can be detected from the terminal voltages. Therefore delaying these zero-crossing points by 30° is required to obtain the correct commutation instants [11, 14–17], but it may introduce some commutation errors.

In CSI, the line-to-line back-EMFs can be easily sensed from the terminal voltages, and thus the commutation instants can be obtained directly without the processing of the additional 30° delay. However, no position sensorless control methods for IGBT-based CSI with square-wave current commutations had been found in literature.

In this paper, the current source in Fig. 2 is implemented by the buck converter and the buck-type CSI-fed BDCM drive is designed. It is noted that the position sensorless control for buck-type CSI-fed BDCM is first proposed. The provided simulation and experimental results support the validity of the proposed CSI-based position sensorless control.

2 Current source inverter fed BDCM

For servo applications, the torque performance is most important. However, in the promotion of residential variable-speed products, such as air conditioners, the cost issue is more critical to the performance issue. Thus, the manufactures take a simple strategy – producing near-sinusoid-EMF BDCMs to reduce the cost of motor.

For the high-performance series of the air conditioners, the high-cost sinusoid-current drive is applied with the other high-efficiency system techniques. However for the popular series, the low-cost square-current drive is utilised even when the yielded torque is not constant. Thus, the sinusoidal rotor magnets are initially assumed.

2.1 Ideal current source inverter

The variable-speed drive BDCM fed by ideal current source is plotted in Fig. 2, where the current source is variable according to the speed controller output I_d^*. According to the winding distribution in Fig. 1, the flux linkages of three phase windings can be assumed as $\phi_{as} = \Phi_{MAX} \sin\ \theta_e$, $\phi_{bs} = \Phi_{MAX} \sin(\theta_e - 2\pi/3)$ and $\phi_{cs} = \Phi_{MAX} \sin(\theta_e + 2\pi/3)$, where Φ_{MAX} is the maximum flux linkage. Thus, the induced voltages for each phase winding can be expressed as

$$\begin{aligned} e_a &= \frac{d\varphi_{as}}{dt} = \Phi_{MAX}\omega_e \cos\theta_e = \frac{P}{2}\Phi_{MAX}\omega_r \cos\left(\frac{P}{2}\theta_r\right) \\ e_b &= \frac{d\varphi_{bs}}{dt} = \frac{P}{2}\Phi_{MAX}\omega_r \cos\left(\frac{P}{2}\theta_r - \frac{2\pi}{3}\right) \\ e_c &= \frac{d\varphi_{cs}}{dt} = \frac{P}{2}\Phi_{MAX}\omega_r \cos\left(\frac{P}{2}\theta_r + \frac{2\pi}{3}\right) \end{aligned} \quad (1)$$

where P is the pole number, ω_e is the synchronous frequency in 'rads/s', and $\theta_r = 2\theta_e/P$ is the rotor position.

When the position θ_e is between 0 and $\pi/3$ ($0 \le \theta_e < \pi/3$), both switches T_1 and T_2 are conducting and the current I_d flows through the a-phase and c-phase windings $I_d = i_a = -i_c$. The winding currents i_a, i_b and i_c are in phase with the back-EMF voltages e_a, e_b and e_c, respectively.

The voltage e_s is denoted by (see (2))

where k is an integer and K_E is the voltage gain $K_E = P\Phi_{MAX}/2$. It is clear that the voltage e_s is a periodic waveform and its average value is $\overline{e_s} = 3\sqrt{3}K_E\omega_r/\pi$.

Since $i_a + i_b + i_c = 0$ in Y-connected windings, the neutral voltage v_n can be represented in terms of the terminal voltages

$$v_n = \frac{v_a + v_b + v_c}{3} \quad (3)$$

When the switch T_3 is conducting, the terminal voltage v_b is equal to the bus voltage $v_b = V_{bus}$, and when the switch T_6 is conducting, the terminal voltage v_b must be zero. When both switches T_3 and T_6 are not conducting, b-phase winding is floating and the terminal voltage v_b is equal to the sum of the neutral voltage plus the induced b-phase voltage $v_b = v_n + e_b$.

Therefore when the position θ_e is located between 0 and $\pi/3$ ($0 \le \theta_e < \pi/3$), both switches T_1 and T_2 are conducting. The terminal voltage v_a can be expressed as $v_a = V_{bus} = e_a - e_c + 2I_dR_s \simeq e_s$ and the terminal voltage v_c is zero. From (3), the neutral voltage terminal is $v_n = (V_{bus} + v_b)/3$ and thus, the floating b-phase voltage v_b is closed to

$$v_b = \frac{V_{bus}}{2} + \frac{3}{2}e_b \simeq \frac{e_a - e_c}{2} + \frac{3}{2}e_b \simeq e_b - e_c \simeq \sqrt{3}K_E\omega_r \sin\theta_e \quad \text{when} \quad 0 \le \theta_e < \pi/3 \quad (4)$$

The illustrated waveforms are plotted in Fig. 3. Three position signals H_a, H_b and H_c are used as the commutation signals to obtain the BDCM speed ω_r and generate six switching signals by the common six-step conduction scheme.

2.2 Buck-type current source inverter

In addition, there is always one upper switch and one lower switch at the same time in common six-step commutation and thus, the BDCM can be modelled as a series-connected circuit with an inductance $2L_s$, a resistance $2R_s$ and the voltage e_s as shown in Fig. 4, where L_s and R_s are the winding inductance and the winding resistance, respectively. L_B is the output inductance of the buck converter.

In practice, the current source can be implemented by a buck converter as plotted in Fig. 4 because of the output inductor L_B in the buck converter. The bus current I_d is

$$e_s = \begin{cases} e_a - e_c = \sqrt{3}K_E\omega_r \cos(\theta_e - \pi/6), & \text{when} \quad 2k\pi \le \theta_e < 2k\pi + \pi/3 \\ e_b - e_c = \sqrt{3}K_E\omega_r \cos(\theta_e - \pi/2), & \text{when} \quad 2k\pi + \pi/3 \le \theta_e < 2k\pi + 2\pi/3 \\ e_b - e_a = \sqrt{3}K_E\omega_r \cos(\theta_e - 5\pi/6), & \text{when} \quad 2k\pi + 2\pi/3 \le \theta_e < (2k+1)\pi \\ e_c - e_a = \sqrt{3}K_E\omega_r \cos(\theta_e - 7\pi/6), & \text{when} \quad (2k+1)\pi \le \theta_e < 2k\pi + 4\pi/3 \\ e_c - e_b = \sqrt{3}K_E\omega_r \cos(\theta_e - 3\pi/2), & \text{when} \quad 2k\pi + 4\pi/3 \le \theta_e < 2k\pi + 5\pi/3 \\ e_a - e_b = \sqrt{3}K_E\omega_r \cos(\theta_e - 11\pi/6), & \text{when} \quad 2k\pi + 5\pi/3 \le \theta_e < (2k+2)\pi \end{cases} \quad (2)$$

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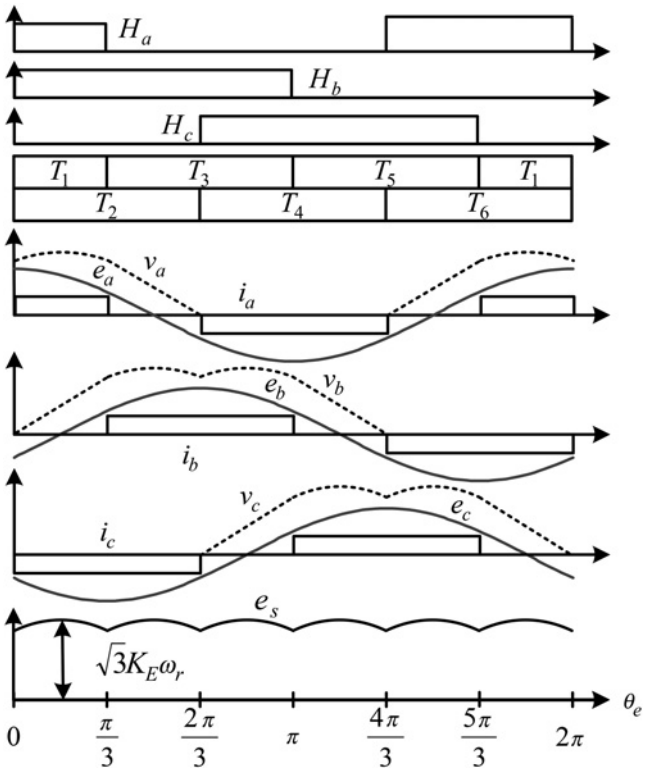

Fig. 3 *Illustrated waveforms for ideal CSI-fed BDCM*

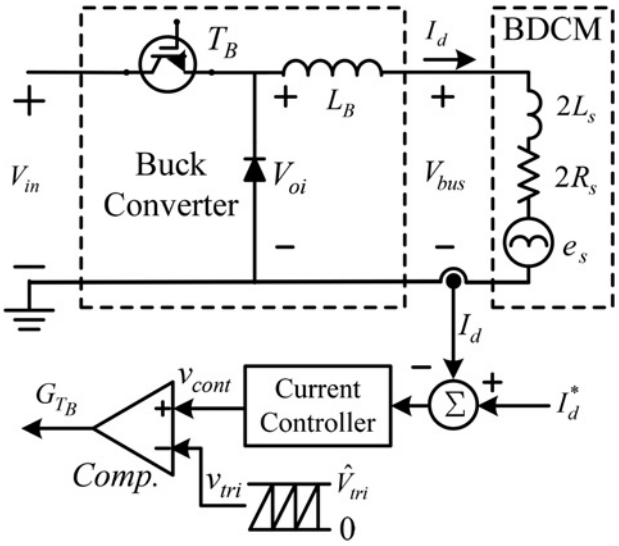

Fig. 4 *Buck-type CSI with equivalent circuit of BDCM*

sensed and a current loop is designed for regulating the bus current I_d to the current reference I_d^*. The gate signal G_{TB} of the controllable switch T_B is obtained from the comparison of the controller output v_{cont} and the fixed-frequency sawtooth signal v_{tri} with a fixed amplitude $\hat{V}_{\mathrm{tri}}$.

The duty ratio d_B of the controllable switch T_B can be expressed as $d_B = v_{\mathrm{cont}}/\hat{V}_{\mathrm{tri}}$ and thus, the average diode voltage $\langle V_{o_i}\rangle_{T_s}$ within the switching period T_{s} becomes

$$\langle V_{o_i}\rangle_{T_s} = \frac{v_{\mathrm{cont}}}{\hat{V}_{\mathrm{tri}}} V_{\mathrm{in}} \tag{5}$$

From Fig. 4, the voltage drop V_{drop} across the inductance $(L_B + 2L_{\mathrm{s}})$ and the resistance $2R_{\mathrm{s}}$ is the difference between the diode voltage V_{o_i} and the equivalent voltage e_s. Thus, the transfer function between the voltage drop V_{drop} and the yielded bus current I_d can be expressed as

$$\frac{I_d(s)}{V_{\mathrm{drop}}(s)} = \frac{1}{(L_B + 2L_s)s + 2R_s} \tag{6}$$

From (6), the equivalent block diagram of Fig. 4 can be plotted in Fig. 5. The current controller $G_{\mathrm{c}}(s)$ is the proportional and integral controller and it can be expressed as

$$G_{\mathrm{c}}(s) = \frac{sk_{\mathrm{cP}} + k_{\mathrm{cI}}}{s} \tag{7}$$

To design the controller parameters, the ratio of the proportional gain k_{cP} and the integral gain k_{cI} is set to be

$$\frac{k_{\mathrm{cP}}}{k_{\mathrm{cI}}} = \frac{\hat{V}_{\mathrm{tri}}}{V_{\mathrm{in}}} \frac{L_B + 2L_s}{2R_s} \tag{8}$$

Then, the transfer function between the yielded bus current I_d and the bus current command I_d^* can be obtained by

$$\frac{I_d(s)}{I_d^*(s)} = \frac{(k_{\mathrm{cI}}/2R_s)}{s + (k_{\mathrm{cI}}/2R_s)} \tag{9}$$

Equation (9) behaves like a low-pass filter with the cut-off frequency $f_{\mathrm{cc}} = k_{\mathrm{cI}}/(4\pi R_{\mathrm{s}})$ in hertz (Hz). Since the frequency of the equivalent voltage e_s is six times the electrical frequency in Hz corresponding to the BDCM speed ω_{r} in revolutions per minutes (rpms). The cut-off frequency f_{cc} in Hz should be carefully selected between one tenth the PWM frequency ($f_{\mathrm{tri}}/10$) and six times the electrical frequency of the maximum BDCM speed

$$6 \times \frac{P}{2} \times \frac{\omega_{\mathrm{r,MAX}}}{60} = \frac{P\omega_{\mathrm{r,MAX}}}{20} \le f_{\mathrm{cc}} \le \frac{f_{\mathrm{tri}}}{10} \tag{10}$$

where $\omega_{\mathrm{r,MAX}}$ is the maximum operating speed of BDCM in rpm.

2.3 Terminal voltages of CSI-fed BDCM

When both T_1 and T_2 are conducting (i.e. $0 \le \theta_e < \pi/3$), the bus current I_d flows through T_1 and T_2. It shows that both *a*- and *c*-phase windings can be seen as the excited phases and the *b*-phase winding is seen as the floating phase. The equivalent circuit with turning on and turning off the switch T_B are plotted in Figs. 6*a* and *b*, respectively. With

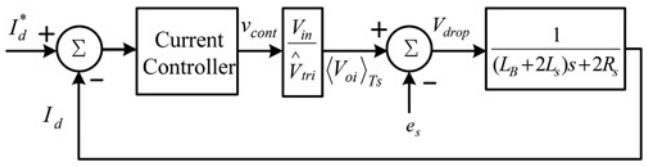

Fig. 5 *Equivalent block diagram for the circuit in Fig. 4*

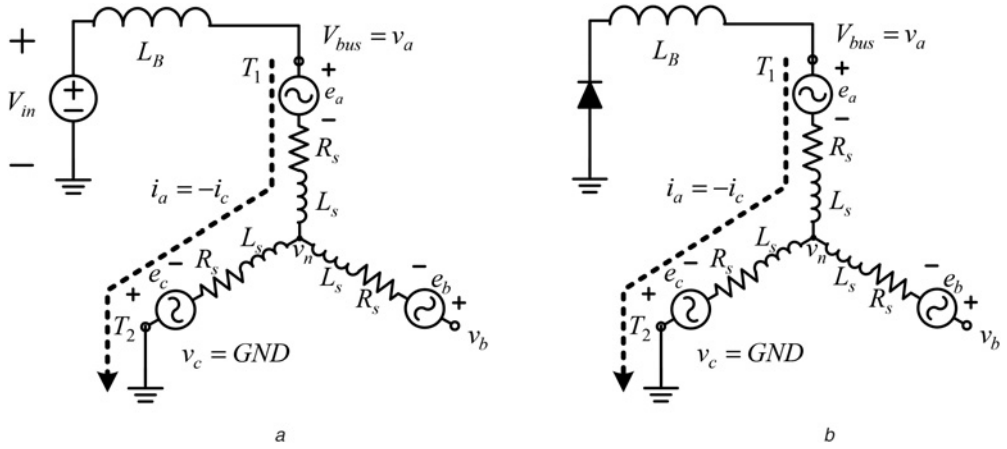

Fig. 6 *Circuit and the current flowing path*

a With turning on T_B
b With turning off T_B

consideration of the conducting state of the switch T_B, the terminal voltages v_a and v_b may be expressed as the following two equations, respectively

$$v_a = \left(G_{\mathrm{TB}} V_{\mathrm{in}} - e_a + e_c - 2I_d R_s\right) \frac{2L_s}{L_B + 2L_s} + \left(e_a - e_c\right) + 2I_d R_s \quad 0 \le \theta_e \le \frac{\pi}{3} \tag{11}$$

$$v_{\mathrm{b}} = \left(G_{\mathrm{TB}} V_{\mathrm{in}} - e_a + e_c - 2I_d R_s\right) \frac{L_s}{L_B + 2L_s} + \left(e_b - e_c\right) + I_d R_s \quad 0 \le \theta_e \le \frac{\pi}{3} \tag{12}$$

where the switching signal G_{TB} is

$$G_{\mathrm{TB}} = \begin{cases} 1, & \text{when } v_{\mathrm{cont}} > v_{\mathrm{tri}} \text{ and the switch } T_B \text{ turns on} \\ 0, & \text{when } v_{\mathrm{cont}} < v_{\mathrm{tri}} \text{ and the switch } T_B \text{ turns off} \end{cases} \tag{13}$$

By neglecting the voltage drop across the equivalent resistance R_{s}, the terminal voltages in (11) and (12) can be simplified to be

$$v_a \simeq G_{\mathrm{TB}} V_{\mathrm{in}} \frac{2L_s}{L_B + 2L_s} + e_a \frac{L_B}{L_B + 2L_s} - e_c \frac{L_B}{L_B + 2L_s} \quad 0 \le \theta_e \le \frac{\pi}{3} \tag{14}$$

$$v_{\mathrm{b}} \simeq G_{\mathrm{TB}} V_{\mathrm{in}} \frac{L_s}{L_B + 2L_s} - e_a \frac{L_s}{L_B + 2L_s} + e_b - e_c \frac{L_B + L_s}{L_B + 2L_s} \quad 0 \le \theta_e \le \frac{\pi}{3} \tag{15}$$

From (14) and (15), it is clear that the switching signal G_{TB} contributes to the voltage ripples in the terminal voltages. From (14), the voltage ripple $2L_{\mathrm{s}}V_{\mathrm{in}}/(L_B + 2L_{\mathrm{s}})$ in the terminal voltage v_a is double the ripple $L_{\mathrm{s}}V_{\mathrm{in}}/(L_B + 2L_{\mathrm{s}})$ in the terminal voltage v_{b}. The illustrated waveforms for buck-type CSI-fed BDCM are plotted in Fig. 7. The ripple in the bus voltage V_{bus} is fixed and equal to $2L_{\mathrm{s}}V_{\mathrm{in}}/(L_B + 2L_{\mathrm{s}})$.

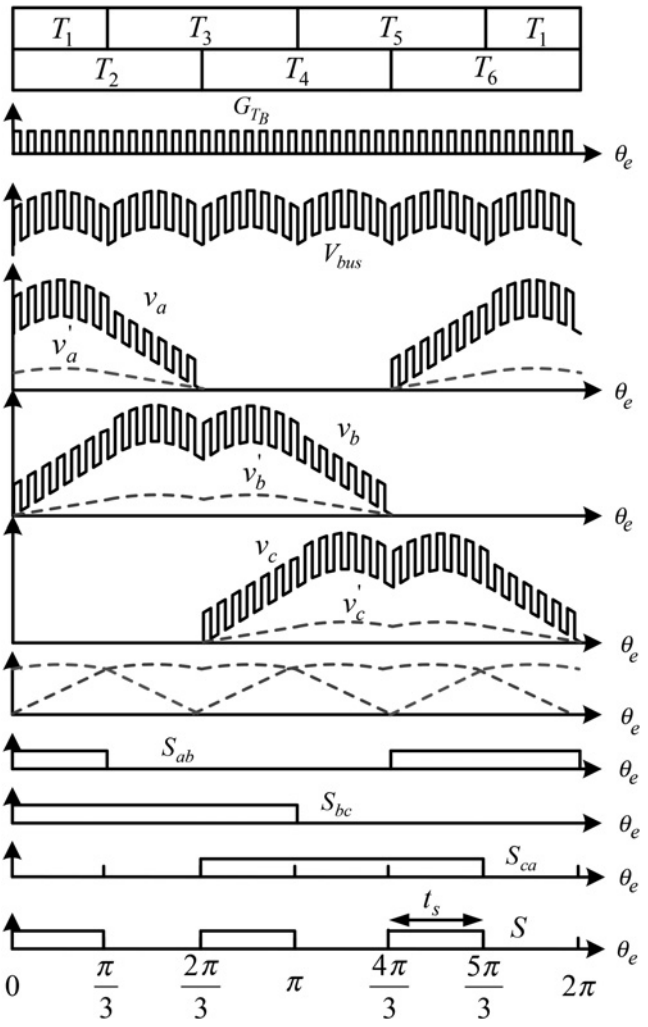

Fig. 7 *Illustrated waveforms for buck-type CSI-fed BDCM*

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3 Position sensorless control for buck-type CSI-fed BDCM

The proposed position sensorless control for buck-type CSI-fed BDCM is plotted in Fig. 8, where a buck converter is connected in front of the common CSI inverter. There are seven switches $T_1 \sim T_6$ and T_B in the buck-type CSI. The gate signal of switch T_B is generated from the comparison of the current controller output $v_{\rm cont}$ and the sawtooth signal $v_{\rm tri}$. The other gate signals are obtained from three commutation signals $S_{\rm ab}$, $S_{\rm bc}$ and $S_{\rm ca}$. Their generating rules are as follows

$$G_{T_1} = S_{\rm ab} \cdot \overline{S_{\rm ca}} \tag{16}$$

$$G_{T_2} = S_{\rm bc} \cdot \overline{S_{\rm ca}} \tag{17}$$

$$G_{T_3} = S_{\rm bc} \cdot \overline{S_{\rm ab}} \tag{18}$$

$$G_{T_4} = S_{\rm ca} \cdot \overline{S_{\rm ab}} \tag{19}$$

$$G_{T_5} = S_{\rm ca} \cdot \overline{S_{\rm bc}} \tag{20}$$

$$G_{T_6} = S_{\rm ab} \cdot \overline{S_{\rm bc}} \tag{21}$$

The low-pass filter circuits composed of the capacitance C_2 and the resistances R_1 are used to sense the three terminal voltages and to generate three filtered signals v'_a, v'_b and v'_c. Then, the three signals $S_{\rm ab}$, $S_{\rm bc}$ and $S_{\rm ca}$ are obtained by comparing two of the three filtered signals v'_a, $v'_{\rm b}$ and v'_c.

In order to attenuate the PWM voltage ripple across the terminal voltages, the cut-frequency $f_{\rm LP} = (R_1 + R_2)/(CR_1R_2)$ of the low-pass filter is selected between the switching frequency $f_{\rm tri}$ in Hz and ten times the electrical frequency corresponding to the maximum BDCM speed $\omega_{\rm r,\ MAX}$.

$$f_{\rm tri} > f_{\rm LP} \geq 10 \times \frac{P}{2} \times \frac{\omega_{\rm r,MAX}}{60} = \frac{P\omega_{\rm r,MAX}}{12} \tag{22}$$

Assume that the PWM voltage ripples are filtered out without introducing phase delay by the low-pass filter. From (14) and (15), the filtered signals v'_a and $v'_{\rm b}$ can be simplified to be

$$v'_a = \frac{R_2}{R_1 + R_2}\frac{L_B}{L_B + 2L_s}(e_a - e_c) \quad 0 \leq \theta_e \leq \frac{\pi}{3} \tag{23}$$

$$v'_{\rm b} = \frac{R_2}{R_1 + R_2}\frac{L_B}{L_B + 2L_s}(e_b - e_c) + \frac{R_2}{R_1 + R_2}\frac{L_s}{L_B + 2L_s}(2e_b - e_a - e_c) \quad 0 \leq \theta_e \leq \frac{\pi}{3} \tag{24}$$

By selecting the buck inductance much larger than the winding inductance $L_B \gg L_s$, the second term in (24) can be neglected and the filtered signal $v'_{\rm b}$ of the floating phase can be expressed as

$$v'_{\rm b} \simeq \frac{R_2}{R_1 + R_2}\frac{L_B}{L_B + 2L_s}(e_b - e_c) = A_v(e_b - e_c) \quad 0 \leq \theta_e \leq \frac{\pi}{3} \tag{25}$$

where $A_v = R_2/(R_1 + R_2)$ is the gain factor.

According to the various conducting states, the expressions of the filtered signals are tabulated in Table 1, and they are also illustrated in Fig. 7. It is clear that the commutating instants occur at the crossing points of the three filtered

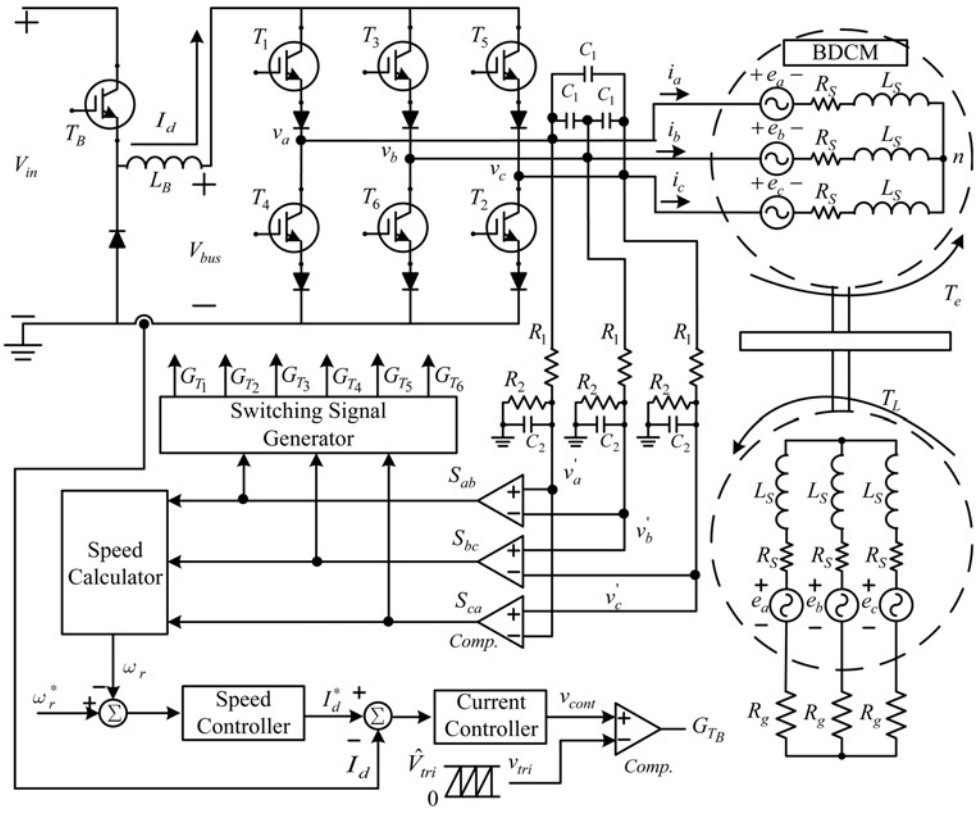

Fig. 8 *Proposed position sensorless control for buck-type CSI-fed BDCM*

Table 1 Filtered signals in various conducting states

	v'_a	v'_b	v'_c
T_1, T_2	$A_v(e_a - e_c)$ exciting phase	$A_v(e_b - e_c)$ floating phase	0 exciting phase
T_2, T_3	$A_v(e_a - e_c)$ floating phase	$A_v(e_b - e_c)$ exciting phase	0 exciting phase
T_3, T_4	0 exciting phase	$A_v(e_b - e_a)$ exciting phase	$A_v(e_c - e_a)$ floating phase
T_4, T_5	0 exciting phase	$A_v(e_b - e_a)$ floating phase	$A_v(e_c - e_a)$ exciting phase
T_5, T_6	$A_v(e_a - e_b)$ floating phase	0 exciting phase	$A_v(e_c - e_b)$ exciting phase
T_6, T_1	$A_v(e_a - e_b)$ exciting phase	0 exciting phase	$A_v(e_c - e_b)$ floating phase

signals. Therefore the signals S_{ab}, S_{bc} and S_{ca} can be used to generate the switching signals in (16)–(21).

By using the exclusive (XOR) operator, the signal S is generated from three commutation signals S_{ab}, S_{bc} and S_{ca} by

$$S = S_{ab} \otimes S_{bc} \otimes S_{ca} \tag{26}$$

where $\otimes$ is the common XOR operator. Then, the period t_S (in s) between the rising/falling edges of the combined signal S is counted and the BDCM speed ω_r in rpm is calculated by

$$\omega_r = \frac{1}{t_s \times 6} \times \frac{2}{P} \times 60 = \frac{20}{P \times t_s} \tag{27}$$

Three AC capacitors C_1 are connected across the BDCM terminals to provide flowing path for the commutation currents. However, the commutation currents flow through the capacitors and may make the terminal voltages either smaller than zero or larger than the bus voltage V_{bus}. So, each switch is connected with a diode in series to withstand the negative voltage because of the commutation currents.

When both T_4 and T_5 are conducting (i.e. $\pi \le \theta_e < 4\pi/3$), the bus current I_d flowing through T_4 and T_5, and the terminal voltage is zero $v_a = 0$ as shown in Fig. 9*a*. Since the bulky inductance is selected $L_B \gg L_s$, the bus current can be seen as a current source in Fig. 9. After turning on the switch T_6 and turning off the switch T_4, the commutation current i_{CC} may flow through the capacitor and lift the terminal voltage v_a until the commutation current i_{CC} decays to zero. The steady-state equivalent circuit during turning on both T_5 and T_6 (i.e. $4\pi/3 \le \theta_e < 5\pi/3$) is plotted in Fig. 9*b*.

From Fig. 3, the induced voltages of phases *a* and *b* is closed to each other $e_a \simeq e_b$ at the commutation instant $\theta_e = 4\pi/3$, and thus, the Kirchhoff voltage law (KVL) equation for the commutation current path can be expressed as

$$2L_s \frac{\mathrm{d}i_{CC}(t)}{\mathrm{d}t} + 2R_s i_{CC}(t) + \frac{1}{C_1}\int i_{CC}(t)\mathrm{d}t \simeq 0 \tag{28}$$

The commutation current i_{CC} has initial value I_d at the beginning of the current commutation, and the initial energy E stored in the inductance L_s can be expressed as

$$E \simeq \frac{1}{2} L_s I_d^2 \tag{29}$$

Assume quarter energy E is transferred to the capacitance C_1, and then dissipated by the resistances. The peak terminal voltage during the commutation instant $\theta_e = 4\pi/3$ would be

$$v_{pk} \simeq I_d \sqrt{\frac{L_s}{4C_1}} \tag{30}$$

Therefore the capacitance C_1 should be selected as

$$C_1 > \frac{L_s I_d^2}{4(v_{limit})^2} \tag{31}$$

where v_{limit} is the maximum voltage with consideration of the diode blocking voltage.

When permanent magnet synchronous motor (PMSM) is standstill, the back-EMFs are zero and the proposed sensorless control needs starting strategy [18]. The proposed starting strategy plotted in Fig. 10 is divided into constant current mode (CCM) and constant speed mode (CSM). In CCM, the bus current command is given by $I_d^* = I_1$ and the currents commutate with an increasing frequency until the rotor runs at the constant speed ω_1 in rpm. After a given time t_1, the operating mode changes from CCM to CSM.

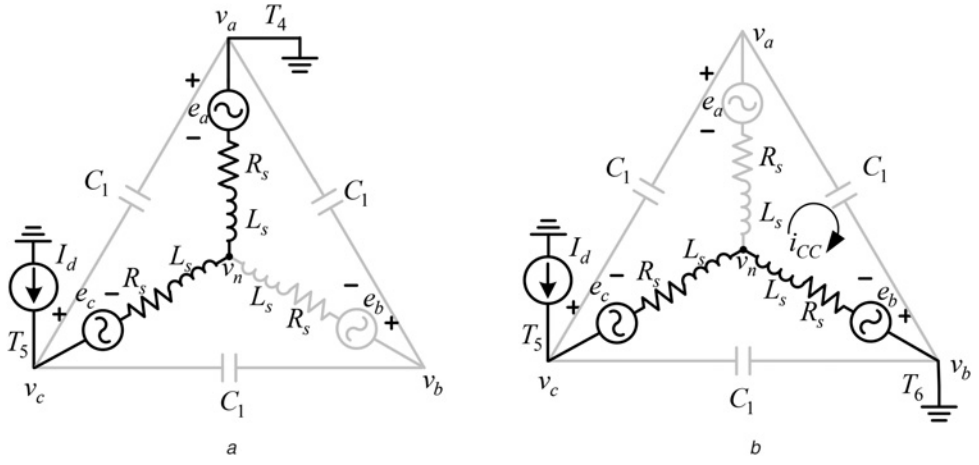

Fig. 9 *Steady-state current flowing path*

a When both T_4 and T_5 are conducting
b When both T_5 and T_6 are conducting

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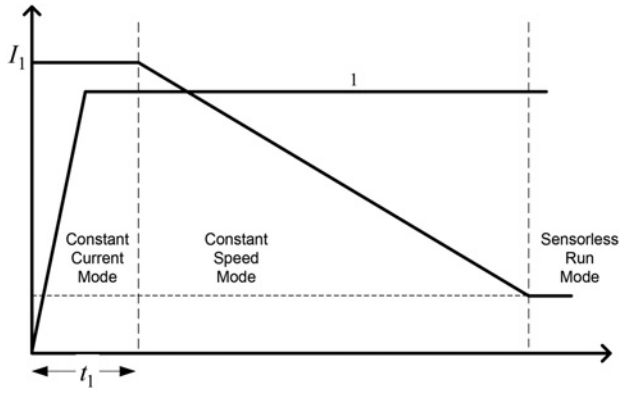

Fig. 10 *Operating modes during start-up*

In CSM, the bus current command I_d^* decreases linearly, but the currents commutate with fixed frequency. At the same time, the rotor speed ω_r is calculated and checked if the difference between the speeds ω_1 and ω_r is near zero. Once the speed difference $|\omega_1 - \omega_r|$ is smaller than 30 rpm, the operation mode will change from CSM to the sensorless run mode (SRM).

Table 2 Simulated parameters of buck-type CSI and BDCM

BDCM stator resistance/phase	$R_s = 0.3\ \Omega$
BDCM stator inductance/phase	$L_s = 1.7$ mH
BDCM pole number	$P = 8$
BDCM maximum speed	$\omega_{r,MAX} = 2000$ rpm
BDCM voltage gain	$K_E = 75$ V/krpm
buck input voltage	$V_{in} = 300$ V
buck inductor	$L_B = 20$ mH
buck switching frequency	$f_{tri} = 10$ kHz
CSI output capacitor	$C_1 = 0.033\ \mu$F

In SRM, the currents commutate according to the commutation signals S_{ab}, S_{bc} and S_{ca}, and the bus current command I_d^* is obtained from the speed controller.

4 Simulation results

In this section, some simulation results are provided and the simulated parameters are shown in Table 2. A eight-pole BDCM with the resistance $R_s = 0.3\ \Omega$ and the inductance $L_s = 1.7$ mH is used, and its maximum operating speed is $\omega_{r,MAX} = 2000$ rpm (i.e. 133.33 Hz in electrical frequency). According to (22) and the parameters in Table 2, the cut-off

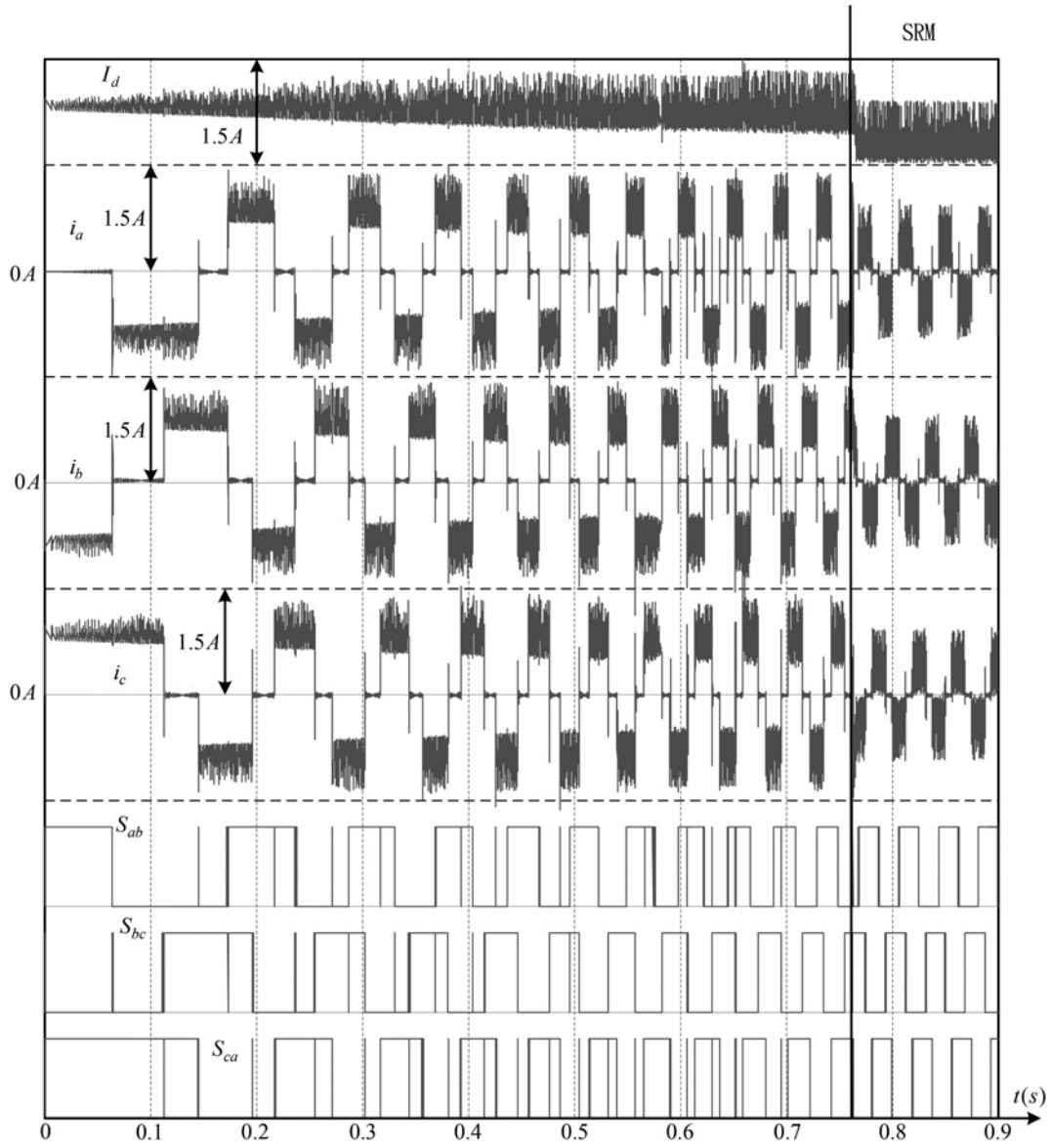

Fig. 11 *Simulated waveform during the starting process*

frequency f_{LP} must be within the range

$$1.333\,\text{kHz} \le f_{LP} = \frac{R_1 + R_2}{R_1 R_2 C_2} \le 10\,\text{kHz} \qquad (32)$$

After choosing the gain factor $A_v = 0.07$ in (25) and the cut-off frequency $f_{LP} = 3$ kHz from (32), the parameters for the terminal voltage sensing circuit are obtained by $R_1 = 130$ kΩ, $R_2 = 7.5$ kΩ and $C_2 = 0.047$ μF.

Since the blocking voltage of the diode is 600 V and the maximum amplitude of the square-wave current is 5 A, the CSI AC capacitor is selected with $C_1 = 0.033$ μF from (31).

As shown in Fig. 8, two identical BDCMs are used and their shafts are coupled together to become a motor-generator set. One BDCM is connected to CSI, and the other is connected to the *Y*-connected resistors R_g. Therefore both BDCMs have the same motor speed $\omega_r = 2000$ rpm and the same BDCM induced voltages e_a, e_b and e_c.

The waveforms during the starting process are plotted in Fig. 11 and the used parameters are $I_1 = 1$ A and $\omega_1 = 400$ rpm. BDCM is successfully changed from CCM and CSM to SRM. The simulated waveforms of the speed command $\omega_r^* = 2000$ rpm with load resistors $R_g = 100\,\Omega$ and $R_g = 33.3\,\Omega$ are plotted in Figs. 12*a* and *b*, respectively.

The buck current I_d is well regulated and the yielded motor current i_a is in phase with the induced voltage e_a. Owing to CSI, the rising time and the falling time of the square-wave currents are relatively small. But the peak of the bus voltage V_{bus} increases with the yielded bus current I_d.

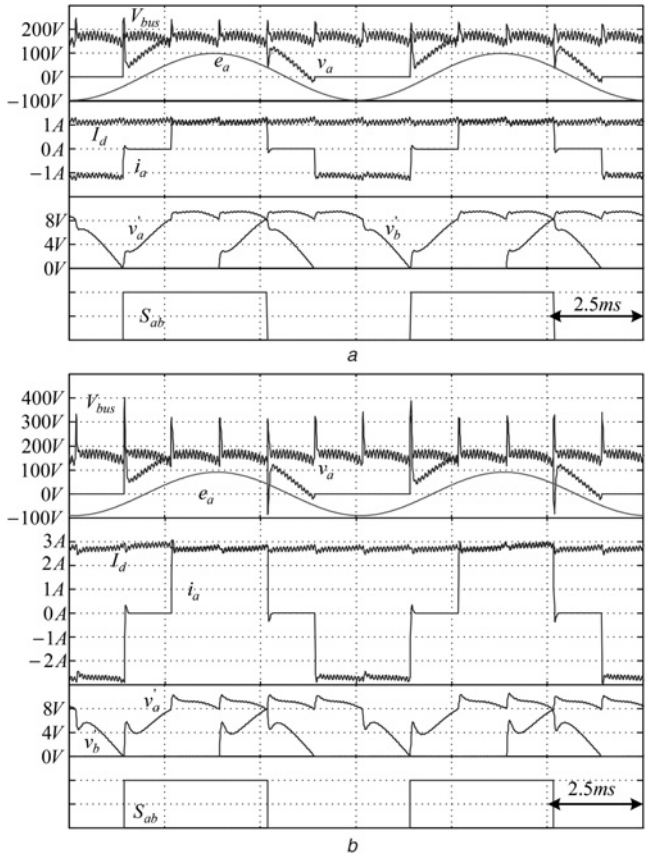

Fig. 12 *Simulated results for the proposed position sensorless control*

a $\omega_r = 2000$ rpm and $R_g = 100\,\Omega$
b $\omega_r = 2000$ rpm and $R_g = 33.3\,\Omega$.

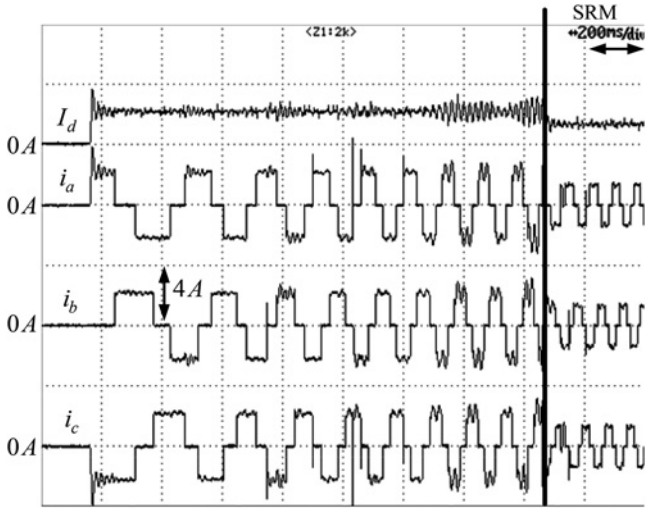

Fig. 13 *Waveforms during the starting process*

From Fig. 12, the terminal voltage v_a may change rapidly because of the commutating current i_{CC} illustrated in Fig. 9. In Fig. 12*b*, the peak of the terminal voltage v_a may be 400

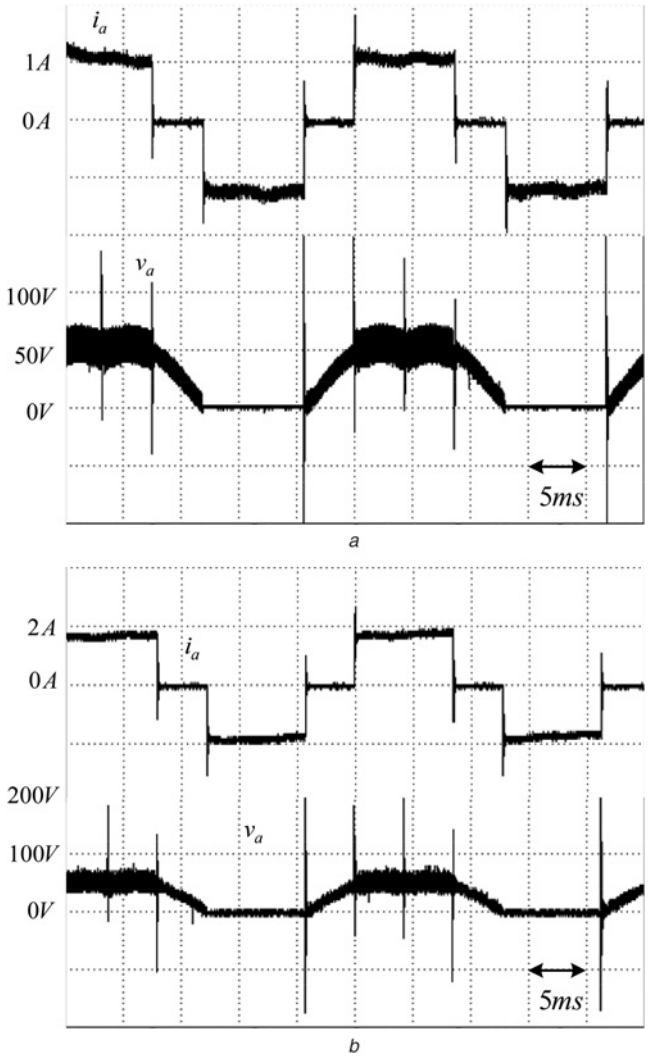

Fig. 14 *Experimental results for the proposed position sensorless control*

a $\omega_r = 500$ rpm and $R_g = 100\,\Omega$
b $\omega_r = 500$ rpm and $R_g = 33.3\,\Omega$

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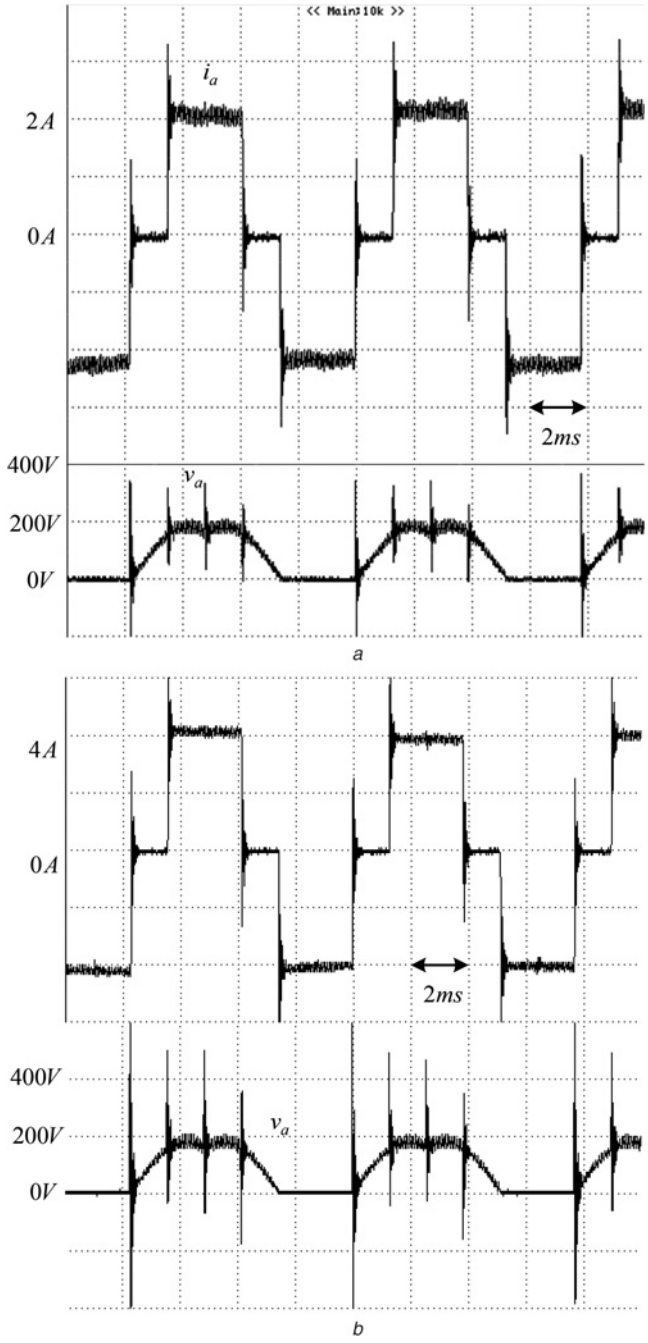

Fig. 15 *Experimental results for the proposed position sensorless control*

a $\omega_r = 2000$ rpm and $R_g = 100\ \Omega$
b $\omega_r = 2000$ rpm and $R_g = 33.3\ \Omega$

and -100 V. It means that the switch voltage may be negative. Since the controllable semiconductor devices are not able to withstand the negative voltage, the diodes are connected to the switches in series to provide the bipolar withstanding ability.

5 Experimental results

The proposed position sensorless control is implemented in a FPGA-based system. The nominal parameters are the same as those in Table 2. Owing to no A/D and no D/A function in commercial FPGA XC3S200 chip, an external A/D converter is used to sense the current input and some D/A converters are used to show the control variables in the scope.

The waveforms during the starting process are plotted in Fig. 13. After 1.5 s, BDCM successfully enters into SRM. The experimental waveforms of the speed command $\omega_r^* = 500$ rpm with load resistors $R_g = 100\ \Omega$ and $33.3\ \Omega$ are plotted in Figs. 14*a* and *b*, respectively. BDCM runs stably at 500 rpm with various loads.

From (14) and (15), the ripple of the terminal voltage during the exciting and the floating phases can be calculated to be 43.6 and 21.8 V, respectively, which meets the observations from the experimental waveforms. From Fig. 14*b*, the peak voltage appearing in the terminal voltage v_a are near 200 and -100 V, which are smaller than the diode blocking voltage 600 V. Thus, the voltage pulse would not damage to the switch.

The experimental waveforms of the speed command $\omega_r^* = 2000$ rpm with load resistors $R_g = 100\ \Omega$ and $33.3\ \Omega$ are plotted in Figs. 15*a* and *b*, respectively, which shows that the proposed position sensorless control for BDCM runs stably at 2000 rpm with various loads.

From Fig. 15*b*, the peak voltage appears in the terminal voltage v_a are near 600 and -400 V, which are smaller than the diode blocking voltage 600 V. Thus, the voltage pulse would not damage to the CSI circuit.

From Figs. 14 and 15, the voltage ripples in the terminal voltage are fixed, which also demonstrates the derived (14) and (15). In (14) and (15), the profile of the voltage ripples because of the switching signal G_{TB} is fixed regardless of the BDCM speed ω_r.

6 Conclusions

In this paper, the behaviour of the buck-type CSI has been studied and the design rules for the buck inductor and the output AC capacitors have been provided. Additionally, the position sensorless control method with square-wave currents for buck-type CSI-fed BDCM has been proposed. The provided simulation and experimental results show that the proposed position sensorless control works stably.

7 References

1 Lelkes, A., Krotsch, J., De Doncker, R.W.: 'Low-noise external rotor BLDC motor for fan applications'. Proc. IAS, 2002, pp. 2036–2042
2 Wang, C.M., Wang, S.J., Lin, S.K., Lin, H.Y.: 'A novel twelve-step sensorless drive scheme for a brushless DC motor', *IEEE Trans. Magn.*, 2007, **43**, (6), pp. 2555–2557
3 Chen, H.C., Chang, Y.C., Huang, C.K.: 'Practical sensorless control for inverter-fed BDCM compressors', *IET Electr. Power Appl.*, 2007, **1**, (1), pp. 127–132
4 Lee, K.W., Kim, D.K., Kim, B.T., Kwon, B.I.: 'A novel starting method of the surface permanent-magnet BLDC motors without position sensor for reciprocating compressor', *IEEE Trans. Ind. Appl.*, 2008, **44**, (1), pp. 85–92
5 Shao, J.: 'An improved microcontroller-based sensorless brushless DC (BLDC) motor drive for automotive applications', *IEEE Trans. Ind. Appl.*, 2006, **42**, (5), pp. 1216–1221
6 Wu, Z., Su, G.-J.: 'High-performance permanent magnet machine drive for electric vehicle applications using a current source inverter'. Annual Conf. IEEE Industrial Electronics Society (IECON), November 2008, p. 2812
7 Tang, L., Su, G.J.: 'Boost mode test of a current-source-inverter-fed permanent magnet synchronous motor drive for automotive applications', *Control Model. Power Electron.* (COMPEL), 2010, pp. 1–8
8 Park, J.W., Hwang, S.H., Kim, J.M.: 'Sensorless control of brushless DC motors with torque constant estimation for home applications', *IEEE Trans. Ind. Appl.*, 2012, **48**, (2), pp. 677–684
9 Han, Q., Samoylenko, N., Jatskevich, J.: 'Average-value modeling of brushless DC motors with 120° voltage source inverter', *IEEE Trans. Energy Convers.*, 2008, **23**, (2), pp. 423–432

10 Singh, B., Singh, S.: 'Single-phase power factor controller topologies for permanent magnet brushless DC motor drives', *IET Power Electron.*, 2010, **3**, (2), pp. 147–175
11 Lin, C.T., Huang, C.W., Liu, C.W.: 'Position sensorless control for four-switch three-phase brushless DC motor drives', *IEEE Trans. Power Electron.*, 2008, **23**, (1), pp. 438–444
12 Gu, B., Nam, K.: 'A DC-link capacitor minimization method through direct capacitor current control', *IEEE Trans. Ind. Appl.*, 2006, **42**, (2), pp. 573–581
13 Chen, H.C., Liaw, C.M.: 'Current-mode control of sensorless BDCM drive with intelligent commutation tuning', *IEEE Trans. Power Electron.*, 2002, **17**, (5), pp. 747–756
14 Su, G.J., Mckeever, W.: 'Low-cost sensorless control of brushless DC motors with improved speed range', *IEEE Trans. Power Electron.*, 2004, **19**, (2), pp. 296–302
15 Kim, D.K., Lee, K.W., Kwon, B.I.: 'Commutation torque ripple reduction in a position sensorless brushless DC motor drive', *IEEE Trans. Power Electron*., 2006, **21**, (6), pp. 1762–1768
16 Lai, Y.S., Lin, Y.K.: 'Novel back-EMF detection technique of brushless DC motor drives for wide range control without using current and position sensors', *IEEE Trans. Power Electron*., 2008, **23**, (2), pp. 934–940
17 Damodharan, P., Vasudevan, K.: 'Sensorless brushless DC motor drive based on the zero-crossing detection of back electromotive force (EMF) from the line voltage difference', *IEEE Trans. Energy Convers.*, 2010, **25**, (3), pp. 661–668
18 Wang, Z., Lu, K., Blaabjerg, F.: 'A simple start-up strategy based on current regulation for back-EMF-based sensorless control of PMSM', *IEEE Trans. Power Electron*., 2012, **27**, (8), pp. 3817–3825

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