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Al-SiO_2-Y_2O_3-SiO_2-poly-Si Thin-Film Transistor Nonvolatile Memory Incorporating a Y_2O_3 Charge Trapping Layer

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In this letter, we investigate the structural properties and electrical characteristics of the Al–SiO_2–Y_2O_3–SiO_2–poly-Si (AOYOP) thin-film transistor (TFT) nonvolatile memory device. The composition of Y_2O_3 charge-trapping layer was analyzed using X-ray photoelectron spectroscopy. The Y_2O_3 AOYOP TFT memory device exhibited a large memory window of 2.5 V, a long charge retention time of ten years with a minimal charge loss of ∼15%, and a better endurance performance for P/E cycles up to 10^5.
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Low-temperature polycrystalline silicon thin-film transistors (LTPS-TFTs) are widely used for active matrix liquid crystal display and active matrix organic light emitting diode.[1] With the rapid advance in the manufacturing technologies, the extent and complexity of circuit integration have been tremendously increased. The realization of integrating an entire system on the top of the panel is then being rigorously pursued by low-temperature process.[2,3] With the increasing demand of system reconfigurability in advanced system-on-chip (SOC), many different memory functions are necessitated.[4–6] Specifically, non-volatile memory (NVM) is crucial and, therefore, careful choice of the best NVM device to be integrated in the system is most important. Silicon–oxide–nitride–oxide–silicon (SONOS)–type flash memory device has received a considerable amount of interest in the electronics industry because of its non-volatility, low power consumption, and fast speed.[7,8] However, the erase saturation phenomenon and vertical stored charge migration[9,10] for conventional SONOS–type memory open critical issues in device performance and reliability.

Various technologies have been developed for improving the performance and reliability of SONOS–type memory. Chen et al. developed a bandgap engineering of SiN_x film to improve the retention and endurance characteristics.[11] Lin et al. suggested the Hf-silicate film as the charge trapping layer deposited by cosputtering method for achieving long retention time and good endurance.[12] Recently, we have proposed and demonstrated an yttrium oxide (Y_2O_3) film as a good candidate for charge trapping layer in flash memory technology.[13,14] However, Y_2O_3 thin film integrated in LTPS-TFT memory device has not been reported. Moreover, Y_2O_3 film can also be considered as one of the most promising candidate materials for LTPS-TFT memory applications due to its large dielectric constant (13∼17) and wide bandgap energy (5.6 eV).[15,16] In this letter, we explore the structural properties and electrical characteristics of the Al–SiO_2–Y_2O_3–SiO_2–poly–Si (AOYOP) TFT nonvolatile memory device integrated with an Y_2O_3 charge trapping layer. This memory exhibits good electrical characteristics, including large memory window, good retention time, and high endurance.

Experimental

The cross sectional view of the Y_2O_3 AOYOP TFT nonvolatile memory is illustrated in Fig. 1a. First, a 500 nm-thick thermal oxide was grown on the Si wafer by wet oxidation system to substitute the glass substrate. A 50 nm-thick amorphous-Si (α-Si) film for the channel region was deposited at 550°C by a low-pressure chemical vapor deposition (LPCVD) system. Subsequently, solid-phase crystallization was performed at 600°C for 24 h in N_2 ambient for polycrystalline channel formation. The source and drain (S/D) regions were doped by phosphorous ion implantation with a dose of 5×10^{15} ions/cm^{-2} at 17 keV, then activated by furnace at 600°C for 24 h. A ∼10 nm tetraethyloxysilane (TEOS) silicon oxide film as a tunneling layer was deposited through LPCVD system. A ∼3 nm-thick Y_2O_3 film was then deposited on the tunneling oxide by a physical vapor deposition system. Another thin film of ∼20 nm SiO_2 as a blocking oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350°C. After creating the contact holes at S/D region, a 500 nm-thick Al was deposited by physical vapor deposition and patterned for gate and S/D contact pads. The length and width of the n-channel AOYOP TFT memory device were 10 and 10 μm, respectively. The threshold voltage (V_{TH}) values are obtained from the current-voltage (transfer characteristics) curves at a fixed drain current value of 100 nA (100 × W/L nA).

Results and Discussion

In order to analyze the physical properties of yttria charge trapping layer, the chemical elements were detected by X-ray photoemission spectroscopy (XPS). Figs. 1b and 1c show the Y 3d and O 1s spectra, respectively, of the Y_2O_3 charge trapping film with their appropriate peak curve-fitting lines. The Y 3d double peaks (157.2 eV and 159.3 eV) shifted to higher binding energy by 0.4 eV relative to the Y_2O_3 reference position (156.8 eV and 158.9 eV).[17] It may be attributed to the formation of a silicate layer at the Y_2O_3-SiO_2 interface. Fig. 1c depicts that the O 1s spectra of Y_2O_3 film can be deconvoluted into three peaks located at 529.5, 531.8, and 533 eV, corresponding to Y_2O_3, Y-silicate, and SiO_2,[17] respectively. The intensity of O 1s peak corresponding to silicate layer was larger compared to other peaks, indicating the formation of a thicker silicate layer between the Y_2O_3 and SiO_2 interface.

Fig. 2a shows the transfer characteristics of the Y_2O_3 AOYOP TFT memory device following the P/E operations. The AOYOP TFT memory device exhibited good transistor behavior with a high I_{on}/I_{off} ratio of 5.3×10^6. The field-effect mobility of 15.32 cm$^2 \cdot$V$^{-1} \cdot$s^{-1} and a subthreshold swing of 1.34 V/dec were obtained in the AOYOP TFT memory device. The TFT memory device was programmed by channel hot electron (CHE) injection method, whereas the erasing was carried out by band-to-band hot hole (BTBHH) injection to the device. After programming at the V_{GS} of 10 V and the V_{DS} of 10 V for 1 s, the threshold voltage shifted from 3.4 V (fresh device) to 5.6 V (programmed state). This can be attributed to the electron trapping in the charge trapping layer in the TFT memory device. The electron trapping can be explained by considering the band diagram presented in Fig. 2b. The conduction band offset between the tunneling oxide and the Y_2O_3 charge trapping layer is 2.3 eV. The large electric field in the poly-Si channel of the TFT device creates impact ionized hot-electrons whose energy when exceeds the gate-oxide potential barrier (3.1 eV) can be injected to the gate oxide and Y_2O_3 charge trapping layer. This electron trapping causes the I_{DS}-V_{GS} curve in Fig. 2a to move to the right, and thus increasing the V_{TH} value after programming. After erase operation of the TFT memory device, we can clearly observe that the I_{DS}-V_{GS} curve did not fully recover to the initial transfer characteristic. This behavior might be due to the mismatch between the localized spatial distributions for the injected electrons and holes by using CHE programming and BTBHH erasing. The uncompensated

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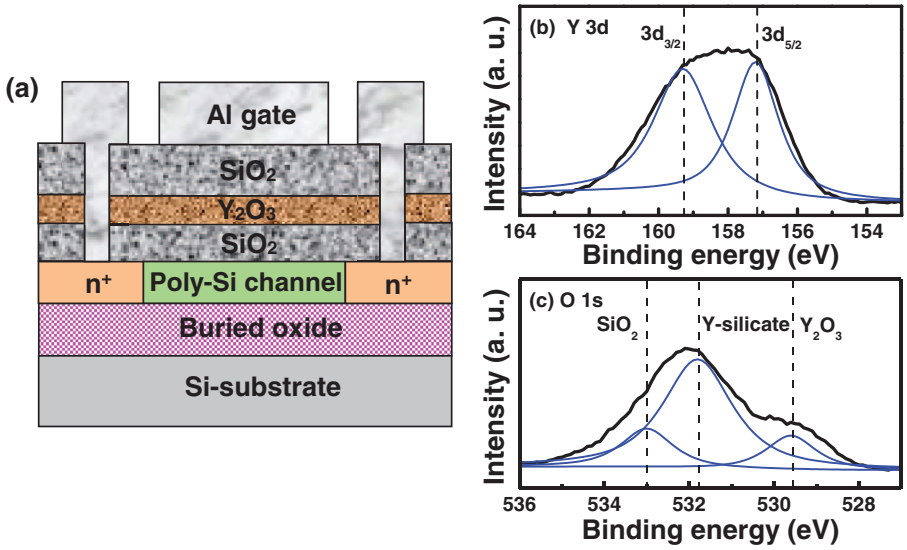

Figure 1. (a) Cross-sectional view of the AOYOP TFT device memory structure using a Y_2O_3 charge trapping layer. XPS spectra of (b) Y 3d and (c) O 1s for Y_2O_3 charge trapping layers.

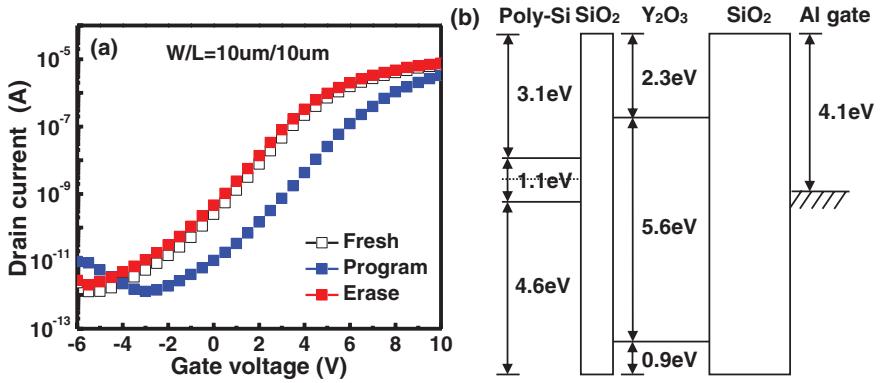

Figure 2. (a) Transfer characteristics of the AOYOP TFT memory device. (b) Band diagram of the AOYOP TFT memory.

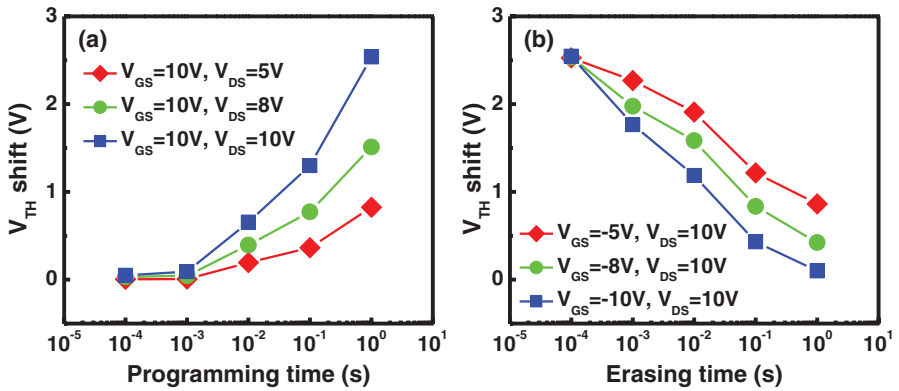

Figure 3. (a) Programming and (b) erasing characteristics of AOYOP TFT memory devices.

charge will then cause the V_{TH} to shift. Moreover, another important parameter for memory read-out operation in the TFT memory device is the difference between the programming current (I_{PR}) and the erasing current (I_{ER}) at certain reading voltage. The I_{PR}/I_{ER} current ratio of programmed and erased state in AOYOP TFT device at the read-out voltage of 2 V is more than two-orders-of magnitude, which suffices for nonvolatile memory applications.

Figure 3a demonstrates the program speed of the AOYOP TFT memory device, performed under three different stress conditions at V_{DS} of 5, 8, and 10 V and V_{GS} of 10 V for CHE programming. The V_{TH} shift is defined as the change in the threshold voltage of a TFT memory device between the programmed and the erased states. At the larger programming bias at $V_{GS} = V_{DS} = 10$ V for 1 s programming, we observed a large V_{TH} shift of ~2.5 V. It is also observed that the V_{TH} shift increases with the increase of applied drain voltage. This is because a large amount of "hot" electrons were generated when a larger drain voltage was applied, and thus more electrons were capable of crossing the barrier height to become trapped in the Y_2O_3 layer. The erase speed behaviors of the AOYOP TFT memory device were also presented in Fig. 3b. We can clearly observe significant increase of programming and erasing speed for higher drain and gate voltage, respectively.

Fig. 4a shows the retention characteristics of the AOYOP TFT memory devices at room temperature and 85°C. The retention measurement was performed after the CHE programming. The normalized V_{TH} shift is defined as the ratio of V_{TH} shift at the time of interest and at the beginning. The retention times of the AOYOP TFT memory device can be extrapolated more than 10 years operation time for a minimal charge loss of 15% at room temperature. Such good retention behavior can be attributed to the tight embrace of the Y_2O_3 trapping layer with

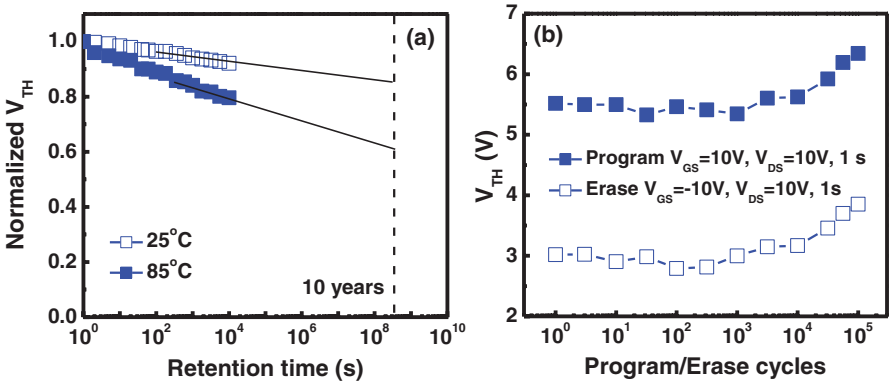

Figure 4. (a) Retention and (b) endurance characteristics of AOYOP TFT memory devices.

sufficiently deep trap energy level.[6] However, at elevated temperature of 85°C, the retention capability of AOYOP TFT memory device degraded significantly and a charge loss of ∼35% was observed after 10^8 s. We believed that the AOYOP device with a thick tunnel oxide can be used to improve the charge-keeping capability. Fig. 4b demonstrates the endurance characteristics of the AOYOP TFT memory device. The device was programmed at $V_{GS} = 10$ V and $V_{DS} = 10$ V and erased at $V_{GS} = -10$ V and $V_{DS} = 10$ V with the same programming and erasing time of 1 s. No significant memory window narrowing is observed in the AOYOP TFT memory device. Though, the V_{TH} increases for both memory states after 10^3 P/E cycles. We consider three aspects to explain this behavior. First, the gradual increase of V_{TH} may be due to the induced electron trapping to the vicinity of trapping layer during P/E cycling test. Second, the stress induced electron traps generated in the tunnel oxide. The other reason is the presence of uncompensated charge due to mismatch between localized spatial distributions of the injected charges. But, we believe that the third reason is most dominant since it can successfully explain the erase characteristics in Fig. 2a. The Y_2O_3 film as the charge trapping layer exhibits the potential to be incorporated into the future LTPS-TFT nonvolatile memory fabrication.

Conclusion

In conclusion, we have fabricated the AOYOP TFT nonvolatile memory device using an Y_2O_3 charge trapping layer. The XPS analysis indicates the formation of a thicker yttrium silicate layer. The AOYOP TFT memory device exhibited better electrical characteristics in terms of large memory window (2.5 V), long charge retention time (∼15% charge loss at ten years), and good endurance (up to 10^5 P/E cycles) with no memory window narrowing. The Y_2O_3 thin film is a promising charge trapping layer material for the fabrication of LTPS-TFT memory devices.

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