Electrical Characterization and Materials Stability Analysis of La_2O_3/HfO_2 Composite Oxides on n-$In_{0.53}Ga_{0.47}As$ MOS Capacitors With Different Annealing Temperatures

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***Abstract*— In this letter, a high-k composite oxide composed of La_2O_3 and HfO_2 is investigated for n-$In_{0.53}Ga_{0.47}As$ metal–oxide–semiconductor (MOS) capacitor application. The composite oxide was formed by depositing five layers of La_2O_3 (0.8 nm)/HfO_2(0.8 nm) on InGaAs with post deposition annealing at 500 °C. The MOS capacitors fabricated show good inversion behavior, high capacitance, low leakage current, with excellent interface trap density (D_{it}) of 7.0 × 10^{11} $cm^{-2}eV^{-1}$, small hysteresis of 200 mV and low capacitance equivalent thickness of 2.2 nm at 1 kHz were also achieved.**

***Index Terms*— HfO_2, InGaAs, La_2O_3, metal–oxide–semiconductor (MOS), molecular beam deposition (MBD), post deposition annealing (PDA).**

I. Introduction

RECENTLY III–V metal–oxide–semiconductor field-effect transistors (MOSFETs) have been widely investigated for post CMOS application because of the high electron mobility nature of III–V materials. Unlike SiO_2 on Si substrate, the lack of high-quality thermodynamically stable gate dielectric insulators on III–V compound semiconductors is still the main obstacle to realize the III–V MOSFET technology with commercial value. Al_2O_3 and HfO_2 are the most effective high-κ oxides that were used as gate insulators for III–V metal–oxide–semiconductor (MOS) devices [1]–[3]. However, the integration of novel high-k oxides on III–V compound semiconductors as gate insulators still needs a lot of effort. Rare earth oxide (REO) thin films are currently being investigated as high-k gate dielectric for future ultrascaled devices, due to their high dielectric constant and high conduction-band offset with respect to silicon [4]–[7]. Among the binary REOs, La_2O_3 is considered as one of the most potential gate dielectric materials due to its promising properties, such as high-κ value of (20–27), high bandgap of 4.6 eV, and high conduction-band offset of 23 eV.

When La_2O_3 is, however, in direct contact with InGaAs material, strong interdiffusion between InGaAs and La_2O_3 occurs after post deposition annealing (PDA) process [8]. A diffusion barrier layer is needed to avoid the interaction between La_2O_3 and $In_XGa_{1-X}As$ for MOS devices. HfO_2 has a high-k value of 27 and a high energy bandgap of 5.5 eV and is known to demonstrate inversion behavior with $In_XGa_{1-X}As$ [9]–[11], the material can also be used as a diffusion barrier. In this letter, a high-k composite oxide of La_2O_3 and HfO_2 grown on 100-nm n-$In_{0.53}Ga_{0.47}As$ with doping concentration of 5 × 10^{17} cm^{-3} on n+-InP is investigated for MOS capacitor application. An *in situ* molecular beam deposition (MBD) system was used to deposit the multilayers La_2O_3/HfO_2 stack on n-$In_{0.53}Ga_{0.47}As$. The interfacial properties of La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ with different PDA temperatures are studied in this letter.

II. Experiment

The MOS capacitor process includes surface treatment, oxide deposition, gate metal evaporation, and Ohmic formation. The wafers were first cleaned in 4% HCl solution for 3 min, followed by the $(NH_4)_2S$ solution dip for 30 min at room temperature. Then, the wafers were loaded into the MBD system for the oxide deposition, the composite HfO_2 (0.8 nm)/La_2O_3(0.8 nm) layer was deposited for 5 cycles at 300 °C. After deposition, the films were annealed at 400 °C, 500 °C, and 550 °C in nitrogen gas for 5 min to optimize the PDA temperature. Then, Ni/Au was deposited by electron beam evaporator as gate contact metal. Finally, Au/Ge/Ni/Au was deposited by electron beam evaporator on backside of n+ InP substrate and annealed at 250 °C for 30 s for Ohmic contact formation. An 8-nm HfO_2/ n-$In_{0.53}Ga_{0.47}As$ MOS capacitor with PDA at 500 °C for 5 min was also fabricated for device performance comparison in this letter.

III. Results and Discussion

After film deposition and PDA process, the La_2O_3(0.8 nm)/HfO_2(0.8 nm)composite dielectric was analyzed by X-ray

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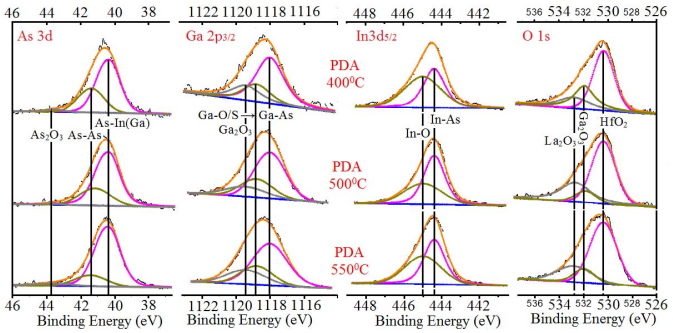

Fig. 1. As 3d, Ga2$p_{3/2}$, In 3$d_{5/2}$, and O 1s XPS spectra of the La_2O_3 (0.8 nm)/HfO_2(0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ composite structure with PDA temperature of 400 °C, 500 °C, and 550 °C in nitrogen gas for 5 min.

photoelectron spectroscopy (XPS) to determine the film composition and interfacial properties. The As 3d, Ga 2$p_{3/2}$, In 3$d_{5/2}$, and O 1s XPS spectra of the samples with different PDA temperatures were investigated. For the La_2O_3 (0.8 nm)/HfO_2(0.8 nm) films on n-$In_{0.53}Ga_{0.47}As$, the number of As-As bond was reduced when the annealing temperature was increased, also the amounts of As, Ga, and In related oxides were decreased. However, the amount of La_2O_3 was increased when the PDA temperature was increased to 500 °C. The XPS analysis results are shown in Fig. 1. The slight reduction of the native oxides in Fig. 1 could be explained by the conversion of As-O, Ga-O, and In-O bonding to InAs, GaAs, and La_2O_3 during thermal process. When the PDA temperature was increased up to 550 °C, the As, Ga, and In related oxides increased significantly as shown in Fig. 1 by As 3d, Ga 2$p_{3/2}$, and In 3$d_{5/2}$ spectra as compared with PDA at 500 °C. This indicates that at PDA temperature of 550 °C, the As, Ga, and In atoms diffused into the oxide layers significantly.

Fig. 2 shows the C–V curves for the five layers of La_2O_3(0.8 nm)/HfO_2(0.8 nm) composite oxides structure on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA temperature at 400 °C, 500 °C, and 550 °C. Abnormal accumulation capacitance increase in lower frequency region was observed for the composite oxide device with PDA at 400 °C as shown in Fig. 2(b), which is probably due to higher leakage current and D_{it}. When the PDA temperature was, however, increased to 500 °C, the electrical characteristics for the composite dielectric capacitor were greatly improved, and were much better than the electrical characteristics of the HfO_2/n-$In_{0.53}Ga_{0.47}As$ capacitors. The capacitance equivalent thickness (CET) at 1 kHz was reduced to 2.2 nm and the frequency dispersion improved to 3.5% as shown in Fig. 2(a) (for 8-nm HfO_2 on n-$In_{0.53}Ga_{0.47}As$ capacitor with PDA at 500 °C, CET = 2.7 nm, and frequency dispersion = 5.1%).

Fig. 3 shows the cross section of transmission electron microscopy (TEM) images and energy dispersive X-ray spectroscope for the five layers of La_2O_3(0.8 nm)/HfO_2(0.8 nm) composite oxides structure and the 8-nm HfO_2 on n-$In_{0.53}Ga_{0.47}As$ devices. No clear interdiffusion was observed for the as deposited oxide layers on n-$In_{0.53}Ga_{0.47}As$ as shown in Fig. 3(a). An interfacial layer of $\sim$ 1.6 nm was, however, formed due to In, Ga, and As diffusion into oxides after the sample was annealed at 500 °C as shown in Fig. 3(b). Fig. 3(c) shows the TEM image for 8-nm HfO_2 device. The oxide crystallized after the device was annealed at

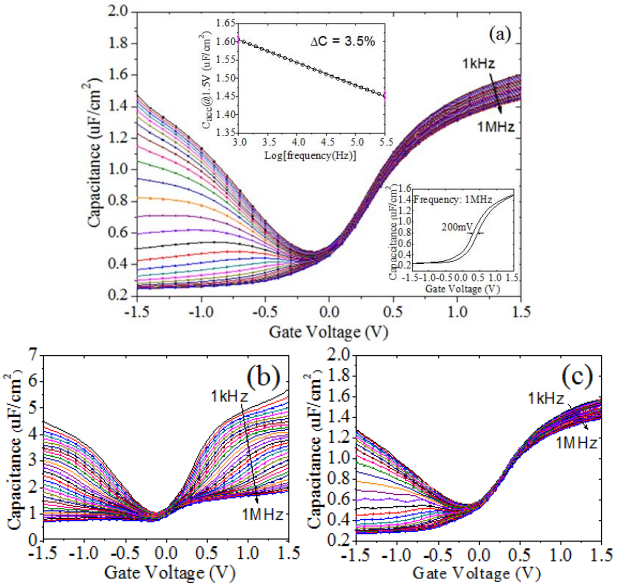

Fig. 2. C–V characteristics for the five layers of La_2O_3 (0.8 nm)/HfO_2(0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at (a) 500 °C, (b) 400 °C, and (c) 550 °C in nitrogen gas for 5 min.

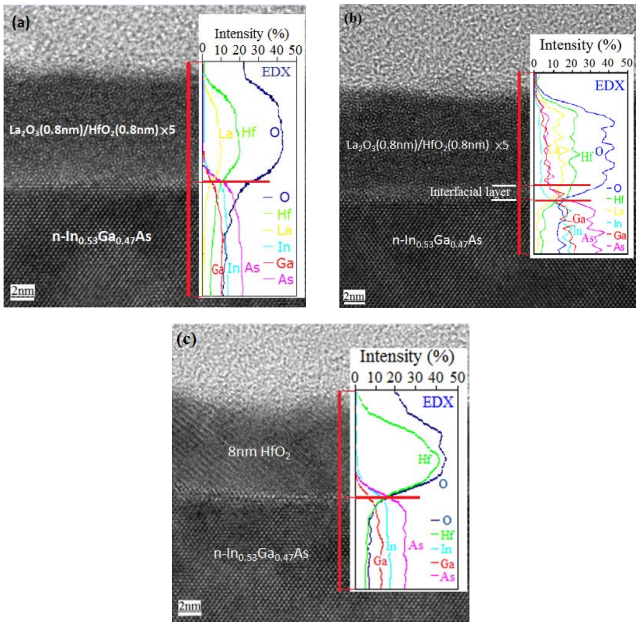

Fig. 3. Cross-sectional TEM image of the five layers of La_2O_3(0.8 nm)/HfO_2(0.8 nm) composite oxides structure for (a) as-deposited and (b) PDA at 500 °C, and (c) 8-nm HfO_2 with PDA at 500 °C on n-$In_{0.53}Ga_{0.47}As$ devices.

500 °C. Therefore, the alternate thin layers of 0.8-nm HfO_2 and 0.8-nm La_2O_3 design will make the oxide remain amorphous after annealing and increase the device capacitance as compared with the single HfO_2 oxides that are crystallized.

Fig. 4(a) and (b) are Gp/wqA versus frequency plot and D_{it} versus energy plot for the five layers of La_2O_3(0.8 nm)/HfO_2(0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at 500 °C. The C–V behaviors show improved interface traps densities (D_{it}) value, as estimated by conductance method, when PDA temperature was increased from 400 °C (D_{it} >10^{13} cm^{-2}•eV^{-1}) to 500 °C (D_{it} = 7.0 × 10^{11} cm^{-2}•eV^{-1}). But, the D_{it} degraded when PDA temperature was 550 °C (D_{it} = 9 × 10^{11} cm^{-2}•eV^{-1}). Lower

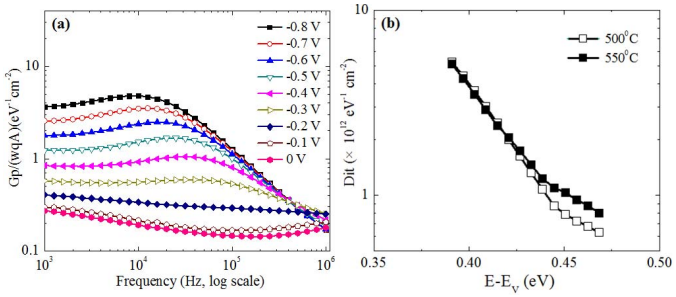

Fig. 4. (a) Gp/wqA (A:1.33 × 10^{-4} cm^2) versus frequency curves at different gate biases after 500 °C PDA and (b) D_{it} versus energy curves after 500 °C and 550 °C PDA for the five layers of La_2O_3(0.8 nm)/HfO_2(0.8 nm)on n-$In_{0.53}Ga_{0.47}As$ MOS devices.

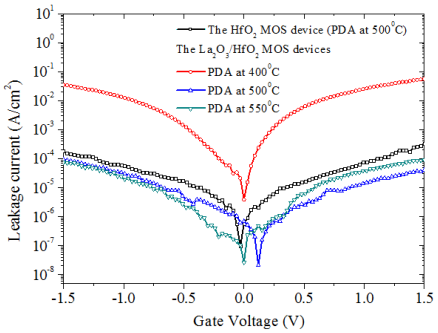

Fig. 5. Comparison of the leakage currents of the 8-nm HfO_2on n-$In_{0.53}Ga_{0.47}As$, and the five layers of La_2O_3(0.8 nm)/HfO_2(0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at 400 °C, 500 °C, and 550 °C.

D_{it} was however, achieved for the composite oxides MOS capacitor with over 500 °C PDA temperature. The 500 °C annealed sample shows good C–V responses with small hysteresis of 200 mV, and clear accumulation/depletion/inversion regions. This is in consistence with the decrease of As-, In-, and Ga-oxides at La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ interface as indicated in the XPS spectra. At the PDA temperature of 550 °C, As-oxides, Ga-oxides, and In-oxides bonding increased due to significant number of As, Ga, and In atoms diffused into oxide layers, resulting in C–V behavior degradation as indicated by the increase of frequency dispersion and depleted capacitance [3]. The five layers of La_2O_3 (0.8 nm)/HfO_2(0.8 nm) on n-$In_{0.53}Ga_{0.47}$ As with PDA at 500 °C MOS capacitor has lower D_{it} than the 8-nm HfO_2 on n-$In_{0.53}Ga_{0.47}$ As capacitor with PDA at 500 °C (D_{it} = 2.4 × 10^{12}cm^{-2}· eV^{-1}), previous papers for HfO_2 on n-$In_{0.53}Ga_{0.47}As$ MOS capacitor (D_{it} = 2.0 × 10^{12} cm^{-2}· eV^{-1}) [12], and HfO_2/Al_2O_3 on n-$In_{0.53}Ga_{0.47}$ As MOS capacitor (D_{it} = 2.0 × 10^{12} cm^{-2}· eV^{-1}) [13], and closed to the Al_2O_3 on n-$In_{0.53}Ga_{0.47}$ As MOS capacitor (D_{it} = 5.0 × 10^{11} cm^{-2}· eV^{-1}) [14].

Fig 5 shows the comparison of the leakage current for an 8-nm HfO_2on n-$In_{0.53}Ga_{0.47}As$ and the leakage currents of the five layers of La_2O_3 (0.8 nm)/HfO_2(0.8 nm) composite oxides structure on n-$In_{0.53}Ga_{0.47}As$ devices with PDA at 400 °C, 500 °C, and 550 °C. It indicates that lower leakage current was achieved for the composite oxide MOS device with the PDA temperature over 500 °C, much less than the 8-nm HfO_2MOS device. A higher annealing temperature will, however, result in the out diffusion of In, Ga, and As atoms to oxide layer from the $In_XGa_{1-X}As$ layer, and resulting in the increase of the leakage current.

IV. Conclusion

A high-k composite dielectric composed of La_2O_3 and HfO_2 layers on n-$In_{0.53}Ga_{0.47}As$ for MOS capacitor application is investigated. The composite oxide composed of the five layers of La_2O_3(0.8 nm)/HfO_2(0.8 nm) structure was annealed at different temperatures from 400 °C to 550 °C for performance comparison. When the annealing temperature was 500 °C, the n-$In_{0.53}Ga_{0.47}As$ MOS device showed best results with good inversion behavior, high capacitance and low leakage current. Excellent interface traps densities (D_{it}) of 7.0 × 10^{11} cm^{-2}eV^{-1}, small hysteresis of 200 mV and lower CET of 2.2 nm at 1 kHz were also achieved.

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