High-Performance Programmable Metallization Cell Memory With the Pyramid-Structured Electrode

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Abstract—The pyramid structure fabricated with the potassium hydroxide (KOH) anisotropically etched (100) silicon substrate has been deposited with a copper film as the bottom electrode of the programmable metallization cell (PMC) memory to significantly improve the resistive switching characteristic. As compared with the conventional flat copper electrode, this pyramid-structured electrode exhibited the set/reset voltage as low as 1/0.6 V and superior endurance of 2400 cycles at the set/reset voltages of $-5/+3$ V for the voltages pulsewidth of 1 μs. The high performance of this PMC could be attributed to high local electrical fields at the tips of the pyramid structure, resulting in the formation of the narrower conductive filaments that facilitate the lower operation voltage and better endurance.

Index Terms—Potassium hydroxide (KOH) surface texturing, programmable metallization cell (PMC), pyramid structure, resistive random-access memory (RRAM or ReRAM).

I. INTRODUCTION

RESISTIVE random access memory (RRAM) has recently received significant attention for the next-generation non-volatile memory technology because of its fast write and read access, low energy operation, and low cost [1], [2]. The electrochemical metallization RRAMs fabricated with active electrode metals such as Ag or Cu are referred to as programmable metallization cell (PMC) or conductive bridging RAM (CBRAM) [2]–[4]. The resistive switching phenomena of the PMC are attributed to the cations oxidized from the active anode metal, the ionic transport of these cations, and the reduced cations on the cathode. The nanoscale metallic conductive filaments (CFs) are formatted (the set process) and ruptured (the reset process) via the reduction-oxidation process of the cations in the resistive switching layer. This leads to the low and the high resistive states [5]–[8]. According to previous research [2], [5], [6], [9], [14], growth of the CFs are affected by the local electrical fields. Thus the adjustment of local electrical fields via the electrode structure should improve the resistive switching characteristics of the PMC memory. Therefore, the pyramid structured silicon surface produced by potassium hydroxide (KOH) anisotropic etching techniques

has been used to form electrodes with tips that could induce high electrical fields, and which have the advantages of a simple and low-cost production process [10]–[13].

Therefore, the pyramid structured electrode PMC is proposed in this letter and exhibited good repetitive operations reliability and low power consumption. The electric field distribution of the proposed sample was simulated by integrated systems engineering (ISE) technology computer-aided design (TCAD) simulation to clarify the possible reason of the improved resistive switching characteristics.

II. DEVICE FABRICATION

The p-type (100) oriented crystalline silicon wafers were dipped into hydrofluoric acid to remove the native oxide and rinsed in deionized water. Then the cleaned wafers were etched in a 1 wt% potassium hydroxide (KOH) solution at 80 °C for 30 min to produce saw damage on the surface and subsequently form the pyramid structure in a mixture of 1 wt% KOH with 30 vol% isopropyl alcohol buffer solution at 80 °C for 10 min [13]. Next, a 100-nm-thick Cu layer was deposited on the pyramid-structured silicon substrates as the bottom active electrodes, using a dc sputtering system. Then, a 200-nm-thick TiO_2 layer was reactively sputtered with the Ti target at the power of 190 W, total pressure of 5×10^{-3} torr, and flow rates of 22.4 and 9.6 sccm for the Ar and O_2 gases, respectively, on the bottom electrode as the resistive switching layer. Finally the 50-nm-thick Pt layer was deposited through a shadow mask as the top inert electrode, followed by the 1-μm-thick Al layer as the disk-shaped contact metal pad with the diameter of 356.9 μm For comparison conventional samples with flat electrodes on the unetched silicon substrate were also fabricated.

Electrical field distribution of the PMC memory sample with the proposed pyramid-structured electrode was also simulated by the ISE TCAD 10.0 simulator. The resistive switching characteristics were measured at room temperature in the dark with an Agilent 4156 C precision semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

Fig. 1(a) shows the 45° tilted view field-emission scanning electron microscopy (FE-SEM) image of the pyramid-structured Cu bottom electrode surface. As can be seen, many pyramids are randomly distributed, with possessed the base size ranging from 1 to 2 μm. Therefore, it was conjectured
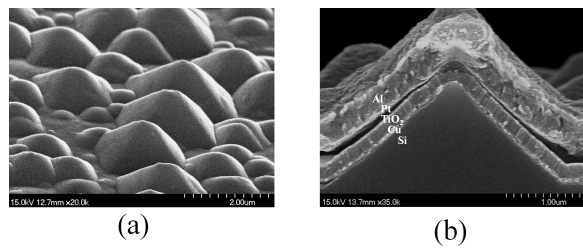
Fig. 1. (a) 45° tilted-view and cross-sectional FE-SEM image of the pyramid-structured Cu bottom electrode surface. (b) Cross-sectional FE-SEM image of the Al/Pt/TiO$_2$/Cu/Si stacked pyramid structure cell.

Fig. 3. (a) Iread-Vset curves with varied pulsewidths of the proposed pyramid-structured electrode sample. (b) The Iread-Vset curves with the varied pulsewidths of the conventional flat electrode sample.
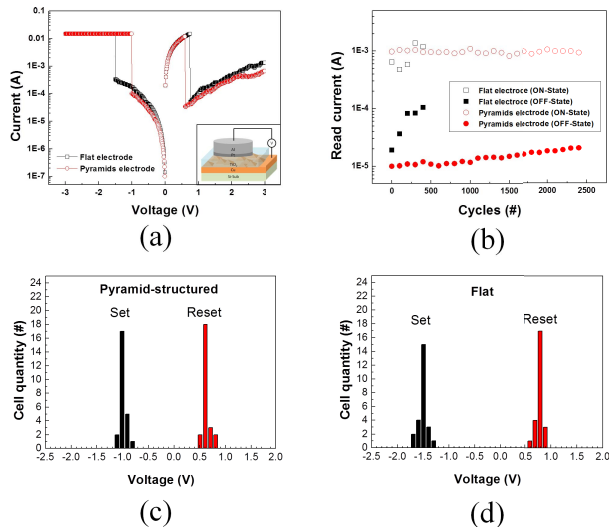

Fig. 2. (a) DC sweep I-V curves and structure diagrams of the proposed pyramid-structured electrode sample and the conventional flat electrode sample. (b) Endurances of the proposed pyramid-structured electrode sample and the conventional flat electrode sample. (c) The uniformity of the set/reset voltages for statisticed by the DC sweep measurements of 25 cells for the proposed pyramid-structured sample. (d) The uniformity of the set/reset voltages for statisticed by the DC sweep measurements of 25 cells for the conventional flat electrode sample.

Fig. 4. Electrical field contours for the proposed pyramid-structured electrode sample with simulation by ISE TCAD 10.0.

that the suitable cell sizes of the pyramid-structured electrode samples were speculated at least as large as 5 μm × 5 μm for accommodated at least one tip for formatted the CFs. Fig. 1(b) shows the cross-sectional FE-SEM image of the cell with the Al/Pt/TiO$_2$/Cu/Si stacked pyramid structure.

Fig. 2(a) shows the dc sweep I–V curves of the proposed pyramid-structured samples and the conventional flat samples, beginning in the reverse bias of 0 to −3 V and following the forward bias of 0 to +3 V. The current compliance (I_{Comp}) is set to 15 mA to protect the device from breakdown. The proposed pyramids-structured sample clearly can be switched to the low resistive state (ON-state) at −1 V during the reverse bias sweep and switched to high resistive state (OFF-state) at +0.6 V during the forward bias sweep. In contrast, the conventional flat sample was switched to the ON-state at −1.5 V and switched to the OFF-state at +0.8 V. A schematic diagram of the I–V measurement is also shown in the inset of Fig. 2(a). Fig. 2(b) shows the repeating resistive switching endurances of the proposed pyramid-structured and the conventional flat specimens. To fairly compare the reliability of these two samples, the same operation parameters with the set/reset pulse
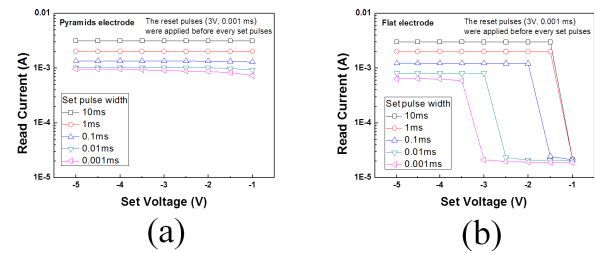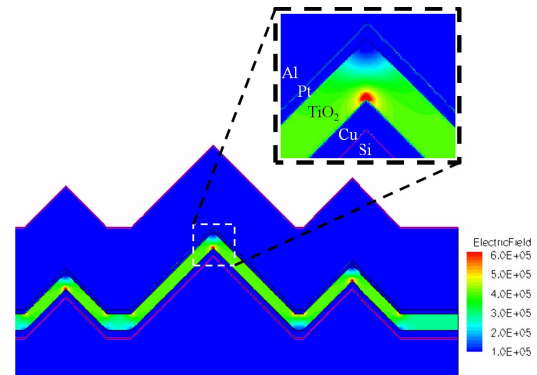
voltages of −5/+3 V, pulsewidth of 1 μs, the read voltage of 0.1 V, and the compliance current of 10 mA were carried out. Therefore the proposed pyramid-structured samples achieved 2400 resistive switching cycles, compared with 400 cycles for the conventional flat sample. In addition, the uniformity of the set/reset voltages for both the specimens were statisticed by the dc sweep measurements of 25 cells for both the pyramid-structured and conventional flat samples, as shown in Fig. 2(c) and (d), correspondingly.

The read current (I_{read}) was ∼1 × 10^{-5}. A measuring at 0.1 V for both pyramid structured and conventional flat specimens at the OFF-state. The pyramid-structured sample could be set from the OFF-state into the ON-state via the setting pulses (V_{set}) with the various pulsewidths and voltages, than followed by measuring the I_{read} at 0.1 V. Even for the V_{set} with a pulsewidth as short as 1 μs and voltage as low as −1 V, the magnitude of the I_{read} after the resetting pulse was attain to ∼1 × 10^{-3} A (define as ON-state) as shown in Fig. 3(a). As for the conventional flat one, the required V_{set} voltages to attain the ON-state were increased with the shortening of the pulsewidths, as shown in Fig. 3(b). It suggests that the proposed pyramid-structured electrode sample could setting faster with the lower required setting voltage than the conventional flat one. In addition, both the pyramid-structured and conventional flat specimens could be reset into the OFF-state from the ON-state via the identical resetting pulse with a pulsewidth of 1 μs and voltage of +3 V.

To better understand the superior resistive switching characteristic of the proposed pyramid-structured compared with conventional flat PMC devices, the electric field distribution of the pyramid-structured sample was simulated by an ISE TCAD

10.0 simulator, as shown in Fig. 4. The pyramid-structured bottom electrodes are significant higher than the those other area. Thus, it was expected that the required set/reset voltages for the pyramid-structured samples would be lower than the flat ones, consistent with the results in Fig. 2(a). According to the model of Mott and Gurney for the ionic transport in the resistive switching layer, the ionic current density (J) driven by the electric field can be described by the following [2], [14]:

$$ J = 2 \cdot Zq \cdot N_i \cdot a \cdot f \cdot \exp\left(\frac{-E_a}{kT}\right) \cdot \sinh\left(\frac{Zq \cdot E \cdot a}{2kT}\right) (1) $$

where q is the charge, Z is the number of the ions charged, N_i is the concentration of mobile cations, a is the jump distance of the cations, f is the attempt-to-escape frequency, E_a is the activation energy, E is the electric field, and kT is the thermal energy. From the formula (1), the enhanced local electrical field on the tips of the pyramid Cu electrode would not only enhance the cation current density through the resistive switching layer during the set and reset process, but also lead to the faster growth of the CFs near the tips with the substantially increased ionic current density caused by the enhanced electrical fields with respect to those at other areas. Furthermore, the fast growth of the CFs would result in a higher read current under a low set voltage with the shorter pulsewidth, as shown by the results in Fig. 3(a) and (b).

According to previous researches, the diameters of the CFs grow and become coarser with applied voltage and time during the setting process for a PMC memory [5], [9], [14]. On the other hand, the grown CFs would be broken by thinning and rupturing during the reset process. In addition, the residual Cu atoms from the ruptured CFs are reported to exist in the resistive switching layer at the OFF-state after numerous resistive switching cycles [15], [16] It is therefore conjectured that the higher local electrical fields of the proposed pyramid-structured sample were induced to form narrower CFs than the conventional flat one during the set process. Thus the narrower CFs of the pyramid-structured sample would be more easily ruptured and lead to less residual Cu atoms in the resistive switching layer. In addition, the narrower CFs would result in lower operation voltage and lower OFF-state leakage current, as well as better endurance than the conventional flat electrodes.

IV. CONCLUSION

The KOH anisotropically etched Si surface has been used to form textured pyramids that were subsequent deposited with a Cu film as the bottom electrode for the PMC memory. This pyramid-structured Cu electrode for PMC memory achieved the lower set/reset voltages of $-1/0.6$ V and the better endurance of 2400 cycles, compared with the conventional flat electrode, which had $-1.5/0.8$ V and 400 cycles, respectively. This was attributed to high local electrical fields near the tips of pyramids-structured electrode to form narrow CFs during the setting process and less residual Cu atoms during the reset process. This structured active metal electrode with enhanced local electrical fields has potential applications for PMC memory.

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