Flexible Three-Bit-Per-Cell Resistive Switching Memory Using a-IGZO TFTs

Shih-Chieh Wu, Hsien-Tsung Feng, Ming-Jiue Yu, I-Ting Wang, and Tuo-Hung Hou, *Member, IEEE*

***Abstract*— This letter proposes a novel high bit density nonvolatile memory using a logic compatible flexible amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistor (TFT) structure fabricated at low temperature. Before electrical forming, the a-IGZO TFT exhibits excellent transistor performance, including an ON/OFF current ratio of 8.8×10^6, a steep subthreshold slope of 0.14 V/decade, a threshold voltage of 0.55 V, and a maximum field-effect mobility of 2 cm^2/Vs. After electrical forming, a three-bit-per-cell resistive switching memory is realized using localized multilevel resistance states at the drain and source bits. Combining dual functionalities to achieve low-cost integration and excellent device characteristics at bending states, the proposed device is promising for future system-on-plastic applications.**

***Index Terms*— Amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs), flexible electronics, random access memory (RRAM), resistive switching, three-bit-per-cell.**

I. Introduction

THE high-mobility amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistor (TFT) [1] has emerged as a new generation active-matrix backplane technology in high-performance liquid crystal displays and organic light-emitting diode displays. It also enables the recently developed flexible display technology because of its low process temperature [2]. In addition, numerous logic circuits including logic gates, ring oscillators, shift registers, and static random access memory [3]–[5] have also been successfully demonstrated. Therefore, the high-mobility a-IGZO TFT technology offers promising potential for monolithic system-on-plastic (SoP) integration in low-cost flexible electronics. Nonvolatile memory (NVM) is another essential building block for a successful SoP integration. Several NVMs have been proposed with various degrees of compatibility with the a-IGZO TFT technology. For example, a-IGZO memories were fabricated using additional floating-gate or charge-trapping layers [6], [7]. The a-IGZO resistive-switching random access memory (RRAM) can be implemented in backend metallization processes [8], [9]. None of the mentioned devices can be, however, integrated into the standard process flow of a-IGZO TFTs without adding process steps and masks, which pose significant challenges for device yields and the cost of SoP integration.

Manuscript received July 16, 2013; accepted August 7, 2013. Date of publication September 11, 2013; date of current version September 23, 2013. This work was supported in part by the National Science Council of Taiwan under Grant NSC 100-2628-E-009-025-MY2 and Grant 101-2221-E-009-089-MY3, and by the NCTU-UCB I-RiCE program under Grant NSC-102-2911-I-009-302. The review of this letter was arranged by Editor W. S. Wong.

The authors are with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: thhou@mail.nctu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2013.2278098

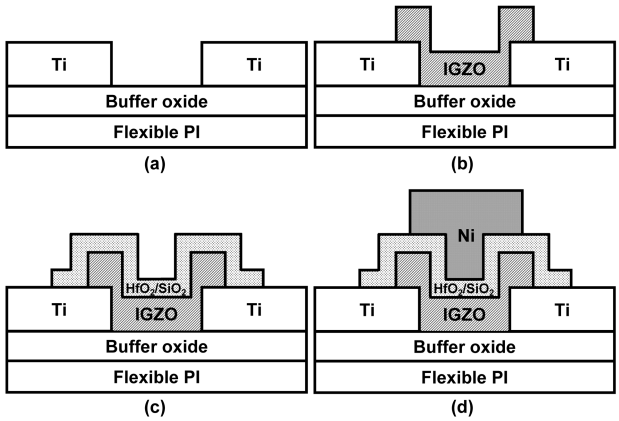

Fig. 1. Cross-sectional diagrams of the staggered a-IGZO TFT using a four-mask process flow.

Localized and independent resistive switching (RS) at drain and source bits in poly-Si TFTs [10] and a-IGZO TFTs [11] have been demonstrated using appropriate high-k gate dielectrics and metal gates. Its multibit-per-cell feature enables extremely high bit-density and low-cost embedded NVM using a completely logic compatible process flow. In addition to the localized RS, multiple resistance states in RRAM [12] might be used to further increase bit density. The same analogy combining two distinct regions of charge storage and multiple charge levels in a single cell has been used in high-density Flash memory [13]. In this letter, a three-bit-per-cell NVM technology was realized using localized multiple resistance states in a-IGZO TFTs. Excellent transistor and NVM characteristics can be achieved using an identical staggered a-IGZO TFT structure. The proposed device fabricated at low temperature on a flexible substrate exhibited negligible degradation at bending states, thereby promising for low-cost SoP integration in the future.

II. Experimental Procedure

Fig. 1 shows a staggered a-IGZO TFT fabricated using a four-mask process flow on a flexible polyimide (PI) substrate. Before the device fabrication, a 75-μm-thick Kapton PI film was cut to a size of 7 cm $\times$ 7 cm and cleaned using acetone to remove particles, followed by baking at 100 °C for 30 min.

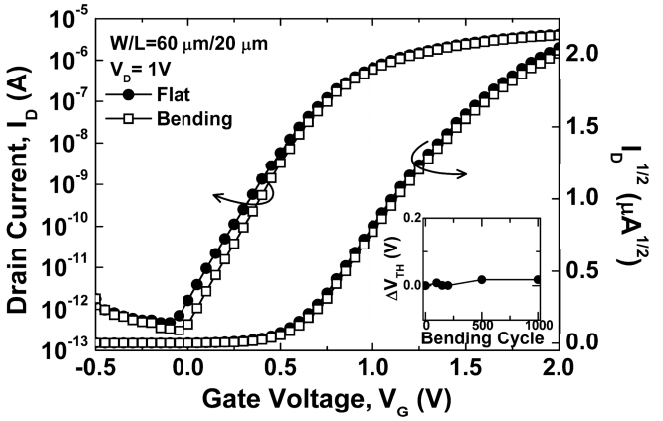

Fig. 2. I_D–V_G characteristics of the staggered a-IGZO TFT at flat and bending states. Inset: negligible V_{TH} shift of the flexible a-IGZO TFT subject to repeated compressive bending cycles with a bending radius of 10 mm.

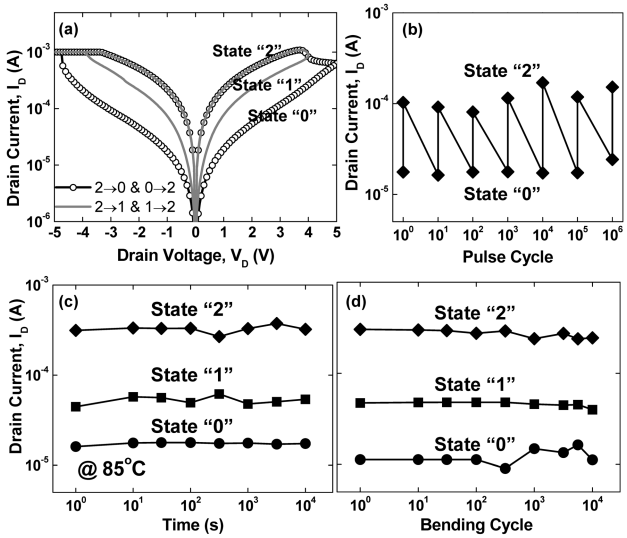

Fig. 3. (a) Three distinct resistance states (States 2, 1, 0) in the a-IGZO TFT RS memory. Voltage was applied to the drain while the gate was grounded. (b) Robust endurance of the staggered a-IGZO TFT RS memory exceeding 10^6 pulse cycles. Set and reset pulses were -5 V for 10 μs and 5 V for 500 μs, respectively. (c) Retention characteristics at 85 °C. (d) Bending endurance over concessive 10^4 cycles with a bending radius of 10 mm.

The cleaned PI substrate was then attached on a silicon carrier wafer. A 300-nm SiO_2 layer was deposited using plasma-enhanced chemical vapor deposition at 80 °C as a buffer layer.

Subsequently, a 50-nm Ti layer was deposited using electron beam evaporation and patterned as source/drain electrodes using a liftoff process [Fig. 1(a)]. A 40-nm a-IGZO film was deposited using dc sputtering at room temperature and an IGZO target (In:Ga:Zn:O = 2:2:1:7), followed by patterning and wet etching the active regions [Fig. 1(b)]. A bilayer gate dielectric, while also serving as an RS layer, comprised an interfacial SiO_2 layer of 2 nm and a HfO_2 layer of 10 nm with a total effective oxide thickness of 4.5 nm. The 2-nm SiO_2 layer was deposited using electron beam evaporation without heating the substrate. The deposition rate was ~0.01 nm/s. The 10-nm HfO_2 layer was reactively sputtered using an Hf metal target and Ar/O_2 = 5/1 at 200 W. After source/drain contacts were opened using dry etching [Fig. 1(c)], an 80-nm Ni layer was defined using a liftoff process to serve as the top electrode of both the TFT and the RS memory [Fig. 1(d)]. The gate overlap length over the source/drain was 4 μm. Finally, the PI substrate was detached from the Si carrier wafer.

III. Results and Discussion

Fig. 2 shows the transfer characteristic (I_D–V_G) curve of the fabricated staggered a-IGZO TFT at both flat and bending states with $V_D = 1$ V. A compressive strain along the channel length direction was imposed at the bending state with a bending radius of 10 mm. The device had an ON/OFF current ratio of 8.8×10^6, a steep subthreshold slope of 0.14 V/decade, a threshold voltage (V_{TH}) of 0.55 V, and a maximum field-effect mobility of 2 cm^2/Vs. V_{TH} shifted positively from 0.55 to 0.57 V under compressive strain, which can be explained by the change of channel conductivity. The decreased distance between atoms under compressive stain increased the IGZO bandgap and reduced film conductivity, thereby increasing V_{TH} [14]. In addition, verifying the device stability when subject to repeated bending cycles is critical for flexible electronics applications. The inset in Fig. 2 shows a negligible V_{TH} shift of the flexible a-IGZO TFT during consecutive 1000 compressive bending cycles using a mechanical bending vehicle.

Through applying a forming voltage of -6.5 V to the drain while the gate was grounded, the RS memory bit located at the gate/drain overlapped region can be activated in the otherwise high-performance TFT, which is capable of logic applications. Fig. 3(a) shows the typical bipolar RS characteristics with three distinct resistance states using dc I_D–V_D sweeps with a negative set voltage (V_{SET}) and a positive reset voltage (V_{RESET}). The gradual reset characteristics allowed precise control of multiple resistance states using appropriate V_{RESET}. The low resistance state, the intermediate resistance state, and the high resistance state were denoted as State 2, State 1, and State 0, respectively. The device was at State 2 after set. Reset from State 2 to State 1 was realized using a V_{RESET} of 4 V, while reset from State 2 to State 0 or from State 1 to State 0 was realized using a V_{RESET} of 5 V. Note that V_{SET} was also increased proportionally to V_{RESET}.

A separate a-IGZO TFT device using Ti metal gates instead of Ni did not show a stable RS. Furthermore, the gradual reset was not observed in a similar $Ni/HfO_2/SiO_2/Pt$ structure when replacing a-IGZO with Pt [11]. Although the exact mechanism of multilevel RS is still under investigation, a plausible model was proposed based on modulating the Ni-filament/a-IGZO Schottky barrier at the gate/drain overlapped region [11]. The Ni filament was formed only after electrical forming, which also ensured no interference between logic and memory functionalities. The gradual reset using larger reset voltage is the signature of increasing tunnel distance, most often involving oxygen ion migration [15]. The bipolar set/reset and multiple resistance states in the proposed device might be explained by the modulation of the oxygen vacancy concentration at the Ni-filament/a-IGZO interface and the Schottky barrier thickness. Fig. 3(b) shows robust endurance of the staggered a-IGZO TFT RS memory exceeding 10^6 pulse cycles. Only two levels (States 2 and 0) are shown because the precise control of multiple resistance states using short pulses

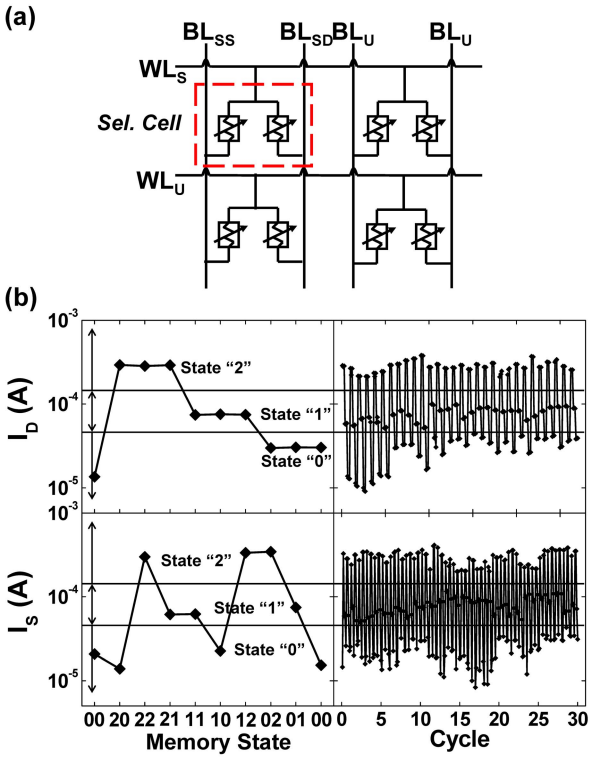

Fig. 4. (a) Schematic diagram of a-IGZO TFT RS memory array. One-transistor unit cell contains two 3-state bits. Two bit lines BL_{SD} and BL_{SS} are used to read out I_D at the drain bit and I_S at the source bit simultaneously. (b) Simultaneous I_D and I_S readout of an operating sequence through all nine available states, 00 (D:HRS; S:HRS) →20 (D:LRS; S:HRS) → 22 (D:LRS; S:LRS) → 21 (D:LRS; S:IRS) →11 (D:IRS; S:IRS) →10 (D:IRS; S:HRS) → 12 (D:IRS; S:LRS) → 02 (D:HRS; S:LRS) → 01 (D:HRS; S:IRS) → 00 (D:HRS; S:HRS) for one cycle (left) and for 30 cycles (right).

was more difficult to achieve in the present standalone device without current-limiting transistors. Fig. 3(c) shows the stable retention characteristics of three resistance states at 85 °C. Finally, Fig. 3(d) shows superior bending endurance exceeding 10^4 consecutive cycles.

Similar RS characteristics were also achieved at the source bit. RS can be precisely controlled at the drain/source bits without interference by suppressing the coupling through the a-IGZO channel. The independent RS was guaranteed when the channel current was less than that required for set and reset by choosing appropriate device dimensions. Combining two three-state bits at the drain and source, total nine states (3^2) could be defined using simultaneous readouts of I_D and I_S in an one-transistor unit cell, as shown in Fig. 4(a) [10]. For instance, the memory state 00 and 20 denoted when the drain/source bits were at State 0/State 0 and State 2/State 0, respectively. Using two bit lines and appropriate peripheral program/read circuits, the one-transistor unit cell is capable of storing three-bit data which requires 2^3 states. Fig. 4(b) shows simultaneous I_D and I_S readouts using a switching sequence through all nine available states in a device with a channel width and length of 20 and 10 μm, respectively. The state of the drain bit remained unaltered when the source bit was programmed, and vice versa, showing negligible interference between two physical bits. The results demonstrated the first three-bit-per-cell RRAM using localized multilevel RS. Enlarging the maximum resistance ratio in the future might add more distinct levels to each localized bit and further increase bit density.

IV. Conclusion

This letter demonstrated a novel flexible NVM technology using logic compatible a-IGZO TFTs fabricated at low temperature. Independent multilevel RS at the drain and source bits enabled reliable three-bit-per-cell operations. In addition to the excellent flexible memory characteristics and high bit density, the a-IGZO TFTs without undergoing electrical forming showed promising transistor performance and bending stability. This letter suggests that both logic circuits and NVM can be seamlessly integrated on the flexible substrate using an identical a-IGZO TFT technology, which creates new opportunities for future SoP applications.

References

[1] K. Nomura, H. Ohta, A. Takagi, *et al.*, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.

[2] J. S. Park, T. W. Kim, D. Stryakhilev, *et al.*, "Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 95, no. 1, pp. 013503-1–013503-3, 2009.

[3] H. Luo, P. Wellenius, L. Lunardi, *et al.*, "Transparent IGZO-based logic gates," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 673–675, May 2012.

[4] M. Mativenga, M. H. Choi, J. W. Choi, *et al.*, "Transparent flexible circuits based on amorphous-indium-gallium-zinc-oxide thin-film transistors," *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 170–172, Feb. 2011.

[5] N. Münzenrieder, C. Zysset, T. Kinkeldei, *et al.*, "A flexible InGaZnO based 1-bit SRAM under mechanical strain," in *Proc. Semicond. Conf. Dresden*, 2011, pp. 1–4.

[6] H. Yin, S. Kim, H. Lim, *et al.*, "Program/erase characteristics of amorphous gallium indium zinc oxide nonvolatile memory," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2071–2077, Aug. 2008.

[7] J. Jang, J. C. Park, D. Kong, *et al.*, "Endurance characteristics of amorphous-InGaZnO transparent flash memory with gold nanocrystal storage layer," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3940–3947, Nov. 2011.

[8] M. C. Chen, T. C. Chang, C. T. Tsai, *et al.*, "Influence of electrode material on the resistive memory switching property of indium gallium zinc oxide thin films," *Appl. Phys. Lett.*, vol. 96, no. 26, pp. 262110-1–262110-3, 2010.

[9] Q. Wang, H. Y. Xu, X. H. Li, *et al.*, "Flexible resistive switching memory device based on amorphous InGaZnO film with excellent mechanical endurance," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1442–1444, Oct. 2011.

[10] S. C. Wu, C. Lo, and T. H. Hou, "Novel two-bit-per-cell resistive-switching memory for low-cost embedded applications," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1662–1664, Dec. 2011.

[11] S. C. Wu, H. T. Feng, M. J. Yu, *et al.*, "Multi-bit-per-cell a-IGZO TFT resistive-switching memory for system-on-plastic applications," in *IEDM Tech. Dig.*, 2012, pp. 100–103.

[12] C. Yoshida, K. Tsunoda, H. Noshiro, *et al.*, "High speed resistive switching in $Pt/TiO_2/TiN$ film for nonvolatile memory application," *Appl. Phys. Lett.*, vol. 91, no. 22, pp. 223510-1–223510-3, 2007.

[13] B. Eitan, G. Cohen, A. Shappir, *et al.*, "4-bit per cell NROM reliability," in *IEDM Tech. Dig.*, 2005, pp. 539–542.

[14] N. Münzenrieder, K. H. Cherenack, and G. Tröster, "The effects of mechanical bending and illumination on the performance of flexible IGZO TFTs," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 2041–2048, Jul. 2011.

[15] S. Yu, X. Guan, and H.-S. P. Wong, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization," in *IEDM Tech. Dig.*, 2011, pp. 413–416.