High-Current-Drive Dual-Gate a-IGZO TFT With Nanometer Dotlike Doping

Chun-Hung Liao, Chang-Hung Li, Hsiao-Wen Zan, Hsin-Fei Meng, and Chuang-Chuang Tsai

***Abstract*— In this letter, we use a dual-gate (DG) structure together with nanometer dotlike doping (NDD) in active channel to produce a-IGZO thin-film transistors with very high current drive. With DG operation, the output current increases from 0.14 mA of the conventional device to 0.76 mA of the NDD device. The enhanced lateral field and improved carrier accumulation in DG operation may explain the significantly enlarged drive current. Particularly, simulated electron distribution reveals that high carrier concentration is induced under NDD regions in DG operation. The device without NDD, however, does not exhibit improved drive current in DG operation.**

***Index Terms*— a-IGZO thin-film transistor (TFT), dot doping, double gate, dual gate (DG), oxide thin-film transistor.**

I. Introduction

INCREASING current drive of a-IGZO thin-film transistors (TFTs) is important when developing a-IGZO TFT as high-quality array transistor in display applications or as high-speed transistors in flexible electronics [1]–[4]. With ultimate channel geometry design (i.e., maximum allowed width over length) and operation voltage, improving output current relies on increasing carrier concentration and mobility while keeping high ON/OFF current ratio. According to [5]–[7], dual-gate (DG) operation increases drive current by increasing the lateral electric field and total channel carrier amount. The current enhancement ratio (CER), which is the ratio between the drive current of DG operation and sum of currents of the top gate (TG) and bottom gate (BG) operations, is as high as 140% at 10 V overdrive [5]. On the other hand, the carrier transport in a-IGZO follows percolation transport [8]. Potential barriers generated because of the random distribution of Ga^{3+} and Zn^{2+} ions in the network structure strongly limit the carrier transport. From the analytical expression of the percolation model, carrier mobility is expressed as $\mu = \mu_0 \exp(-e\varphi_{\rm eff}/kT)$, where $\varphi_{\rm eff}$ is the effective potential barrier height. Lateral electric field is expected to reduce $\varphi_{\rm eff}$ according to the field-induced barrier lower effect [9]. In [4], we proposed a new doping structure, named as nanometer dotlike doping (NDD), to greatly increase the effective mobility of a-IGZO TFT from 4 to 79 $\rm cm^2V^{-1}s^{-1}$. The dotlike doping reduces the effective channel length. In addition, the potential barrier in intrinsic a-IGZO is lowered by the neighboring high-conductive regions and hence the mobility is greatly enlarged. Here, to further enhance the output current drive, we introduce DG structure in NDD IGZO TFT.

In this letter, DG NDD a-IGZO TFTs with different doping dot densities are produced. The DG operation is used to enhance lateral field and increase channel carrier amount [5]–[7]. The enhanced lateral field is expected to further lower down $\phi_{\rm eff}$ and increase mobility. We successfully obtain CERs as 180–210% at 10 V overdrive ($V_{\rm ov}$) for DG-NDD a-IGZO TFTs with different dot densities. For DG a-IGZO TFTs without NDD design, the CER is only close to 1 in our letter. In addition, output current and transconductance of DG-NDD a-IGZO TFT (with high dot density) are five times higher than those of conventional DG a-IGZO TFT, indicating that combining DG and NDD is an effective approach to elevate device current. In addition, for the first time, simulated electron distribution reveals that DG-NDD structure (under NDD regions) exhibits 5–10 times enlarged electron concentration than conventional DG a-IGZO TFTs.

II. Experiment

The fabrication steps and the 45° view of schematic structure of DG-NDD a-IGZO TFT are shown in Fig. 1(a) and (b), respectively. The p-type heavily doped Si wafer was prepared as the BG and the 100-nm-thick SiN_x was used as the bottom gate insulator (BI). We used radio-frequency sputtering to deposit a 50-nm-thick IGZO on SiN_x at room temperature. After annealed at 400 °C for 1 h in N_2 environment a 2000-Å cross-linkable poly(4-vinyl phenol) (PVP) was spin-coated and cross-linked at 200 °C for 60 min in air to serve as the top gate insulator (TI). The surface of PVP was made hydrophilic by exposure to UV-ozone for 1 min before submerging the substrate into positively charged polystyrene (PS) spheres (Merck, K6–020) diluted in an ethanol solution. The PS spheres with diameters as 200 nm were adsorbed on PVP surface to serve as the shadow mask. A 1000-Å Al was then evaporated as a top metal gate electrode. Followed by removing the PS spheres using an adhesive tape (Scotch, 3M), the PVP at sites without Al coverage was removed by 50-W O_2 plasma treatment for 13 min. After that, 50-W Ar plasma was applied onto the bare IGZO channel region for 1 min for increasing the conductivity. Under gate region, IGZO exhibits

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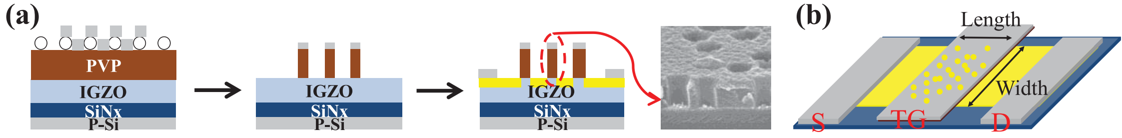

Fig. 1. (a) Fabrication process of the DG-NDD a-IGZO TFT and the SEM image in porous structure. (b) 45° view of the device structure. Channel width and length are defined by the patterned of the IGZO and the TG metal.

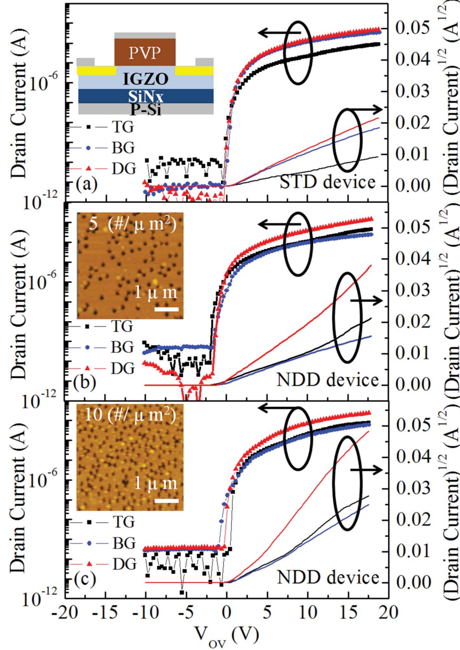

Fig. 2. Transfer characteristics of (a) STD, (b) NDD (low dot density), and (c) NDD (high dot density) a-IGZO TFTs operated in TG, BG, and DG modes. V_{DS} = 20 V. Inset in (a) is the schematic structure of STD device. AFM images of NDD TG with low and high dot densities are in insets in (b) and (c), respectively.

high-density high-conductivity dots (names as the NDD). Aside of the gate region, high-conductivity IGZO areas [marked by yellow rectangles in Fig. 1(b)] serve as the self-aligned source (S) and drain (D) regions to define the channel length as 300 μm. The width of the IGZO active region defines the channel width as 1000 μm. Finally, aluminum pads were evaporated through a shadow mask to form the source and drain contact pads. The length between two pads is 500 μm. The scanning electron microscope (SEM) image of the DG-NDD a-IGZO TFT is in Fig. 1(a). The schematic structure of dual-gate standard (DG-STD) a-IGZO TFT is shown in the inset of Fig. 2(a) for comparison. For the NDD devices, different dot density can be obtained by controlling the PS sphere dilution concentration For concentrations as 0.8 wt% and 1.5 wt%, the dots densities calculated from atomic force microscopy (AFM) images in the inset of Fig. 2(b) and (c) are 5 and 10 μm^2, respectively.

III. Results and Discussion

The transfer characteristics of STD a-IGZO TFT, NDD a-IGZO TFT with low dot density, and NDD a-IGZO TFT with high dot density are shown in Fig. 2(a), (b), and (c), respectively. TG and BG represent that the gate bias is applied

TABLE I

Typical Parameters of STD and NDD Devices Under TG, BG, and DG Modes. C_{total} Is the Sum of Capacitances in Top and in Bottom Dielectrics

	mode	V_T(V)	S.S (V/dec.)	I (μA)		$I_D L/WC_{total}$
STD	TG	-1.9	0.16	22	DG mode	0.4 REF. [5]
	BG	-2.1	0.21	118		
	DG	-0.8	0.13	143		0.2 REF. [7]
NDD with dots density low / high	TG	-0.7 / 0.6	0.15 / 0.12	112 / 220		
	BG	-5 / 4.1	0.40 / 0.28	98 / 183		**2.9** **NDD-DG high dots density**
	DG	-0.6 / 1	0.18 / 0.17	392 / 762		

only on TG and BG electrodes, respectively. DG represents that the gate bias is applied onto top and BGs simultaneously. For STD device in Fig. 2(a), DG operation is almost the same as BG operation. TG operation gives small current because of the small capacitance in TI. Specifically, the capacitances of TI and BI are 16.1 and 53.1 nF/cm^2, respectively. For NDD devices in Fig. 2(b) and (c), TG and BG operations deliver similar output current. The drain current (at V_{OV} = 1 V and V_{DS} = 2 V), the threshold voltage (V_T), and subthreshold swing of TG, BG, and DG a-IGZO TFTs with STD and NDD (with low and high dots densities) structures are listed in Table I. The effective mobility of the STD device in TG and BG modes are 9.2 and 13 cm^{2}V^{-1}s^{-1}. Saturation μ_{eff} is extracted according to [5] by setting V_{DS} = 20 V and V_{OV} < 8 V. For NDD devices, intrinsic mobility is not extracted because of the lack of model to describe the complicated channel doping profile and variation of carrier concentration in bulk region (will be shown in Fig. 4). The transconductance at V_{DS} = 20 V and V_{OV} = 8 V for DG-NDD device (0.13 mS), however, is five times larger than that for DG device without NDD (0.022 mS). In addition, compared with [5] and [7], DG-NDD device exhibits a significantly larger value in normalized output current ($I_D L/W$) divided by total capacitance (i.e., C_{total}, the sum of the capacitances of TI and BI), indicating a greatly improved driving ability.

The DG operation is further evaluated using CER. For STD device, CER is only ~1 (not shown) indicating that DG operation simply turns ON top channel (TC) and bottom channel (BC) simultaneously. This result is the same as [7]. For NDD devices, the output current at V_{DS} = 20 V, V_{OV} = 10 V and the corresponding CERs with standard deviation are shown in Fig. 3(a). Data are obtained from independent three and four NDD a-IGZO TFTs with low and high dot densities, respectively. The standard deviation may be further suppressed using ordered dots in future research when employing nanoimprint technology. For all the seven NDD devices, CERs > 1.78 are

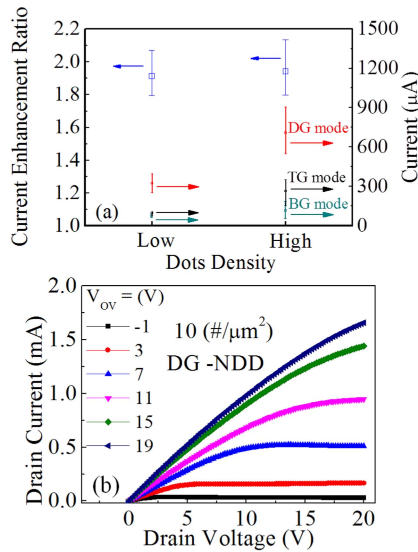

Fig. 3. (a) Stand deviation of output current in TG-NDD, BG-NDD and DG-NDD devices (at $V_{DS} = 20$ V, $V_{OV} = 10$ V), and corresponding enhancement ratios of NDD devices with low dot density (three samples) and high dot density (four samples). (b) Output characteristic of NDD device.

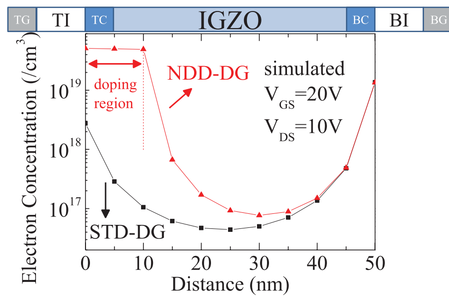

Fig. 4. Simulated electron concentration distribution along the direction from TC to BC with and without the NDD doping. Simulation parameters are in [10].

obtained. The output characteristics of DG-NDD devices with high dot density are shown in Fig. 3(b). At high V_{OV}, current behavior becomes more resistor like. This may be due to the parasitic resistance in source and drain regions. Specifically, Ar plasma treated regions marked by yellow rectangles in Fig. 1 cause large voltage drop under high current level. parasitic resistance can be reduced in future researches, higher current under large V_{OV} can be expected On the other hand, the large parasitic resistance will suppress the current when scaling down the channel length.

Chen *et al*. [5] that researched on conventional a-IGZO TFT and demonstrated an enhanced lateral electric field and improved carrier accumulation in middle channel in DG operation. In this letter, significantly improved CERs are only obtained in DG-NDD devices. Simulation results in Fig. 4 reveal that, compared with STD-DG device NDD-DG device exhibits 5–10 times enlarged carrier concentration under NDD regions (Ar plasma treated regions) in middle channel.[1] Introducing NDD into DG TFT is hence promising.

IV. Conclusion

In this letter, we demonstrated a boosted current drive in DG a-IGZO TFT with NDD designs. The conventional DG a-IGZO TFT delivers 0.14mA output current at 10 V overdrive. Combining NDD with DG structure leads to a five times enlarged output current (0.76 mA) at 10 V overdrive. The NDD structure leads to improved carrier concentration in middle channel. In addition, increased lateral electric field in DG operation may enhance the barrier lowering effect to improve mobility. The results are beneficial for developing a-IGZO TFTs with high current drive.

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[1] The electron mobility and concentration in IGZO are 15 $cm^2V^{-1}s^{-1}$ and 10^{17} cm^{-3}, respectively. Considering limited mesh design in the software, channel length is 1.1 m and NDD is a periodical doping on IGZO back interface. With 100 nm/200 nm as the doping/period length, NDD doping concentration is 5×10^{19} cm^{-3} with 10-nm abrupt doping depth.