Design of $2 \times V_{DD}$-Tolerant I/O Buffer With PVT Compensation Realized by Only $1 \times V_{DD}$ Thin-Oxide Devices

Ming-Dou Ker, *Fellow, IEEE*, and Po-Yen Chiu, *Student Member, IEEE*

***Abstract*—A new $2 \times V_{DD}$-tolerant input/output (I/O) buffer with process, voltage, and temperature (PVT) compensation is proposed and verified in a 90-nm CMOS process. Consisting of the dynamic source bias and gate controlled technique, the proposed mixed-voltage I/O buffer realized by only $1xV_{DD}$ devices can successfully transmit and receive $2 \times V_{DD}$ signal. Utilizing this technique with only $1xV_{DD}$ devices, the digital logic gates are also modified to have $2xV_{DD}$-tolerant capability. With $2xV_{DD}$-tolerant logic gates, the PVT variation detector has been implemented to detect PVT variations from $2 \times V_{DD}$ signal and provide compensation control to the $2 \times V_{DD}$-tolerant I/O buffer without suffering the gate-oxide overstress issue.**

***Index Terms*—Gate-oxide overstress, mixed-voltage I/O buffer, process, voltage, and temperature (PVT) variation.**

I. Introduction

In order to achieve lower power consumption, higher operating speed, and higher integration capability, CMOS devices have been continually scaled down with thinner gate oxide and smaller channel length [1]. As a result, the core circuit devices will be operated in a low voltage level (below 1.2 V) in the advanced CMOS technologies. However, some peripheral components or other integrated circuits (ICs) in a microelectronic system would be still operated in higher voltage levels (above 1.8 V). With the different power supply voltages in the microelectronic system, the conventional I/O buffer circuits are no longer suitable due to reliability concern. Several reliability issues had been reported, such as gate-oxide overstress [2]–[5], hot-carrier degradation [6], and the undesired leakage current paths [7], [8]. Therefore, the mixed-voltage I/O buffers are necessary in the interfaces of IC chips or subsystems having different power supply voltages. In the mixed-voltage I/O buffer, some devices could be directly replaced by the thick-oxide devices to solve the aforementioned reliability issues. However, using both the thick-oxide and thin-oxide devices within a chip increases the fabrication cost. To reduce the fabrication cost, several mixed-voltage I/O buffers realized by only low-voltage (thin-oxide) devices have been reported [9]–[16].

With the scaled-down CMOS devices, the circuit performance becomes more sensitive to process, voltage, and temperature (PVT) variations. In addition to the PVT variations, a recent study had been reported that the die-package stress also influences device or circuit performance [17]. So, it becomes harder to meet the required performance specifications in nanoscale processes. To improve the yield, the PVT variations have been taken into consideration in lots of circuit design scenarios, especially in signal processing, data transmitting, and clock generating [18]–[23]. Similarly, the mixed-voltage I/O buffers also suffer the PVT variation issues. For example, if the I/O buffers are fabricated in the slow-slow (SS) corner and operated at faulty environments of high temperature or low operating voltage, the I/O buffers will not meet the timing specifications such as rise time and fall time. Although this problem can be solved by increasing the I/O buffer's size, too large I/O buffers have another issue called simultaneous switching noise (SSN) [24], [25]. This arises when the I/O buffers with too large dimensions are fabricated in the fast-fast (FF) corner and operated at normal operating conditions. Thus, the I/O buffers should be designed with the compensation technique to maintain a constant slew rate under the PVT variations.

Several previous studies of I/O buffers with PVT compensation provided useful methods to keep the output slew rate within an acceptable range [26]–[31]. However, those methods are not feasible in the mixed-voltage I/O buffers, because the devices would suffer the gate-oxide overstress issue under a higher operating voltage of $2xV_{DD}$.

In this paper, a new $2xV_{DD}$-tolerant I/O buffer with PVT compensation is proposed and verified in a 90-nm CMOS process. The design concepts are described in Section II. The proposed $2xV_{DD}$-tolerant logic gates and circuit implementation of $2xV_{DD}$-tolerant I/O buffer with PVT compensation are presented in Sections III and IV, respectively. The experimental verifications in silicon chip are presented in Section V. Finally, the circuit limitations are discussed in Section VI.

II. Dynamic Source Bias and Gate-Controlled Techniques

Figs. 1 and 2 show the design concepts of the dynamic source bias and gate-controlled techniques to achieve a $2xV_{DD}$- tolerant I/O buffer with transmitting and receiving modes [14].

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The authors are with the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. M.-D. Ker is also with the Biomedical Electronics Translational Research Center, National Chiao-Tung University, Hsinchu, Taiwan (e-mail: mdker@ ieee.org).

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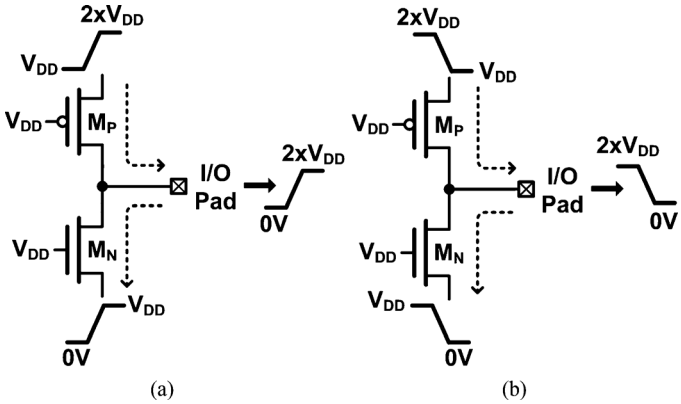


Fig. 1. Dynamic source bias technique in the transmitting mode when transmitting (a) the logic high and (b) the logic low, signals.

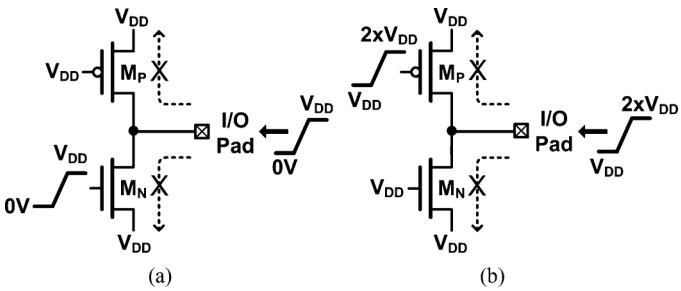


Fig. 2. Gate-controlled technique in the receiving mode when receiving (a) $0\ \mathrm{V}-\mathrm{to}-\mathrm{V_{DD}}$ and (b) $\mathrm{V_{DD}}-\mathrm{to}-2\mathrm{xV_{DD}}$, signals.

Comparing Figs. 1(a) and 1(b) in the transmitting mode, with the gate voltage of $\mathrm{V_{DD}}$ at $\mathrm{M_P}$ and $\mathrm{M_N}$, $\mathrm{M_P}$ and $\mathrm{M_N}$ can be turned on or turned off by changing their source voltages to transmit the $0\ \mathrm{V}-2\mathrm{xV_{DD}}$ or $2\mathrm{xV_{DD}}-0\ \mathrm{V}$ signals. For transmitting a $0\ \mathrm{V}-2\mathrm{xV_{DD}}$ signal as shown in Fig. 1(a), by applying $0\ \mathrm{V}-\mathrm{V_{DD}}$ signal at $\mathrm{M_N}$'s source and $\mathrm{V_{DD}}-2\mathrm{xV_{DD}}$ signal at $\mathrm{M_P}$'s source, the I/O pad can successfully transmit a digital signal from $0\ \mathrm{V}-2\mathrm{xV_{DD}}$. On the other hand, for transmitting a $2\mathrm{xV_{DD}}-0\ \mathrm{V}$ signal as shown in Fig. 1(b), $\mathrm{V_{DD}}-0\ \mathrm{V}$ and $2\mathrm{xV_{DD}}-\mathrm{V_{DD}}$ signals are needed for source terminals of $\mathrm{M_N}$ and $\mathrm{M_P}$, respectively.

For the receiving mode, in order to receive the $0\ \mathrm{V}-2\mathrm{xV_{DD}}$ voltage signal without gate-oxide overstress issue and turn off $\mathrm{M_P}$ and $\mathrm{M_N}$ to avoid unnecessary circuit leakage path, the source voltages of $\mathrm{M_P}$ and $\mathrm{M_N}$ should be biased at $\mathrm{V_{DD}}$. Besides, the gate biases of $\mathrm{M_P}$ and $\mathrm{M_N}$ should be controlled according to the received voltage signal. For example, when receiving the voltage signal from $0\ \mathrm{V}-\mathrm{V_{DD}}$ as shown in Fig. 2(a), the gate voltage of $\mathrm{M_P}$ should be $\mathrm{V_{DD}}$ and the gate voltage of $\mathrm{M_N}$ should be $0\ \mathrm{V}-\mathrm{V_{DD}}$. When receiving the voltage signal from $\mathrm{V_{DD}}-2\mathrm{xV_{DD}}$ as shown in Fig. 2(b), the gate voltage of $\mathrm{M_P}$ should be $\mathrm{V_{DD}}-2\mathrm{xV_{DD}}$ and the gate voltage of $\mathrm{M_N}$ should be $\mathrm{V_{DD}}$. Therefore, the channel of $\mathrm{M_P}$ and $\mathrm{M_N}$ can not be turned on to cause leakage current in the receiving mode. With the dynamic source bias and gate-controlled technique, the output buffer implemented by only $1\mathrm{xV_{DD}}$ devices can transmit or receive $0\ \mathrm{V}-2\mathrm{xV_{DD}}$ voltage signals without suffering the aforementioned reliability issues.

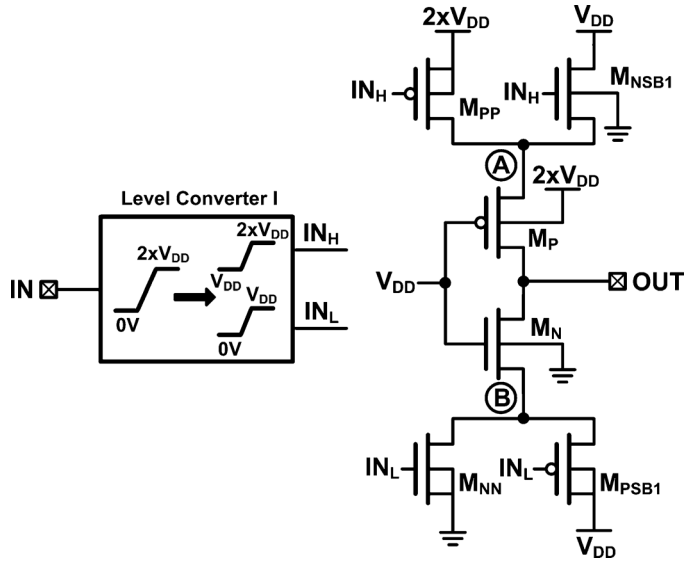


Fig. 3. $2\mathrm{xV_{DD}}$-tolerant NOT gate.

III. $2\mathrm{xV_{DD}}$-Tolerant Logic Gates

By utilizing the dynamic source bias technique, complementary logic gates can be modified to have $2\mathrm{xV_{DD}}$-tolerant capability. Fig. 3 shows the $2\mathrm{xV_{DD}}$-tolerant NOT gate. $\mathrm{M_P}$ and $\mathrm{M_N}$ with gate voltages of $\mathrm{V_{DD}}$ are used to conduct logic level to output and avoid gate-oxide overstress issue during operation. $\mathrm{M_{PP}}$ and $\mathrm{M_{NN}}$ are used to decide the function of logic gate. $\mathrm{M_{NSB1}}(\mathrm{M_{PSB1}})$ is used to bias the source voltage of $\mathrm{M_P}(\mathrm{M_N})$ at $\mathrm{V_{DD}}$ when $\mathrm{M_{PP}}(\mathrm{M_{NN}})$ is turned off during operation. Since the device operation voltage is not allowed to exceed $1\mathrm{xV_{DD}}$ range, the $0\ \mathrm{V}-2\mathrm{xV_{DD}}$ input signal needs to be separated to a $0\ \mathrm{V}-\mathrm{V_{DD}}$ and a $\mathrm{V_{DD}}-2\mathrm{xV_{DD}}$ control signal for pull-low path and pull-high path, respectively.

Fig. 4 illustrates the proposed level converter I, which converts the $0\ \mathrm{V}-2\mathrm{xV_{DD}}$ voltage signal to the require voltage signals. As shown in Fig. 4, when the input signal IN is from 0 V to $\mathrm{V_{DD}}-\mathrm{V_{th}}$, where $\mathrm{V_{th}}$ is MOSFET's threshold voltage, $\mathrm{M_{N1}}$ and $\mathrm{M_{P2}}$ are turned on. $\mathrm{IN_L}$ is conducting the voltage signal from 0 V to $\mathrm{V_{DD}}-\mathrm{V_{th}}$, and $\mathrm{IN_H}$ is biased at $\mathrm{V_{DD}}$. When IN signal is from $\mathrm{V_{DD}}+\mathrm{V_{th}}$ to $2\mathrm{xV_{DD}}$, $\mathrm{M_{N2}}$ and $\mathrm{M_{P1}}$ are turned on. $\mathrm{IN_H}$ is conducting the voltage from $\mathrm{V_{DD}}$ to $2\mathrm{xV_{DD}}$ and $\mathrm{IN_L}$ is biased at $\mathrm{V_{DD}}$. By the proposed level converter I, the $0\ \mathrm{V}-2\mathrm{xV_{DD}}$ voltage signal can successfully be separated to a $0\ \mathrm{V}-\mathrm{V_{DD}}$ voltage signal $\mathrm{IN_L}$ and a $\mathrm{V_{DD}}-2\mathrm{xV_{DD}}$ voltage signal $\mathrm{IN_H}$. Then, the $\mathrm{IN_L}$ signal is connected to the gates of $\mathrm{M_{NN}}$ and $\mathrm{M_{PSB1}}$ at pull-low path, while the $\mathrm{IN_H}$ signal is connected to the gates of $\mathrm{M_{PP}}$ and $\mathrm{M_{NSB1}}$ at pull-high path (as shown in Fig. 3).

With this configuration, the voltage across each MOSFET does not exceed $1\mathrm{xV_{DD}}$ voltage range. Moreover, the output voltage signal can be driven to the required $2\mathrm{xV_{DD}}$ magnitude. When input signal IN is 0 V, the $\mathrm{IN_L}$ signal is also 0 V to turn off the $\mathrm{M_{NN}}$ and turn on $\mathrm{M_{PSB1}}$. At the same time, the $\mathrm{IN_H}$ signal is driven to $\mathrm{V_{DD}}$ to turn on $\mathrm{M_{PP}}$ because the source voltage of $\mathrm{M_{PP}}$ is $2\mathrm{xV_{DD}}$. Therefore, the output voltage of the NOT gate is driven to $2\mathrm{xV_{DD}}$ and the voltage at node B is biased to $\mathrm{V_{DD}}$. On the other hand, when input signal IN is $2\mathrm{xV_{DD}}$, the $\mathrm{IN_L}$

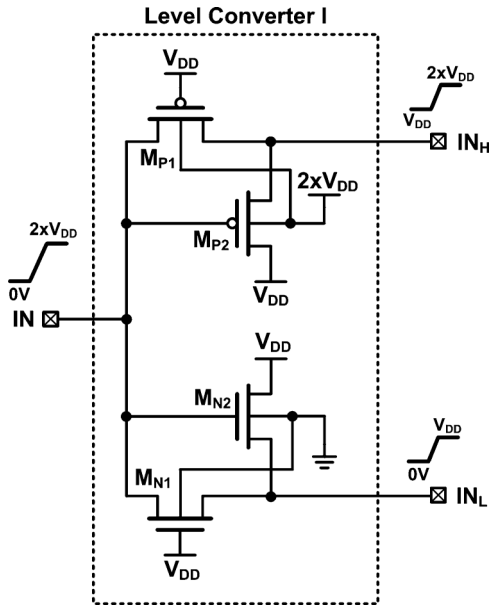


Fig. 4. Circuit implementation of level converter. I.

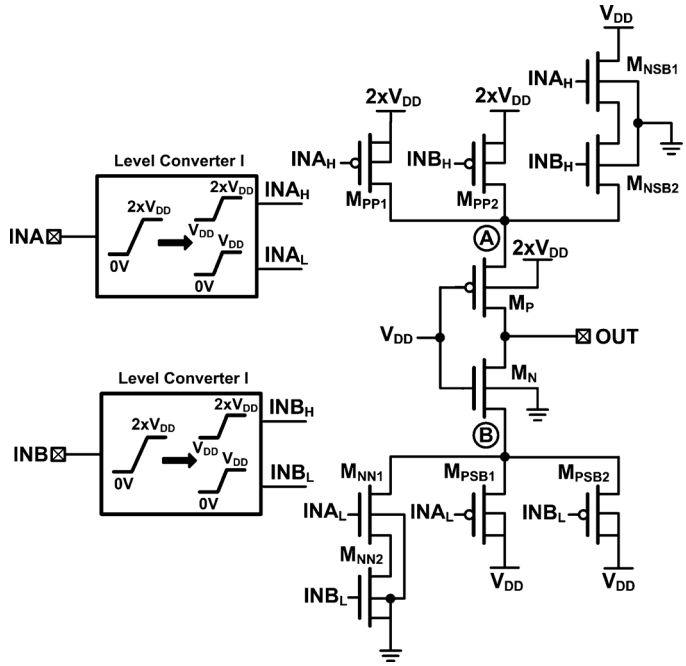


Fig. 5. $2xV_{DD}$-tolerant NAND gate.

signal is V_{DD} to turn on the M_{NN} and turn off M_{PSB1}. At the same time, the IN_H signal is driven to $2xV_{DD}$ to turn off M_{PP} and turn on M_{NSB1}. Therefore, the output voltage of the NOT gate is driven to 0 V and the voltage of node A is biased to V_{DD}. Whether the output voltage is pulled high to $2xV_{DD}$ or pulled low to 0 V, each two terminals of all MOSFETs do not exceed a $1xV_{DD}$. Thus, gate-oxide overstress issue can be completely avoided in the proposed $2xV_{DD}$-tolerant NOT gate.

The NAND and NOR logic gates can also be modified to have $2xV_{DD}$-tolerant capability. Figs. 5 and 6 show the $2xV_{DD}$-tolerant NAND and $2xV_{DD}$-tolerant NOR gate, respectively. M_P and M_N with gate voltage of V_{DD} are also used to conduct logic level to the output and avoid gate-oxide overstress issue. M_{PP1}, M_{PP2}, M_{NN1}, and M_{NN2} are used to define the function of logic gate. M_{PSB1}, M_{PSB2}, M_{NSB1}, and M_{NSB2} are used to bias the source voltage of M_P and M_N at V_{DD} when the pull-low or pull-high path is turned off during operation.

To achieve correct logic operating and source biasing, the function defining devices and source biasing devices need to have complementary structure when the logic gates have more than one input. For example, with the series connection of nMOS M_{NN1} and M_{NN2} in the $2xV_{DD}$-tolerant NAND gate's pull-low path, the source bias pMOS M_{PSB1} and M_{PSB2} should be parallel connected at the source terminal of M_N, as shown in Fig. 5. Even though the pull-low path is turned off when input INA and INB are opposite logic signal, node B still can be biased to the safe voltage of V_{DD} by M_{PSB1} or M_{PSB2}. Based on this design methodology, all complementary logic gates with different input numbers could be modified to have $2xV_{DD}$-tolerant capability.

Figs. 7(a)–7(c) show the simulated waveforms of $2xV_{DD}$-tolerant NOT, NAND, and NOR gates, respectively. Besides, the corresponding circuit logics and devices' behavior of each $2xV_{DD}$-tolerant gate are summarized in Tables I–III, respectively. Implementing in a 90-nm CMOS process, the normal operating voltage $(1xV_{DD})$ for core devices is 1.2 V, while the

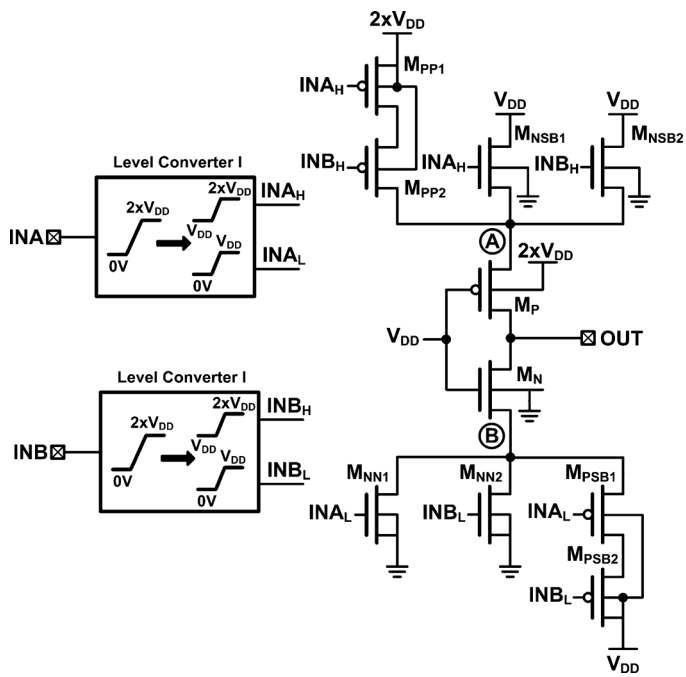


Fig. 6. $2xV_{DD}$-tolerant NOR gate.

I/O devices' operating voltage is 2.5 V, which is as $2xV_{DD}$. In the simulated results, each $2xV_{DD}$-tolerant logic gate performs correct logic operation and no gate-oxide overstress issue is encountered in all MOSFETs.

IV. $2xV_{DD}$-Tolerant I/O Buffer With PVT Compensation

The proposed $2xV_{DD}$-tolerant I/O buffer with PVT compensation is shown in Fig. 8. It incorporates three circuit blocks, which are the $2xV_{DD}$-tolerant I/O buffer [14], $2xV_{DD}$-tolerant PVT variation detector, and $2xV_{DD}$-tolerant 8-to-3 encoder.

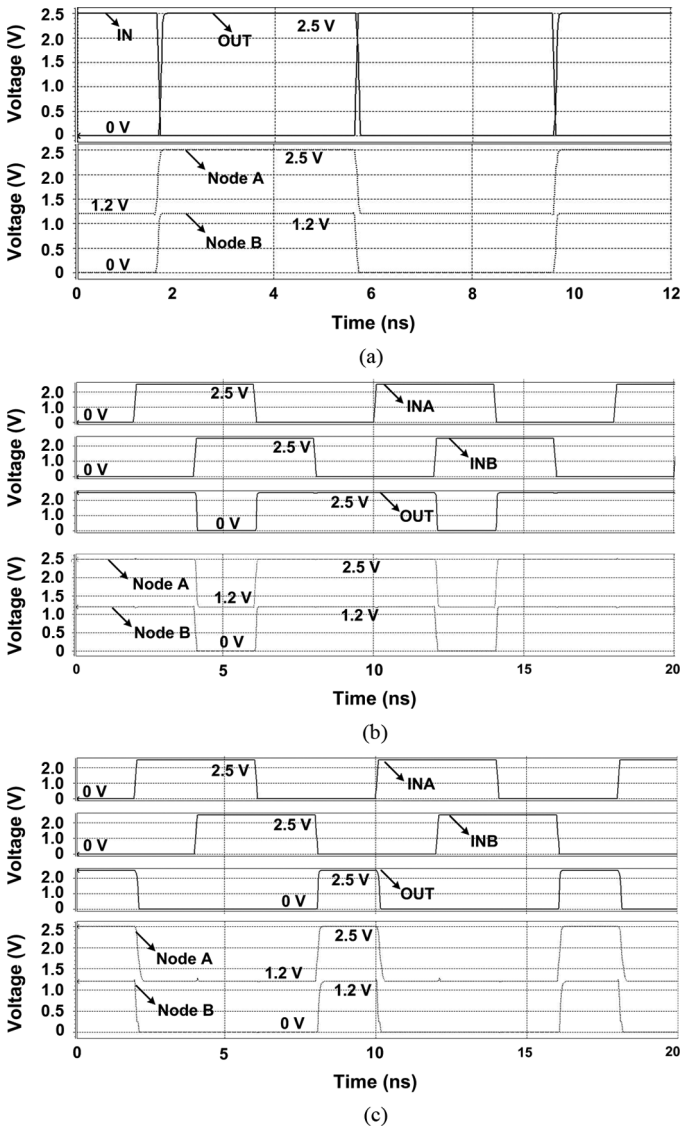


Fig. 7. Simulated voltage waveforms of (a) $2xV_{DD}$-tolerant NOT gate, (b) $2xV_{DD}$-tolerant NAND gate, and (c) $2xV_{DD}$-tolerant NOR gate.

The $2xV_{DD}$-tolerant PVT variation detector detects the influence of PVT variations on the $2xV_{DD}$ voltage signal at the chip and provides the compensation code in that specific environment. Then, the compensation code is inputted to the $2xV_{DD}$-tolerant 8-to-3 encoder to generate the 3-bit control signals for the I/O buffer. With the 3-bit control signals, the I/O buffer can adjust the driving capability to mitigate the impacts caused by PVT variations.

A. $2xV_{DD}$-Tolerant I/o Buffer

In the $2xV_{DD}$-tolerant I/O buffer, the functions include transmitting a $2xV_{DD}$ voltage signal with $1xV_{DD}$ voltage input signal and receiving a $2xV_{DD}$ voltage signal. With the same design concept of dynamic source bias technique, the $0\ V - 2xV_{DD}$ voltage signal is also separated to a $0\ V - V_{DD}$ and a $V_{DD} - 2xV_{DD}$ control signals. The $0\ V - V_{DD}$ voltage signal PD from the pre-driver input of Dout is utilized to control the pull-low path of driving nMOS M_{NN} and the source voltage bias pMOS M_{PSB}. Besides, this $0\ V - V_{DD}$ voltage signal at PU is converted to $V_{DD} - 2xV_{DD}$ voltage signal at PUH by the level converter II (as shown in Fig. 9) to control the pull-high path of driving pMOS M_{PP} and the source voltage bias nMOS M_{NSB}. Thus, the source voltages of M_P and M_N

TABLE I
CORRESPONDING CIRCUIT LOGICS AND DEVICES' BEHAVIOR IN PROPOSED $2xV_{DD}$-TOLERANT NOT GATE

Circuit Logic	Pull-High	Pull-Low
IN	0	$2xV_{DD}$
IN_L	0	V_{DD}
IN_H	V_{DD}	$2xV_{DD}$
Node A	$2xV_{DD}$	V_{DD}
Node B	V_{DD}	0
OUT	$2xV_{DD}$	0
M_{PP}	ON	OFF
M_{PSB1}	ON	OFF
M_P	ON	OFF
M_{NN}	OFF	ON
M_{NSB1}	OFF	ON
M_N	OFF	ON

TABLE II
CORRESPONDING CIRCUIT LOGICS AND DEVICES' BEHAVIOR IN PROPOSED $2xV_{DD}$-TOLERANT NAND GATE

Circuit Logic	Pull-High	Pull-High	Pull-High	Pull-Low
(INA, INB)	(0, 0)	(0, $2xV_{DD}$)	($2xV_{DD}$, 0)	($2xV_{DD}$, $2xV_{DD}$)
(INA_L, INB_L)	(0, 0)	(0, V_{DD})	(V_{DD}, 0)	(V_{DD}, V_{DD})
(INA_H, INB_H)	(V_{DD}, V_{DD})	(V_{DD}, $2xV_{DD}$)	($2xV_{DD}$, V_{DD})	($2xV_{DD}$, $2xV_{DD}$)
Node A	$2xV_{DD}$	$2xV_{DD}$	$2xV_{DD}$	V_{DD}
Node B	V_{DD}	V_{DD}	V_{DD}	0
OUT	$2xV_{DD}$	$2xV_{DD}$	$2xV_{DD}$	0
M_{PP1}	ON	ON	OFF	OFF
M_{PP2}	ON	OFF	ON	OFF
M_{PSB1}	ON	ON	OFF	OFF
M_{PSB2}	ON	OFF	ON	OFF
M_P	ON	ON	ON	OFF
M_{NN1}	OFF	OFF	OFF	ON
M_{NN2}	OFF	ON	OFF	ON
M_{NSB1}	OFF	OFF	ON	ON
M_{NSB2}	OFF	OFF	OFF	ON
M_N	OFF	OFF	OFF	ON

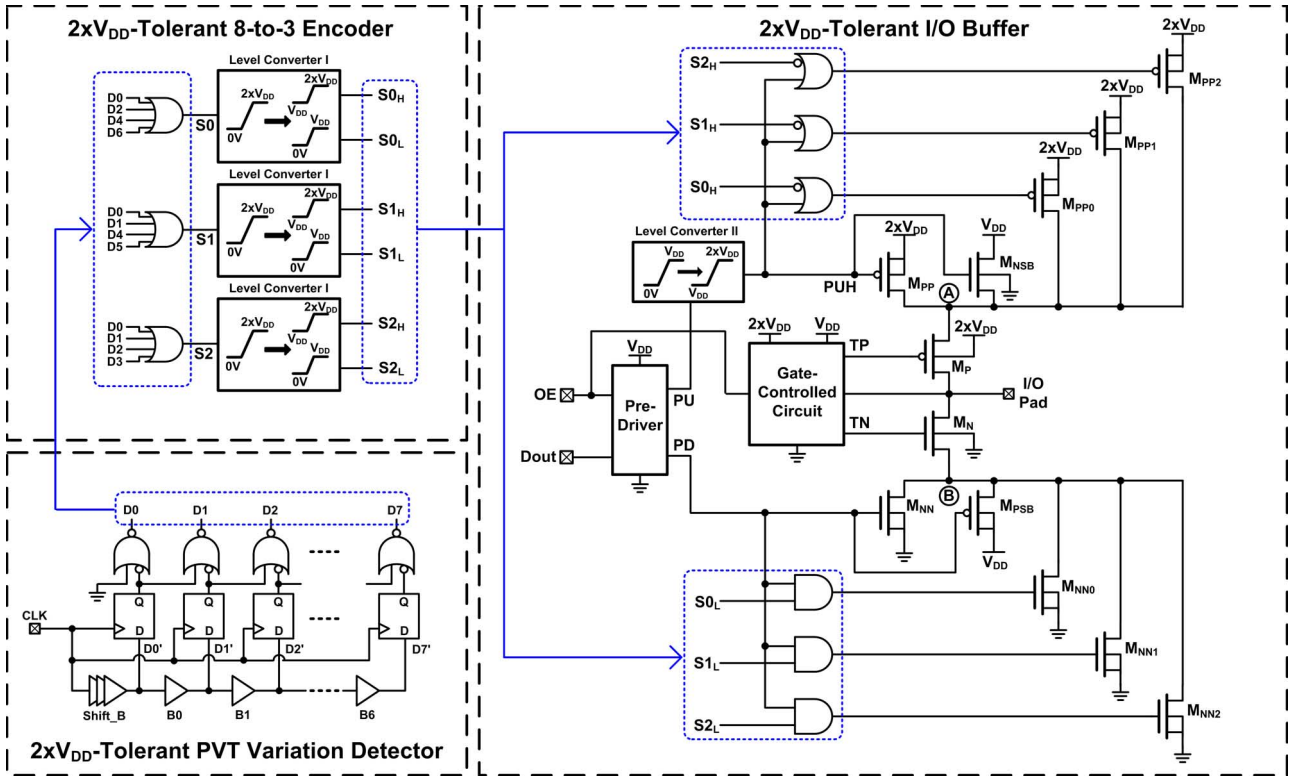


Fig. 8. Proposed $2xV_{DD}$-tolerant I/O buffer with PVT compensation.

TABLE III
CORRESPONDING CIRCUIT LOGICS AND DEVICES' BEHAVIOR IN PROPOSED $2xV_{DD}$-TOLERANT NOR GATE

Circuit Logic	Pull-High	Pull-Low	Pull-Low	Pull-Low
(INA, INB)	(0, 0)	(0, $2xV_{DD}$)	($2xV_{DD}$, 0)	($2xV_{DD}$, $2xV_{DD}$)
(INA_L, INB_L)	(0, 0)	(0, V_{DD})	(V_{DD}, 0)	(V_{DD}, V_{DD})
(INA_H, INB_H)	(V_{DD}, V_{DD})	(V_{DD}, $2xV_{DD}$)	($2xV_{DD}$, V_{DD})	($2xV_{DD}$, $2xV_{DD}$)
Node A	$2xV_{DD}$	V_{DD}	V_{DD}	V_{DD}
Node B	V_{DD}	0	0	0
OUT	$2xV_{DD}$	0	0	0
M_{PP1}	ON	ON	OFF	OFF
M_{PP2}	ON	OFF	OFF	OFF
M_{PSB1}	ON	OFF	OFF	OFF
M_{PSB2}	ON	OFF	ON	OFF
M_P	ON	OFF	OFF	OFF
M_{NN1}	OFF	OFF	ON	ON
M_{NN2}	OFF	ON	OFF	ON
M_{NSB1}	OFF	OFF	ON	ON
M_{NSB2}	OFF	ON	OFF	ON
M_N	OFF	ON	ON	ON

can be biased to the required values during the transmitting and receiving modes. For example, in the transmitting mode, the transmitting enable signal OE is V_{DD} and Dout is 0 V, the PD and PU signals are driven to V_{DD} to turn on M_{NN} and

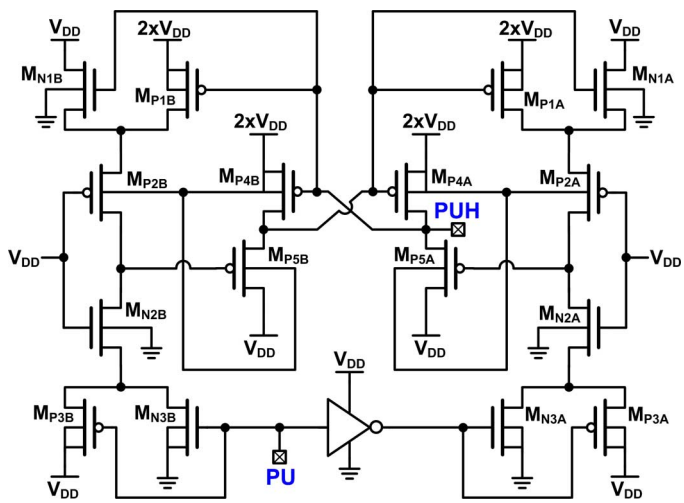


Fig. 9. Circuit implementation of level converter II.

turn off M_{PSB}. At the same time, the PUH signal is converted to $2xV_{DD}$ to turn off M_{PP} and turn on M_{NSB}. Therefore, the output voltage at I/O pad is 0 V and the voltage at node A is V_{DD}. On the other hand, with 0 V OE signal in receiving mode, the PD signal is 0 V, the PU signal is V_{DD}, and the PUH signal is $2xV_{DD}$. Therefore, the M_{PSB} and M_{NSB} are turned on to bias nodes A and B to V_{DD}.

To generate the required gate bias voltage of $M_P(M_N)$ at TP (TN), the gate-controlled circuit is proposed and illustrated in Fig. 10. In transmitting mode (OE signal is V_{DD}), it biases the voltages at TP and TN to V_{DD}. In receiving mode (OE signal is 0 V), TP and TN are adjusted to the required voltages. For

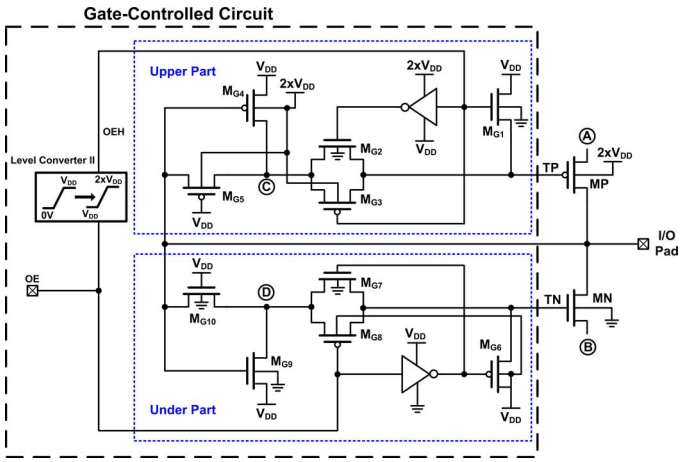


Fig. 10. Gate-controlled circuit for the proposed $2\mathrm{xV_{DD}}$-tolerant I/O buffer.

example, when the I/O pad is $2\mathrm{xV_{DD}}$, the upper part transistors of $\mathrm{M_{G5}}$, $\mathrm{M_{G2}}$, and $\mathrm{M_{G3}}$ are turned on to bias TP at $2\mathrm{xV_{DD}}$. On the other hand, the under part transistors of $\mathrm{M_{G9}}$, $\mathrm{M_{G7}}$, and $\mathrm{M_{G8}}$ are turned on to bias TN voltage at $\mathrm{V_{DD}}$. With the dynamic source bias and gate-controlled techniques, the $2\mathrm{xV_{DD}}$-tolerant I/O buffer actually can transmit and receive a $0\ \mathrm{V} - 2\mathrm{xV_{DD}}$ voltage signal without the gate-oxide overstress issue. To implement PVT compensation, the output driver is modified to multi-stages and the number of turned-on stages is decided by the compensation code. In this work, the output drivers contain three stages and the ratio of $\mathrm{M_{PP0}}(\mathrm{M_{NN0}})$, $\mathrm{M_{PP1}}(\mathrm{M_{NN1}})$, and $\mathrm{M_{PP2}}(\mathrm{M_{NN2}})$ is 1:2:4 to meet 3-bit compensation codes.

B. $2xV_{DD}$-Tolerant PVT Variation Detector

In the prior PVT compensation techniques [26]–[31], the most convenient method is to detect the delay time which is influenced by PVT variation. With the PVT detector, the circuit quantifies the delay time of the delay chain to generate a compensation code [29], [31]. Then, the multiple output stages are turned on according to the compensation signal to adjust the driving capability. With this kind of PVT detector, the output driver can control the slew-rate within one clock cycle time. Besides, each circuit block of PVT detector consists of complementary logic circuits. However, applying the prior PVT detector in the mixed-voltage I/O buffer to detect the variation at the $2\mathrm{xV_{DD}}$ voltage signal suffers the gate-oxide overstress issue. In this work, the PVT detector is modified to tolerant $2\mathrm{xV_{DD}}$ voltage signal by using the proposed $2\mathrm{xV_{DD}}$-tolerant logic gates. The proposed $2\mathrm{xV_{DD}}$-tolerant PVT detector is also shown in Fig. 8. Each logic circuit consists of $2\mathrm{xV_{DD}}$-tolerant logic gates to have $2\mathrm{xV_{DD}}$ tolerant capability. The delay chain buffers (Shift_B and B0-B6) are composed of $2\mathrm{xV_{DD}}$-tolerant NOT gates, and the register (positive edge-triggered D flip flop) is composed of eight $2\mathrm{xV_{DD}}$-tolerant NAND gates. Thus, the proposed PVT detector can be operated under the $2\mathrm{xV_{DD}}$ voltage domain and receive the $2\mathrm{xV_{DD}}$ clock signal.

In the beginning, the reference clock (CLK) delivers the $0\ \mathrm{V} - 2\mathrm{xV_{DD}}$ clock signal into the delay chain buffers. Then, the output signal from each delay buffer is loaded to the register at the clock rising edge. Since the propagation delay of the

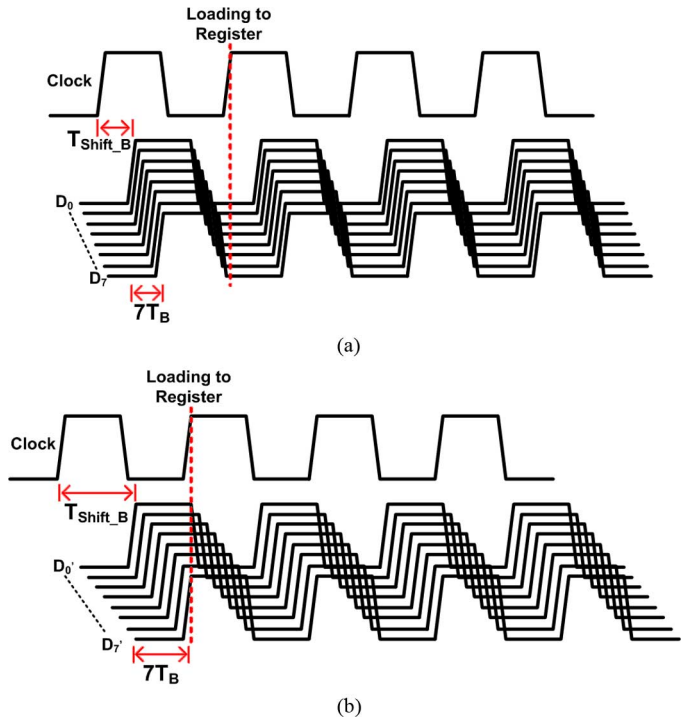


Fig. 11. Timing chart of the delay buffers in (a) the fastest conditions and (b) the slowest conditions.

delay buffer depends on PVT variations, more compensation for driving capability is needed with more logic high signals loaded into the registers. Finally, the data in the registers are used to generate an 8-bit pre-control signal D0 to D7 by the series $2\mathrm{xV_{DD}}$-tolerant NOR gates. For example, in the fastest condition, no logic high signal is loaded into the register; the pre-control signal presents the code "00000000". On the other hand, the logic high signals are loaded into all registers in the slowest condition, leading to the pre-control code of "10000000". To provide the correct compensation codes within one clock cycle time, the delay time of the buffers needs to meet the following requirements:

$$[T_{\mathrm{total\_delay\_min}} = (T_{\mathrm{Shift\_B}} + 7T_B)_{\mathrm{min}}] > \frac{1}{2}T_{\mathrm{Clock}} \quad (1)$$

$$[T_{\mathrm{total\_delay\_max}} = (T_{\mathrm{Shift\_B}} + 7T_B)_{\mathrm{max}}] < T_{\mathrm{Clock}} \quad (2)$$

$$7T_B < \frac{1}{2}T_{\mathrm{Clock}}. \quad (3)$$

The total delay time is formed by the shift buffer $(\mathrm{T_{Shift\_B}})$ and seven buffers $(7\mathrm{T_B})$. The minimum delay time $\mathrm{T_{total\_delay\_min}}$ in the fastest condition should be longer than 1/2 clock cycle time $(\mathrm{T_{Clock}})$, as shown in Fig. 11(a). The maximum delay time $\mathrm{T_{total\_delay\_max}}$ in the slowest conditions should be shorter than one clock cycle time, as showing in Fig. 11(b). Besides, the delay time of buffers $7\mathrm{T_B}(\mathrm{B0} \sim \mathrm{B6})$ should be shorter than 1/2 clock cycle time to avoid loading wrong bits to the registers.

C. $2xV_{DD}$-Tolerant 8-to-3 Encoder

To control the 3-stages output drivers, the 8-bit pre-control signal is encoded to a 3-bit compensation code. Table IV shows

TABLE IV
TRUTH $2xV_{DD}$-TOLERANT 8 TO 3 ENCODER

D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

the truth table of this encoder. According to the truth table, the encoder can be realized with three 4-input $2xV_{DD}$-tolerant NOR gates as shown in Fig. 8. Moreover, the compensation code provided by the 8-to-3 encoder with $2xV_{DD}$ voltage signal is separated to two operating voltage regions to control the pull-high stages and pull-low stages of the output driver. In this design, the encoded signal S0-S2 is separated to the $0\ V - V_{DD}$ signal $S0_L - S2_L$ to control the pull-low stages (M_{NN0}, M_{NN1}, and M_{NN2}) and the $V_{DD} - 2xV_{DD}$ signal $S0_H - S2_H$ to control the pull high stages (M_{PP0}, M_{PP1}, and M_{PP2}).

D. Simulation Results

The circuit behaviors are verified by HSPICE simulation with device models in a 90-nm CMOS process. Fig. 12(a) shows the simulated voltage waveforms of the $2xV_{DD}$-tolerant I/O buffer with a 125-MHz 0 V-1.2 V voltage signal at Dout and 15-pF loading at I/O pad in transmitting mode. During transmitting mode, the gate-controlled circuit successfully provides the 1.2 V gate bias voltage. With the dynamic source voltage at node A (1.2 V-2.5 V) and node B (0 V-1.2 V), the 0 V-2.5 V voltage signal can be successfully transmitted to I/O pad. Fig. 12(b) shows the simulated voltage waveforms with a 125-MHz 0 V-2.5 V voltage signal at I/O pad in receiving mode. Nodes A and B are biased at 1.2 V. The gate-controlled circuit provides the 1.2 V-2.5 V bias voltage at TP and 0 V-1.2 V bias voltage at TN. The corresponding circuit logics and devices' behavior of the proposed $2xV_{DD}$-tolerant I/O buffer in two operation modes are summarized in Table V. According to the simulated results, the maximum voltage across any two terminals of each transistor in the proposed $2xV_{DD}$-tolerant I/O buffer is kept below $1xV_{DD}$. Therefore, the proposed $2xV_{DD}$-tolerant I/O buffer with only $1xV_{DD}$ devices can be successfully operated in $2xV_{DD}$ signal domain without suffering the gate-oxide reliability issue.

In order to observe the compensation efficiency, the slew rates of the output waveforms without and with PVT compensation are compared. The rise and fall slew rates are defined as following equations:

$$SR_{\text{rise}} = \frac{0.9 \times V_{\text{DDH}} - 0.1 \times V_{\text{DDH}}}{T_{\text{rise}}} \quad (4)$$

$$SR_{\text{fall}} = \frac{0.9 \times V_{\text{DDH}} - 0.1 \times V_{\text{DDH}}}{T_{\text{fall}}}. \quad (5)$$

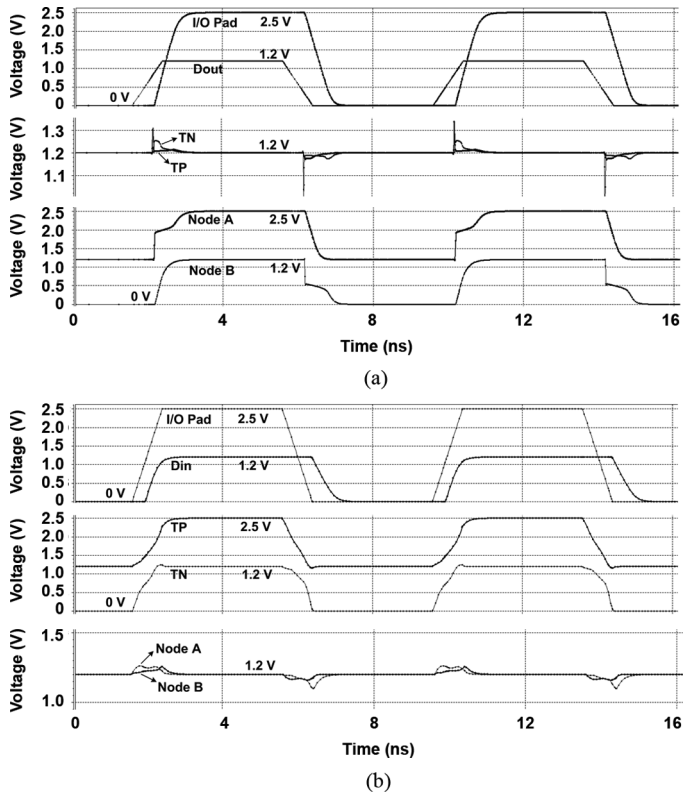


Fig. 12. Simulated waveforms of the proposed I/O buffer with 125-MHz signals in (a) transmitting mode and (b) receiving mode.

TABLE V
CORRESPONDING CIRCUIT LOGICS AND NODE VOLTAGES OF THE PROPOSED $2xV_{DD}$-TOLERANT I/O BUFFER

Operation Mode	Dout	PUH	PD	Node A	Node B	TP	TN	I/O Pad
Transmitting	0V	$2xV_{DD}$	V_{DD}	V_{DD}	0V	V_{DD}	V_{DD}	0V
	V_{DD}	V_{DD}	0V	$2xV_{DD}$	V_{DD}	V_{DD}	V_{DD}	$2xV_{DD}$
Receiving		$2xV_{DD}$	0V	V_{DD}	V_{DD}	V_{DD}	0V	0V
		$2xV_{DD}$	0V	V_{DD}	V_{DD}	$2xV_{DD}$	V_{DD}	$2xV_{DD}$

The V_{DDH} is 2.5 V, SR_{rise} is the slew rate when output transits from $0.1xV_{DDH}$ to $0.9xV_{DDH}$, and SR_{fall} is the slew rate when output transits from $0.9xV_{DDH}$ to $0.1xV_{DDH}$. Tables VI and VII list the simulated slew rates of the proposed $2xV_{DD}$-tolerant I/O buffer without and with PVT compensation. The process variation includes three process corners, which are fast-fast (FF), typical-typical (TT), and slow-slow (SS). Five supply voltages within $\pm 10\%$ variation from the normal value are used in the simulation with the step of 5% V_{DD} voltage. The temperature conditions from $0°C$ to $125°C$ are applied with the step of $25°C$. As listed in Table VI, without PVT compensation, the maximum variation of $SR_{rise}(SR_{fall})$ is 1.92 V/ns (2.02 V/ns). After applying PVT compensation, the maximum variation of $SR_{rise}(SR_{fall})$ is decreased to 1.2 V/ns (1.15 V/ns). The corresponding compensation codes (S0,

TABLE VI
OUTPUT SLEW RATE OF THE PROPOSED $2xV_{DD}$-TOLERANT I/O BUFFER WITHOUT PVT COMPENSATION

FF	Supply Voltage (V_{DD}/V_{DDH})				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	2.25 / 2.31	2.53 / 2.60	2.82 / 2.88	3.11 / 3.16	3.41 / 3.40
50 °C	2.18 / 2.22	2.45 / 2.49	2.73 / 2.76	3.00 / 3.03	3.29 / 3.30
75 °C	2.12 / 2.13	2.37 / 2.38	2.64 / 2.64	2.91 / 2.90	3.19 / 3.16
100 °C	2.06 / 2.04	2.31 / 2.28	2.56 / 2.28	2.82 / 2.77	3.09 / 3.02
125 °C	2.00 / 1.95	2.24 / 2.18	2.49 / 2.41	2.74 / 2.65	3.00 / 2.90
TT	**Supply Voltage (V_{DD}/V_{DDH})**				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	1.95 / 1.89	2.21 / 2.15	2.48 / 2.41	2.75 / 2.68	3.02 / 2.95
50 °C	1.89 / 1.82	2.14 / 2.06	2.40 / 2.31	2.66 / 2.57	2.93 / 2.83
75 °C	1.84 / 1.74	2.08 / 1.98	2.33 / 2.22	2.58 / 2.46	2.84 / 2.71
100 °C	1.79 / 1.67	2.03 / 1.90	2.26 / 2.13	2.50 / 2.36	2.76 / 2.60
125 °C	1.75 / 1.61	1.97 / 1.82	2.20 / 2.04	2.44 / 2.26	2.68 / 2.48
SS	**Supply Voltage (V_{DD}/V_{DDH})**				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	1.65 / 1.56	1.89 / 1.73	2.14 / 1.97	2.39 / 2.23	2.65 / 2.48
50 °C	1.61 / 1.51	1.84 / 1.66	2.08 / 1.90	2.32 / 2.14	2.57 / 2.38
75 °C	1.57 / 1.47	1.79 / 1.60	2.02 / 1.82	2.25 / 2.05	2.49 / 2.29
100 °C	1.53 / 1.43	1.74 / 1.54	1.96 / 1.75	2.19 / 1.97	2.42 / 2.19
125 °C	1.49 / 1.38	1.70 / 1.48	1.91 / 1.68	2.13 / 1.89	2.36 / 2.10

TABLE VII
OUTPUT SLEW RATE OF THE PROPOSED $2xV_{DD}$-TOLERANT I/O BUFFER WITH PVT COMPENSATION

FF	Supply Voltage (V_{DD}/V_{DDH})				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	2.20 / 2.10	2.43 / 2.36	2.70 / 2.61	2.98 / 2.86	3.26 / 3.12
50 °C	2.40 / 2.43	2.36 / 2.26	2.62 / 2.51	2.90 / 2.75	3.17 / 3.00
75 °C	2.61 / 2.69	2.63 / 2.61	2.56 / 2.41	2.75 / 2.64	3.08 / 2.88
100 °C	2.78 / 2.88	2.86 / 2.89	2.85 / 2.78	2.75 / 2.53	3.00 / 2.76
125 °C	2.93 / 3.00	3.04 / 3.08	3.08 / 3.06	3.05 / 2.92	2.93 / 2.64
TT	**Supply Voltage (V_{DD}/V_{DDH})**				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	2.63 / 2.67	2.44 / 2.37	2.39 / 2.21	2.65 / 2.45	2.91 / 2.70
50 °C	2.76 / 2.79	2.65 / 2.62	2.66 / 2.55	2.58 / 2.36	2.83 / 2.59
75 °C	2.69 / 2.68	2.82 / 2.80	2.88 / 2.81	2.87 / 2.72	2.76 / 2.50
100 °C	2.80 / 2.75	2.96 / 2.92	3.07 / 3.01	3.10 / 3.00	3.07 / 2.87
125 °C	2.90 / 2.79	3.08 / 2.99	3.22 / 3.13	3.30 / 3.20	3.32 / 3.16
SS	**Supply Voltage (V_{DD}/V_{DDH})**				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	2.56 / 2.45	2.75 / 2.66	2.83 / 2.52	2.65 / 2.48	2.57 / 2.30
50 °C	2.65 / 2.50	2.69 / 2.56	2.81 / 2.69	2.87 / 2.73	2.86 / 2.65
75 °C	2.59 / 1.40	2.80 / 2.63	2.95 / 2.81	3.06 / 2.91	3.09 / 2.92
100 °C	2.67 / 2.42	2.88 / 2.68	3.07 / 2.89	3.21 / 3.04	3.29 / 3.12
125 °C	2.61 / 2.33	2.82 / 2.57	2.99 / 2.77	3.33 / 3.12	3.40 / 3.25

S1, s2) which generated in the proposed $2xV_{DD}$-tolerant PVT variation detector are listed in Table VIII.

V. EXPERIMENTAL RESULTS

The proposed mixed-voltage I/O buffer with PVT compensation has been fabricated in a 90-nm CMOS process with only 1.2-V devices. Fig. 13 shows the die photo of the whole $2xV_{DD}$-tolerant I/O buffer with and without PVT compensation. In order to observe the $2xV_{DD}$-tolerant PVT variation detector's behavior, the circuit also has been fabricated stand-alone in test chip as shown in Fig. 14.

A. Measured Results of $2xV_{DD}$-Tolerant PVT Detector

Fig. 15 shows the measurement setup to verify the compensation function of $2xV_{DD}$-tolerant PVT detector. The pulse generator Agilent 8133A was used to provide the clock signal. With the supply voltage and temperature changes during measurement, the PVT detector provides the compensation codes from S0 to S2 which were displayed on the LED. Since the foundry only provides the test chips fabricated in the typical TT process corner, the measured results are merely available in this process corner. The measured compensation codes are summarized in Table IX. After changing the supply voltage and temperature, the compensation code is observed to increase as the operating condition becomes worse.

B. Measured Results of $2xV_{DD}$-Tolerant I/O Buffer With PVT Compensation

Figs. 16(a) and 16(b) show the measured voltage waveforms of $2xV_{DD}$-tolerant I/O buffer in transmitting mode and receiving mode, respectively. The data rate verified in those-figures is 125-MHz. As showing in Fig. 16(a), the proposed $2xV_{DD}$-tolerant I/O buffer can successfully transmit an internal 0 V-1.2 V voltage signal to a 0 V-2.5 V voltage signal at I/O pad in transmitting mode. Besides, the proposed $2xV_{DD}$-tolerant I/O buffer can successfully receive the 0 V-2.5 V voltage signal at I/O pad, as showing in Fig. 16(b), where the input data was successfully converted to a 0 V-1.2 V voltage signal at Din1. Measured results have demonstrated that the proposed $2xV_{DD}$-tolerant I/O buffer can provide the correct functions.

To observe the efficiency of PVT compensation with varied supply voltages, Figs. 17(a)–17(c) show the measured output waveforms with different supply voltages at temperature of $25°C$. With the V_{DD}/V_{DDH} voltage of 1.32 V/2.75 V, the PVT detector provides the compensation code "001" to the buffer (as listed in Table IX). However, under this higher operating voltage condition, the output waveforms without and with PVT compensation do not have obvious difference, as shown in Fig. 17(a). When V_{DD}/V_{DDH} voltage is decreased to 1.2 V/2.5 V, the PVT detector provides the compensation signal "011" to the buffer (as listed in Table IX). Comparing the output waveforms with PVT compensation, the output waveforms without PVT compensation are significantly degraded, as shown in

TABLE VIII
SIMULATED COMPENSATION CODES FROM THE PROPOSED $2xV_{DD}$-TOLERANT PVT DETECTOR

FF	Supply Voltage (V_{DD}/V_{DDH})				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	(0, 0, 0)	(0, 0, 0)	(0, 0, 0)	(0, 0, 0)	(0, 0, 0)
50 °C	(0, 0, 1)	(0, 0, 0)	(0, 0, 0)	(0, 0, 0)	(0, 0, 0)
75 °C	(0, 1, 0)	(0, 0, 1)	(0, 0, 0)	(0, 0, 0)	(0, 0, 0)
100 °C	(0, 1, 1)	(0, 1, 0)	(0, 0, 1)	(0, 0, 0)	(0, 0, 0)
125 °C	(1, 0, 0)	(0, 1, 1)	(0, 1, 0)	(0, 0, 1)	(0, 0, 0)
TT	**Supply Voltage (V_{DD}/V_{DDH})**				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	(0, 1, 0)	(0, 0, 1)	(0, 0, 1)	(0, 0, 0)	(0, 0, 0)
50 °C	(0, 1, 1)	(0, 1, 0)	(0, 0, 1)	(0, 0, 0)	(0, 0, 0)
75 °C	(1, 0, 0)	(0, 1, 1)	(0, 1, 0)	(0, 0, 1)	(0, 0, 0)
100 °C	(1, 0, 1)	(1, 0, 0)	(0, 1, 1)	(0, 1, 0)	(0, 0, 1)
125 °C	(1, 1, 0)	(1, 0, 1)	(1, 0, 0)	(0, 1, 1)	(0, 1, 0)
SS	**Supply Voltage (V_{DD}/V_{DDH})**				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	(1, 0, 1)	(1, 0, 0)	(0, 1, 1)	(0, 1, 0)	(0, 0, 1)
50 °C	(1, 1, 0)	(1, 0, 1)	(1, 0, 0)	(0, 1, 1)	(0, 1, 0)
75 °C	(1, 1, 1)	(1, 1, 0)	(1, 0, 1)	(1, 0, 0)	(0, 1, 1)
100 °C	(1, 1, 1)	(1, 1, 1)	(1, 1, 0)	(1, 0, 1)	(1, 0, 0)
125 °C	(1, 1, 1)	(1, 1, 1)	(1, 1, 1)	(1, 1, 0)	(1, 0, 1)

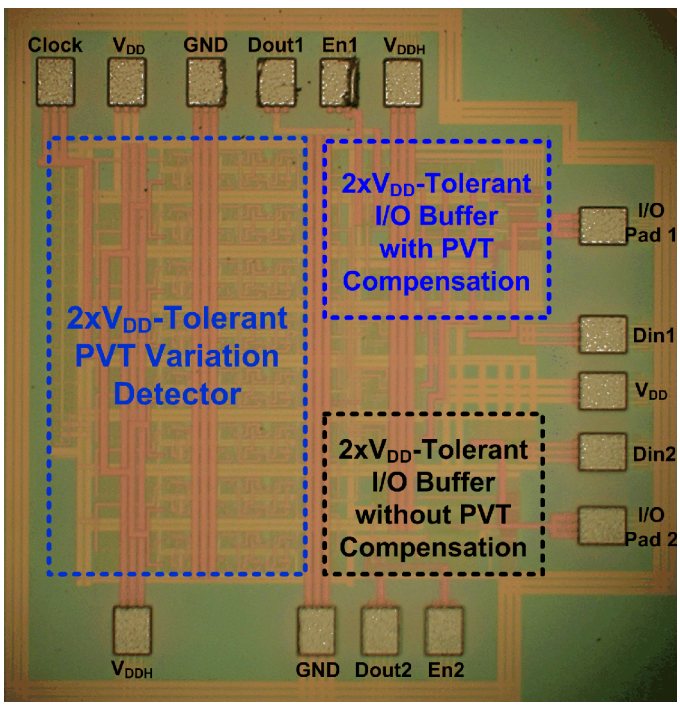


Fig. 13. Die photo of the $2xV_{DD}$-tolerant I/O buffers with and without PVT compensation.

Fig. 17(b). When V_{DD}/V_{DDH} voltage is further decreased to the worst case of 1.08 V/2.25 V, the output waveform without

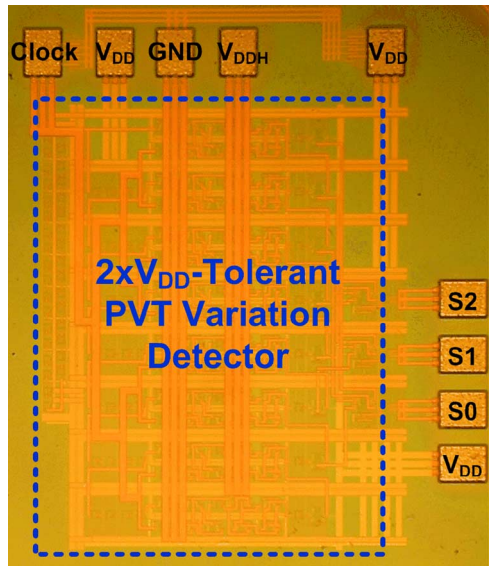


Fig. 14. Die photo of the proposed $2xV_{DD}$-tolerant PVT detector, which is realized by 1.2-V devices in a 90-nm CMOS process for 2.5-V circuit application.

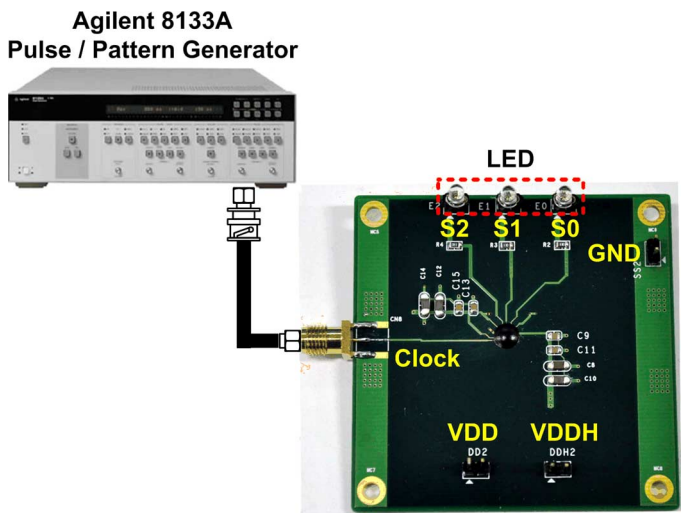


Fig. 15. Measurement setup for the $2xV_{DD}$-tolerant PVT detector.

TABLE IX
MEASURED COMPENSATION CODES FROM THE PROPOSED $2xV_{DD}$-TOLERANT PVT DETECTOR

TT	Supply Voltage (V_{DD}/V_{DDH})				
	(1.08/2.25)	(1.14/2.375)	(1.2/2.5)	(1.26/2.625)	(1.32/2.75)
25 °C	(1, 0, 1)	(1, 0, 0)	(0, 1, 1)	(0, 1, 0)	(0, 0, 1)
50 °C	(1, 1, 0)	(1, 0, 1)	(1, 0, 0)	(0, 1, 1)	(0, 1, 0)
75 °C	(1, 1, 1)	(1, 1, 0)	(1, 0, 1)	(1, 0, 0)	(0, 1, 0)
100 °C	(1, 1, 1)	(1, 1, 1)	(1, 1, 0)	(1, 0, 1)	(1, 0, 0)
125 °C	(1, 1, 1)	(1, 1, 1)	(1, 1, 1)	(1, 1, 0)	(1, 0, 1)

PVT compensation is degraded more seriously, as shown in Fig. 17(c). To observe the efficiency of PVT compensation at different temperatures, Figs. 18(a) and 18(b) show the measured output waveform at 25°C and 125°C with V_{DD}/V_{DDH} of 1.2 V/2.5 V, respectively. Without PVT compensation, the output

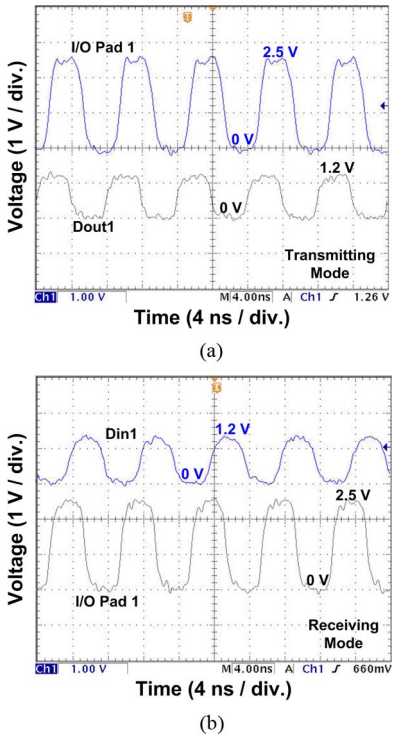


Fig. 16. Measured results of the proposed $2xV_{DD}$-tolerant I/O buffer in (a) transmitting mode and (b) receiving mode.

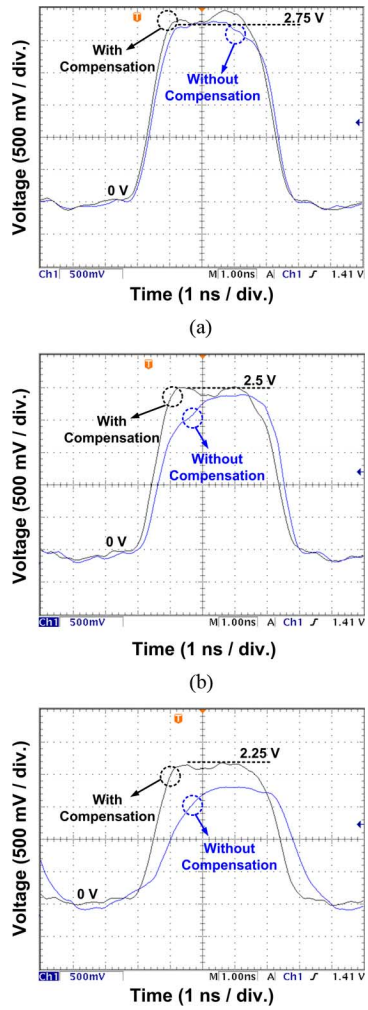


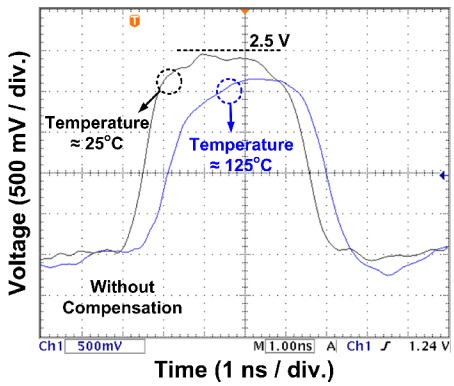
Fig. 17. Measured output waveform of the proposed $2xV_{DD}$-tolerant I/O buffer with VDD/VDDH voltage of (a) 1.32-V/2.75-V, (b) 1.2-V/2.5-V, and (c) 1.08-V/2.25-V.

waveform has seriously degradation at high temperature. With PVT compensation to adjust the driving capability against PVT variation, the output waveform is more preferable.

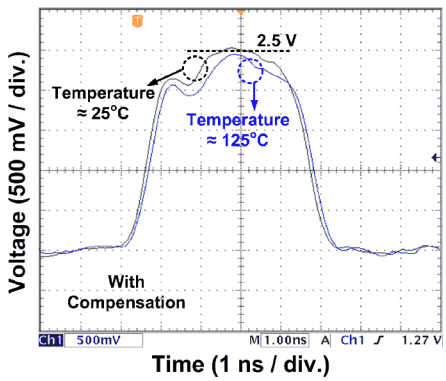
VI. Discussion

About the transistors size in output driver, the size should be designed to meet the specifications of the desired application. However, a single size of output driver will not satisfy in all process corners and operating conditions. Therefore, the PVT compensation is needed to the I/O buffer, especially when it is realized in the nanoscale CMOS processes. In this work, the M_{PPX} and M_{NNX} are designed to mitigate the difference of output slew rate. As shown in Fig. 19, under the poor condition of slow process corner, M_{PPX} and M_{NNX} should be turned on to enhance the output slew rate. On the contrary, under good condition of fast process corner, M_{PPX} and M_{NNX} should be kept off to decrease output slew rate. Moreover, according to the operating conditions due to different PVT variations, M_{PPX} and M_{NNX} are also separated to several stages. By selecting the compensation codes, different stages of M_{PPX} and M_{NNX} can be turned on to adjust the output slew rate. Therefore, the difference of output slew rates in different conditions can be mitigated. In this work, 3-bit compensation code is satisfied to compensate the PVT variation in the given 90-nm CMOS process. Theoretically, more compensation bits will have better accuracy. However, it will increase the fabrication cost due to the overhead of additional circuits to occupy more layout area.

Between the proposed design and the prior designs of mixed-voltage I/O buffers, some advantages and drawbacks are compared in the Table X. The proposed design can successfully mitigate the serious PVT variation issue, but the PVT detection circuit would occupy more silicon area as compared to the prior works of mixed-voltage I/O buffers. Although the output buffer could be designed with the larger device dimensions to enhance the driving capability and to further compensate some PVT variation issue. However, the SSN issue or ground bounce due to the large driving/switching current would degrade the circuit performance again. Fortunately, the PVT detection circuit and some circuitry can be shared by a group of mixed-voltage I/O buffers, which are in the same power domain and placed at the same block in the chip layout. Thus, the overhead of silicon area for each I/O buffer to implement the PVT compensation can be reduced by the arrangement of sharing the PVT detection circuit. Moreover, comparing with simulated and measured results in the compensation codes (as listed in Tables VIII and IX), the measured compensation code is larger than simulated results. Thus, the real condition inside the fabricated silicon chip is worse than the simulation condition, which means the PVT compensation becomes more important for practical application.



(a)



(b)

Fig. 18. Measured output waveforms of the proposed $2xV_{DD}$-tolerant I/O buffer (a) without PVT compensation and (b) with PVT compensation, under different temperatures.

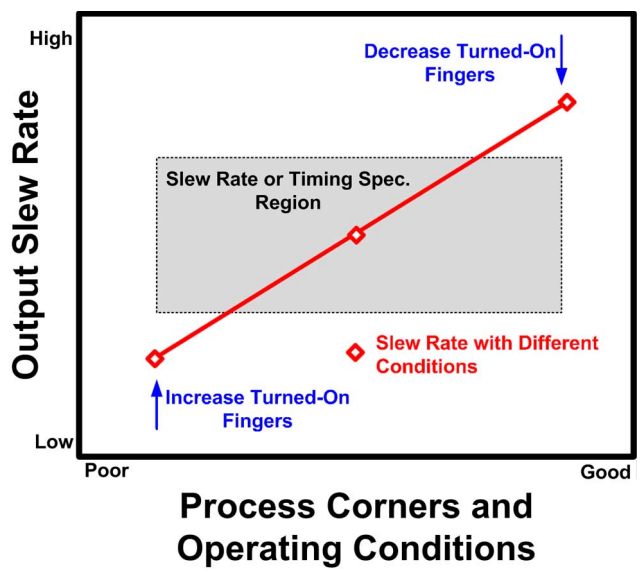


Fig. 19. PVT compensation concept proposed in this work.

In the PVT detector, the delay time can easily be quantified to generate the compensation code, but some limitations exist in this structure. To provide the correct compensation code to the I/O buffer, the delay time of delay cell is dependent on the clock cycle time, so there is an upper limit on the operating frequency.

TABLE X
COMPARISON ON THE FEATURES AMONG THE MIXED-VOLTAGE I/O BUFFERS

Mixed-Voltage I/O Designs	N-Well Bias	Gate-Oxide Reliability Issue	Extra Device Used	Transmit	Receive	PVT Compensation	Area	Power Consumption
Ref. [9]	Yes (Dynamic Bias)	Yes	No	$1xV_{DD}$	$2xV_{DD}$	No	Small	Low
Ref. [10]	No (Fixed Bias) (Extra Pad)	No	Yes (Depletion PMOS)	$1xV_{DD}$	$2xV_{DD}$	No	Small	Low
Ref. [11]	Yes (Dynamic Bias)	No	No	$1xV_{DD}$	$2xV_{DD}$	No	Small	Low
Ref. [12]	Yes (Dynamic Bias)	No	No	$1xV_{DD}$	$2xV_{DD}$	No	Small	Low
Ref. [13]	No (Fixed Bias)	No	No	$1xV_{DD}$	$2xV_{DD}$	No	Small	Low
Ref. [14]	No (Fixed Bias)	No	No	$2xV_{DD}$	$2xV_{DD}$	No	Midium	Midium
Ref. [15]	Yes (Dynamic Bias)	No	No	$1/2xV_{DD}$~ $3xV_{DD}$	$1/2xV_{DD}$~ $3xV_{DD}$	No	Midium	Midium
Ref. [16]	Yes (Dynamic Bias)	No	No	$1/2xV_{DD}$~ $3xV_{DD}$	$1/2xV_{DD}$~ $3xV_{DD}$	No	Midium	Midium
This Work	No (Fixed Bias)	No	No	$2xV_{DD}$	$2xV_{DD}$	Yes	Large	High

With this limitation, this structure cannot compensate the circuits that have different operating frequencies. Besides, the percentage of delay time formed by the pMOS and nMOS cannot be discriminated. So, the PVT detector provides the same control signal to pMOS and nMOS drivers. Namely, this structure would not correctly adjust the driving capability in the slow-fast (SF) or fast-slow (FS) conditions, in which nMOS and pMOS has variation in the opposite direction.

VII. CONCLUSION

A new $2xV_{DD}$-tolerant I/O buffer with PVT compensation has been proposed and verified in a 90-nm CMOS process. With dynamic source bias and gate-control technique, the $2xV_{DD}$-tolerant I/O buffer and the $2xV_{DD}$-tolerant logic gates can be implemented by using only $1xV_{DD}$ devices. Moreover, $2xV_{DD}$-tolerant PVT detector can be realized by the $2xV_{DD}$-tolerant logics gates to detect the PVT variation in the $2xV_{DD}$ voltage domain and provide the compensation function for the $2xV_{DD}$-tolerant I/O buffer. Experimental results show that the proposed $2xV_{DD}$-tolerant I/O buffer with PVT compensation is suitable for mixed-voltage interface applications to mitigate PVT variation without suffering gate-oxide overstress issue. The $2xV_{DD}$-tolerant logic gates proposed in this work can be used in other circuits those facing the mixed-voltage interfaces in a microelectronic system.

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Ming-Dou Ker (F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1993.

He was a Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu. During 2008–2011, he was rotated to be Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. Now, he has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University (NCTU), Taiwan; as well as the Dean of College of Photonics, NCTU. He served as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan during 2010–2011; and currently serving as the Executive Director of National Science and Technology Program on Nano Technology (NPNT) in Taiwan (2011—2014). In the technical field of reliability and quality design for microelectronic circuits and systems, he has published over 450 technical papers in international journals and conferences. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with hundreds of U.S. patents and Taiwan patents. He had been invited to teach and/or consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, circuits and systems for information displays, as well as the biomimetic circuits and systems for biomedical applications.

Dr. Ker has served as member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He ever served as the Associate Editor for the IEEE TRANSACTIONS ON VLSI SYSTEMS during 2006-2007. He was selected as a Distinguished Lecturer in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–2012). He was the Founding President of Taiwan ESD Association. Since 2012, he has served as the Editor of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY.

Po-Yen Chiu (S'08) received the B.S. degree from the Department of Electrical Engineering, Tam-Kang University, Taipei, Taiwan, in 2005, and the M.S. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 2008. He is currently working toward the Ph.D. degree in the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

His current research interests include ESD protection design for CMOS integrated circuits, mixed-voltage I/O interface circuits, and analog circuit design.