A Digital Golay-MPIC Time Domain Equalizer for SC/OFDM Dual-Modes at 60 GHz Band

Wei-Chang Liu, Fu-Chun Yeh, Ting-Chen Wei, Ching-Da Chan, and Shyh-Jye Jou

***Abstract*—In this paper, a digital time domain equalizer (TDE) for 60 GHz radio frequency transmission systems is presented. Significantly, the TDE supports both single carrier (SC) and orthogonal frequency-division multiplexing (OFDM) operation modes for digital baseband receiver. In order to improve the performance, the proposed TDE adopts Golay sequence aided one-shot channel estimation and modified multi-path interference cancellation (MPIC) equalization. Targeting on the line-of-sight (LOS) channel characteristic, MPIC is simplified with single-tap for complexity reduction. From the area efficiency point of view, both SC and OFDM modes are designed within a single hardware to yield 99% of area sharing. The Golay-MPIC TDE structure is realized as feed-forward data path with 8X-parallelism to achieve 2.64 GS/s at 330 MHz clock rate. The Golay-MPIC TDE is fabricated as a part of a digital baseband with 65 nm 1P9M general purpose process. The area of Golay-MPIC TDE occupies 1.05 mm^2 with 405 K gate counts. Besides, the power dissipations for SC and ODFM modes are 56.71 mW@220 MHz (1 V) and 91.29 mW@330 MHz (1.1 V), respectively. Finally, the chip can provide the maximum throughput 15.84 Gb/s (2.64 GS/s with 64-QAM modulation).**

***Index Terms*—Dual modes, OFDM, SC, time domain equalizer, WPAN, 60 GHz, 802.15.3c.**

I. Introduction

THE unlicensed 60 GHz radio frequency (RF) band is a new opportunity to achieve multi-gigabit transmission rate in indoor wireless transmission environment. A number of previous works in [1] and references therein presented that the 60 GHz band has the characteristics of highly directional, highly atmospheric absorption, narrow beamwidth and no rich multi-path effect. For digital home applications, the 60 GHz band transmission is adopted in three standards to reach beyond gigabit per second (Gb/s) in wireless transmission and mitigate the cable tied routing, specifically IEEE 802.15.3c wireless personal area network (WPAN) [2], IEEE 802.11ad wireless local area network (WLAN) [3], and ECMA TC387 [4]. The applications include high definition multimedia interface (HDMI) cable replacement, uncompressed high definition (HD) video streaming (instead of the compressed HD video stream [5]), HD audio/video source/sink and data transmission. The IEEE 802.15.3c standard provides three PHY modes including single carrier (SC), high-speed interface (HSI), and audio/visual (AV) modes. The SC PHY uses single carrier modulation whereas the HSI and AV PHYs employ orthogonal frequency-division multiplexing (OFDM) modulation. In contrast, the IEEE 802.11ad standard provides two PHY modes, such as SC and OFDM. Both of the IEEE standards are proposed for the indoor wireless transmission with more than Gb/s data rate and operated at 60 GHz RF band. The experiment results [6]–[9] indicate that the multi-path effects, caused by the reflection, can be mitigated by directional antenna. Also, for 60 GHz RF band, the reflected signal has serious attenuation by wall reflection. Thus, the RMS delay spread of 60 GHz transmission is less than that of low frequency bands [7], [9]. In addition, the beamforming technique is adopted in both IEEE standards to enhance the transmission power and further realize the line-of-sight (LOS) environment.

Prior works focused on mixed-signal synchronization to support high-speed operation [10]–[12]. The approaches only provide simple modulation scheme up to QPSK. The feedback loop from the digital-domain to analog-domain results in system stability issue. Furthermore, the error propagation problem in the subsequent decision feedback equalizer (DFE), only applicable for SC transmission, leads to performance loss. Fortunately, the main trend in modern transmission system design is digital baseband transceivers with all-digital synchronization scheme, in which no feedback loop exists from digital domain to analog domain. In general, the digital baseband contains three main blocks, which are all-digital synchronization, channel estimation/equalization and data demodulation. The most important part is the channel estimation/equalization. For channel equalization, OFDM modulation has the advantage of inter symbol interference (ISI) free property and easy equalization for frequency-selective channel [13] with frequency domain equalizer (FDE). As for SC modulation, the ISI degrades the system performance and the computational complexity of time domain equalizer (TDE) is proportional to the RMS delay spread [14] of multipath fading channel.

The SC and HSI modes in IEEE 802.15.3c and the SC and OFDM modes in IEEE 802.11ad consist of the similar preamble and payload structure. Therefore, to implement an equalizer in a single hardware structure with the same estimation/equalization method to achieve the least hardware cost and maximum hardware sharing between SC and OFDM modes of these two standards are possible. In addition, it is a great challenge to simultaneously achieve the specified high sampling rate and maintain low hardware complexity. As a result, parallel architectures are adopted to solve the dilemmas of high sampling rate and hardware complexity.

Digital equalizers such as [14], [15] and [16] are proposed to eliminate the channel effects and be applicable for digital baseband. The least square (LS) and least-mean-squares (LMS) frequency domain equalizer in [14] has the problem of noise enhancement in the first LS stage which will result in performance

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degradation. Another concern is the performance saturation in high SNR under OFDM mode. The efficient Golay correlator adopted in [15] and [16] provides more accuracy channel estimation as compared with LS. The Golay correlator has the same function as matched filter but with less hardware cost. However, AWGN noise influences the accuracy of the estimated channel impulse response (CIR). As a result, the performance droops while transforming from channel impulse response in time domain to channel frequency response (CFR) in frequency domain. This phenomenon impacts the performance of MMSE equalizer. In [16], the channel is estimated and equalized at the same domain. Although it performs superior performance with less hardware cost, only applicable for SC transmission and BPSK modulation is the shortcoming. In additional, the hardware complexity grows significantly while supporting higher QAM modulations.

The hardware complexity of linear equalizer is much more sensitive to the length of CIR spread than that of multi-path interference cancellation (MPIC) structure [17]. The data storage requirements and iteratively channel cancellation are the major concern of MPIC. Appreciating to the highly directional characteristic and/or beamforming technique, the transmission channel can be simplified as LOS. Therefore, the complexity of equalization in time domain can be greatly reduced from MPIC structure. In summary, the design challenges of the digital equalizer for 60 GHz system are described as follows:

1) Low computational complexity algorithm of digital equalizer for 60 GHz channel characteristics.
2) Efficient equalizer architecture for SC and OFDM dual modes.
3) Very high sampling rate and beyond Gb/s throughput rate.

Considering the design issues as mentioned above, an 8X-parallelism digital TDE is proposed by using Golay sequence aided channel estimation and simplified one-tap multi-path interference cancellation (MPIC) structure for channel equalization. Since the channel estimation and equalization is operated in time domain, there is no performance loss induced by domain transformation. The equalization structure, simplified as one-tap delayed cancellation from original MPIC structure, reduces the large storage elements and iterative executions. That is because the size of storage elements and number of iteration are in proportional to the number of tap. With the one-tap time domain ISI cancellation by subtracting the multi-path channel response, the computational complexity is greatly reduced compared with the channel inversion and multi-tap FIR filter of conventional TDE. In contrast with the FDE, the proposed equalizer can be operated in SC and OFDM dual modes without additional hardware overhead.

The paper is organized as follows. The system specification and overview of the equalizer state-of-the-art are described in Section II. The proposed LOS Golay-MPIC TDE for SC and OFDM dual modes is presented in Section III. In addition, the detail algorithm, performance analysis and system architecture are addressed. The comparisons of the digital equalizers for 60 GHz band are described in Section IV with measurement results. Finally, the conclusions are given in Section V.

II. System Specifications

Although there are many methods to achieve the target of data rate beyond Gb/s in wireless communication, for example using high-order modulation scheme or multi-input and multi-output (MIMO) system [18], raising the sampling rate is the most direct way since the data rate is proportional to the sampling rate. The crucial is the usage of 60 GHz RF band, which provides large bandwidth and makes the ultra-high sampling rate to be available. With a moderate modulation scheme, the data rate could be multiple times of the sampling rate. In this way, it is easier to achieve the target beyond Gb/s data rate.

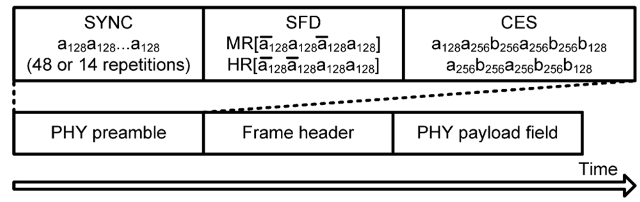

Fig. 1. PHY frame format.

A. SC and OFDM Mode Specifications of 802.15.3c

In this paper, the IEEE 802.15.3c standard is adopted as the equalizer design example because it is the first IEEE wireless standard to reach data rate beyond 1 Gb/s. The SC modulation offers lower complexity and low power operation, whereas the OFDM modulation has high spectral efficiency. Also, different data modulation schemes are provided to achieve specified data rate for different usage models [19]. The frame structure and PHY preamble of both SC and OFDM modes are specified as shown in Fig. 1. The frame synchronization (SYNC) and start frame delimiter (SFD) fields are used to carry out the frame detection and frame timing estimation, respectively. The channel estimation sequence (CES) field, which is composed of the specified complementally Golay sequences, is employed to perform channel estimation. The channel model is based on the golden sets released by IEEE 802.15 TG3c group [20]. The test channel is LOS channel model with RMS delay of 3.2 ns from [20]. The channel model contains two conspicuous tones, such as main path and reflected path with τ delay. In this paper, the design target is the realization of the equalizer for both SC and OFDM (HSI) modes of 802.15.3c within the same hardware because of the similarity of frame structure.

B. Comparison of Time and Frequency Domain Equalizer

From the hardware efficiency point of view, the equalizer hardware has to be designed to operate in both SC and OFDM modes. For the purpose to operate SC and OFDM modes within a single hardware, the equalizer must adopt the same structure for both modes. Fig. 2 illustrates the block diagram and data path for FDE and TDE in digital baseband receiver architecture of SC and OFDM modes.

The FDE for SC mode requires a pair of FFT and IFFT to transform data to frequency domain for equalization and back to time domain for data demodulation, respectively. In contrast, the FDE for OFDM mode inherently requires single FFT. As a result, the total computational overhead of FDE between SC and OFDM modes is an IFFT. Research shows that when the RMS delay spread increases to certain length, the SC-FDE has less computational complexity than the SC-TDE [21]. With the aid of cyclic prefix (CP), the SC-FDE can be implemented easily than ever before [22], [23].

The TDE requires a channel matrix inversion for coefficient update and a FIR filter for channel equalization. The computational complexity of TDE is proportional to the length of the filter taps determined by the length of CIR. However, the superiority of TDE is no overhead for both SC and OFDM modes.

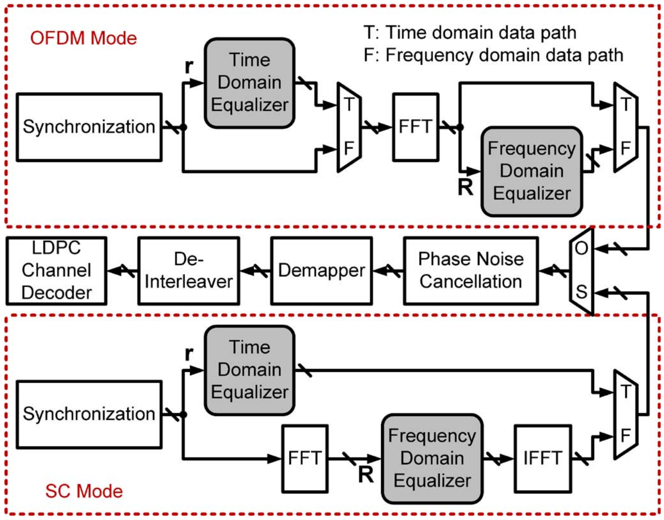

Fig. 2. Block diagram and data path for time and frequency domain equalizers.

TABLE I
SYSTEM PARAMETERS OF SC/OFDM MODE

	SC	HSI
Transmission modulation	Single carrier	OFDM
Sampling rate	1760 MHz	2640 MHz
Data modulation	π/2 BPSK, π/2 QPSK, π/2 8-PSK, π/2 16-QAM	QPSK,16-QAM, 64-QAM
Data rate (after channel decoding)	25.8 Mb/s – 5.28 Gb/s	32.1 Mb/s – 5.78 Gb/s
Block size (FFT size)	512 samples	
Pilot word (guard interval) length	64 samples	
Channel model	LOS residual model [20] RMS delay: 3.2 ns	
No. of parallelism	8 times	
Clock rate[a]	220 MHz	330 MHz

[a] Based on the proposed 8X-parallelism structure.

In summary, FDE has fixed single-tap and less computational complexity than TDE for long CIR. The drawback is that additional CP reduces the data rate. For a long CIR, the CP period has to be increased to prevent the ISI effect and maintain the circular convolution property. On the other hand, the conventional TDE does not need CP added transmission, but it suffers from large computational complexity in the hardware implementation.

Previous works focused on FDE structures, [14] and [15], because of the fixed computational complexity. According to the high propagation attenuation and small multi-path effect of 60 GHz band environments as referred in Section I, the channel characteristics are also different from the traditional lower frequency bands. As [1], [6], [19], and [24] indicate, with the directional antennas, the channel response can be modeled as LOS situation with two paths. Besides, the second path of reflection contains much lower gain. By inspecting the channel convolution, the channel de-convolution can be simplified as a delayed cancellation. Therefore, for TDE, the matrix inversion procedure is possibly ignored and then the FIR filter can be shortened as single-tap substraction, which will be described in Section III.

C. Hardware Design Considerations

The sampling rate is specified as 1760 MHz in SC mode and 2640 MHz in OFDM mode. Therefore, the clock rate in the hardware design has to be able to operate at 2640 MHz for SC and OFDM dual modes system. There are two ways to fulfill the requirement, such as pipelined and parallel structures. Considering a system with high clock rate, long computation path and loop within the path, a deep pipelined structure is not an appropriate solution, because of the overhead of large flip-flops insertion and the extra loop delay. On the other hand, the parallel structure can be employed to reduce the clock rate and maintain the throughput at the same time. The drawback is that the area is proportional to the number of the parallelism. Fortunately, the size of memory, which occupies the large portion of area, is not increased with the number of parallelism.

In this paper, a combined parallel and pipelined structure is presented based on the following points of view. Considering the operation speed limitations of the digital and standard cells, the baseband structure is designed at 330 MHz with 8X-parallelism. Then, the data path of TDE is fulfilled as feed-forward to eliminate the feedback loop. Therefore, pipeline stages can be easily inserted to satisfy the required operation clock without performance loss and stability issue caused by long feedback delay. In summary, the system parameters are listed in Table I.

III. LOS GOLAY-MPIC TIME DOMAIN EQUALIZER

In order to obtain the accurate channel estimation and reduce the hardware complexity, the combined architecture of Golay sequence aided channel estimation and simplified multi-path interference cancellation (MPIC) equalization is proposed to realize the TDE in SC and OFDM dual modes of 60 GHz systems. Comparing to the Golay sequence aided time domain channel estimation with frequency domain equalization method as proposed in [15] and [25], no additional IFFT is required.

A. Golay-Sequence Aided Channel Estimation

Golay sequences with length N are generated by delay and weight vectors with M of each length and a recursive algorithm [26], [27]. Golay sequences are complementary sequences, which have an attractive property that the sum of their autocorrelations has single maximum peak without side lobe.

A pair of Golay sequences $\mathbf{a}_N$ and $\mathbf{b}_N$ of length N, where N is a power of 2, has the following autocorrelation property

$$\mathbf{R}_{\rm a}[i] + \mathbf{R}_{\rm b}[i] = 2N\delta[i] \tag{1}$$

where

$$\mathbf{R}_{\rm a}[i] = \sum_{n=0}^{N-i-1} \mathbf{a}_N[n+i] \times \mathbf{a}_N^*[n] \tag{2}$$

and

$$\mathbf{R}_{\rm b}[i] = \sum_{n=0}^{N-i-1} \mathbf{b}_N[n+i] \times \mathbf{b}_N^*[n] \tag{3}$$

Both CES and PCES fields as shown in Fig. 3 are constructed by Golay sequences and can be divided into two parts, "Part a" and "Part b." The CES has a regular configuration, namely, N_R repetitions of base sequences with length N and cyclic prefix and postfix with length N_{CP}. The base sequences for "Part a" and "Part b" are Golay sequences $\mathbf{a}_N$ and $\mathbf{b}_N$. Then, the total length of CES (N_{CES}) is $2(N_{CP}+N_RN)$. In IEEE 802.15.3c,

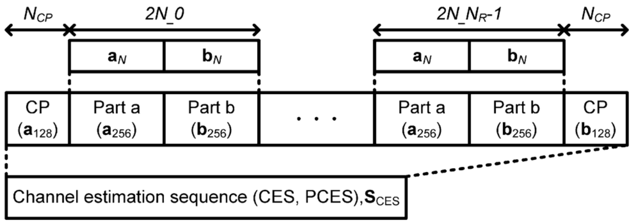

Fig. 3. Golay sequences of CES and PCES field.

$\mathbf{a}_N$ and $\mathbf{b}_N$ are $\mathbf{a}_{256}$ and $\mathbf{b}_{256}$, $\mathbf{a}_{NCP}$ and $\mathbf{b}_{NCP}$ are $\mathbf{a}_{128}$ and $\mathbf{b}_{128}$, where N is 256 and N_R is 2.

The received i^{th} sample $\mathbf{r}_{\text{CES}}$ in CES field can be expressed as

$$\mathbf{r}_{\text{CES}}[i] = \sum_{n=0}^{N_{ch}-1} \mathbf{h}[n] \times \mathbf{s}_{\text{CES}}[i-n] + \mathbf{n}[i] \tag{4}$$

where $\mathbf{s}_{\text{CES}}$ is the channel estimation sequence as shown in Fig. 3, h is the time domain CIR, N_{ch} is the length of CIR and $\mathbf{n}$ is the AWGN noise.

The Golay correlator is used to calculate the correlation values $\boldsymbol{\alpha}[i]$ and $\boldsymbol{\beta}[i]$ between the received CES and Golay sequences. Therefore, $\boldsymbol{\alpha}[i]$ and $\boldsymbol{\beta}[i]$ can be expressed as

$$\boldsymbol{\alpha}[i] = \frac{1}{N} \sum_{n=0}^{N-1} \mathbf{r}_{\text{CES}}[i+n] \times \mathbf{a}_N^*[n] \tag{5}$$

$$\boldsymbol{\beta}[i] = \frac{1}{N} \sum_{n=0}^{N-1} \mathbf{r}_{\text{CES}}[i+n] \times \mathbf{b}_N^*[n] \tag{6}$$

After removing the CP from the correlation values, the correlation values are aligned to the beginning of each Golay sequences and described as

$$\hat{\boldsymbol{\alpha}}[i] = \boldsymbol{\alpha}[i+N_{CP}], \quad i = 0, \ldots, 2N_R \times N - N - 1 \tag{7}$$

$$\hat{\boldsymbol{\beta}}[i] = \boldsymbol{\beta}[i+N_{CP}+N], \quad i = 0, \ldots, 2N_R \times N - N - 1 \tag{8}$$

Furthermore, the estimated channel $\mathbf{h}_{\text{est}}$ can be acquired as

$$\mathbf{h}_{\text{est}}[i] = \frac{1}{2N_R} \sum_{p=0}^{N_R-1} \left(\hat{\boldsymbol{\alpha}}[i+p \times 2N] + \hat{\boldsymbol{\beta}}[i+p \times 2N] \right) \tag{9}$$

Therefore, with system specified parameters, the equation can be expressed as

$$\mathbf{h}_{\text{est}}[i] = \frac{1}{4} \sum_{p=0}^{1} \left(\hat{\boldsymbol{\alpha}}[i+p \times 512] + \hat{\boldsymbol{\beta}}[i+p \times 512] \right) \tag{10}$$

The correlation result of specified Golay sequence is shown in Fig. 4. Obviously, there are two zero-correlation zones with the length of 128 before and after the main peak. Therefore, the channel impulse spread has to be restricted within these zones. Otherwise, CIR spread will ruin the orthogonality and induce performance loss. In order to conquer the pre-cursor ISI in non-line-of-sight (NLOS) channel, $\mathbf{a}_{256}$ and $\mathbf{b}_{256}$ pair, which has additional pre-zero-correlation zone compared with the autocorrelation results of $\mathbf{a}_{512}$ in [1], is used. Finally, the noiseless CIR $\mathbf{h}_{est}$ is employed to perform MPIC equalization.

B. Multi-Path Interference Cancellation Equalization

MPIC method is an efficient way to suppress inter-path interference [28]. Actually, MPIC is composed of two parts.

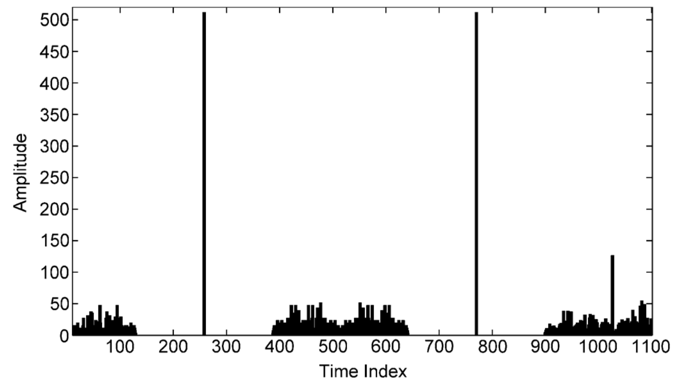

Fig. 4. Correlation result of Golay sequence.

The first part is multi-path interference replica, and the second part is multi-path interference cancellation [17], [29]. The original MPIC algorithm iteratively executes inter-path interference cancellation, which consumes lots of execution time (without loop unrolling) or leads to large latency and hardware complexity (with loop unrolling). In this system, the iteration number can be simplified as one due to the LOS channel characteristics. The cancellation is also modified using delayed cancellation to reduce the storage elements. As a result, the hardware complexity can be greatly reduced.

As mentioned in Section II, the LOS channel has only two dominant paths. Therefore, the received i^{th} sample of $\mathbf{r}$ is expressed as

$$\begin{aligned} \mathbf{r}[i] &= \mathbf{h} \cdot \mathbf{x} \\ &= \sum_{n=0}^{N_{ch}-1} \mathbf{h}[n] \times \mathbf{x}[i-n] + \mathbf{n}[i] \\ &= \mathbf{h}[0] \times \mathbf{x}[i] + \mathbf{h}[\tau] \times \mathbf{x}[i-\tau] + \mathbf{n}[i] \end{aligned} \tag{11}$$

where $\mathbf{x}$ is the transmitted data and τ is the time index of second path.

A modified MPIC from [17] has two stages, such as initial acquisition and updating stages. In initial acquisition stage, the CIR is obtained from channel estimation. The $\mathbf{x}_{\text{ini}}[i]$, which is defined as the initial data, can be derived as

$$\begin{aligned} \mathbf{x}_{\text{ini}}[i] &= \frac{\mathbf{r}[i]}{\mathbf{h}[0]} \\ &= \mathbf{x}[i] + \frac{\mathbf{h}[\tau] \times \mathbf{x}[i-\tau] + \mathbf{n}[i]}{\mathbf{h}[0]} \end{aligned} \tag{12}$$

In the following updating stage, the interference in received signal is canceled by subtracting the second path and then the result is divided by the main path gain to get the updated transmitted data $\mathbf{x}_{\text{r}}[i]$.

$$\mathbf{x}_{\text{r}}[i] = \frac{\mathbf{r}[i] - \mathbf{h}[\tau] \times \mathbf{x}_{\text{ini}}[i-\tau]}{\mathbf{h}[0]} \tag{13}$$

Without loss of generality, (13) can be simplified as

$$\mathbf{x}_{\text{r}}[i] = \mathbf{x}_{\text{ini}}[i] - \frac{\mathbf{h}[\tau] \times \mathbf{x}_{\text{ini}}[i-\tau]}{\mathbf{h}[0]} \tag{14}$$

By expanding $\mathbf{x}_{\text{ini}}[i]$ and $\mathbf{x}_{\text{ini}}[i-\tau]$, and ignoring the noise term, (14) can be rewritten as

$$\mathbf{x}_{\text{r}}[i] = \mathbf{x}[i] - \frac{\mathbf{h}[\tau]^2 \times \mathbf{x}[i-2\tau]}{\mathbf{h}[0]^2} \tag{15}$$

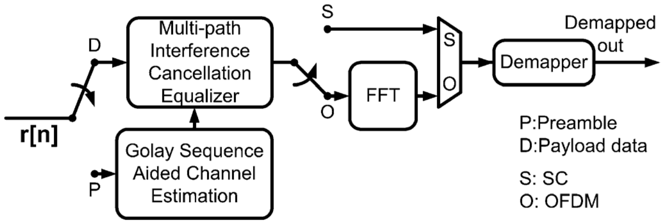

Fig. 5. Block diagram of the proposed Golay-MPIC TDE.

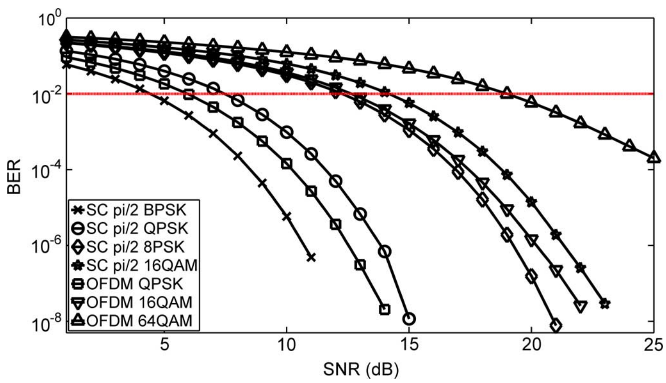

Fig. 6. Uncoded BER of the proposed Golay-MPIC TDE in LOS channel.

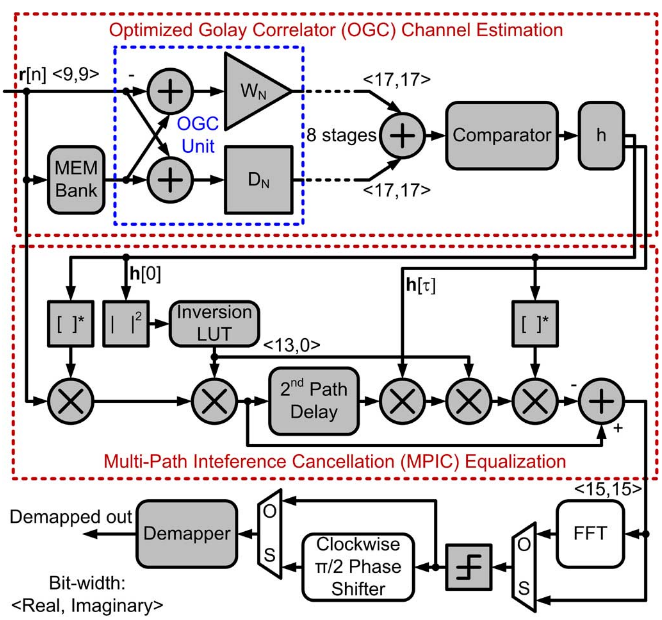

Fig. 7. Detail architecture of the proposed Golay-MPIC TDE.

Obviously, the term of $\mathbf{x}[i-2\tau]$ can be neglected since the multi-path gain $\mathbf{h}[\tau]$ is small enough to make $(\mathbf{h}[\tau]/\mathbf{h}[0])^2$ close to zero. Therefore, $\mathbf{x}_\mathrm{r}[i]$ is approximated to $\mathbf{x}[i]$.

In conclusion, only the 2nd dominant path should be considered since the path interferes the received signal. By using simplified MPIC method, the hardware complexity is reduced compared with conventional TDE. The required tap number is the multi-path number instead of proportional to the length of CIR. In this system, the tap number is one for LOS channel of 60 GHz. For NLOS channel condition, the simplified MPIC requires multiple taps to suppress the inter-path interference. Furthermore, comparing to the conventional FIR filter, the MPIC method requires one multiplication, one substraction and one division for each symbol instead of N_{ch} multiplications and $N_{ch}-1$ additions regardless of the computational complexity for matrix inversion operation.

C. Block Diagram and Data Flow

The block diagram of the proposed Golay-MPIC TDE for SC and OFDM dual modes is shown in Fig. 5, and the pseudo-code of the system flow is shown as below

```
IF (received signals==CES of preamble or PCES) THEN
    Do the one-shot Golay sequences aided channel
    estimation to evaluate the channel impulse response.
ELSE IF (received signals==payload data)
    Equalize the received data by MPIC TDE.
    CASE modulation mode OF
    SC:
        Send equalized signal to demapper.
    OFDM:
        Transform the equalized signal to frequency
        domain by FFT.
        Send frequency domain data to demapper.
    ENDCASE
ELSE
    Sleep.
END IF
```

The proposed Golay-MPIC TDE first estimates the CIR during the CES field by Golay sequence aided channel estimation. After the CIR is obtained, the values and indexes of the maximum two impulses are sent to MPIC block. While the payload field, the MPIC subtracts the second path for interference cancellation. In each PCES field, the CIR is updated by Golay-MPIC TDE again based on Golay sequence aided channel estimation.

D. Performance Simulation and Analysis

The performance simulation of the proposed Golay-MPIC TDE in LOS channel is shown in Fig. 6. The performance requirement of coded BER is 10^{-6}, specified in 802.15.3c with $\pi/2$ QPSK modulation for SC and QPSK modulation for OFDM. According to the channel decoder implementation, the BER before channel decoded is set as 10^{-2}. With $\pi/2$ QPSK modulation in SC mode, the proposed Golay-MPIC TDE achieves the 10^{-2} BER at SNR of 8 dB. With QPSK modulation in OFDM mode, SNR at 10^{-2} BER is 6 dB. Apparently, the performance of OFDM (HSI) mode is better than SC mode, because the FFT has the effect of smoothing noise.

E. Architecture Design

The system architecture of the proposed Golay-MPIC TDE is illustrated in Fig. 7. The signal flow of SC mode is almost the same as that of OFDM mode. Only additional "Clockwise $\pi/2$ Phase Shifter" is used in SC mode since the modulation in SC mode is $\pi/2$ M-PSK.

In channel estimation, the optimized Golay correlator (OGC) [30] architecture is adopted to implement the Golay sequence aided channel estimation. Compared with the efficient Golay correlator employed in [15] and [16], OCG has less computational complexity while maintaining the same performance [31]. By using the characteristic of Golay sequence, the OGC is able to realize the same function as matched filter with less hardware cost. The number of stages for OGC is equivalent to $\log_2 N$,

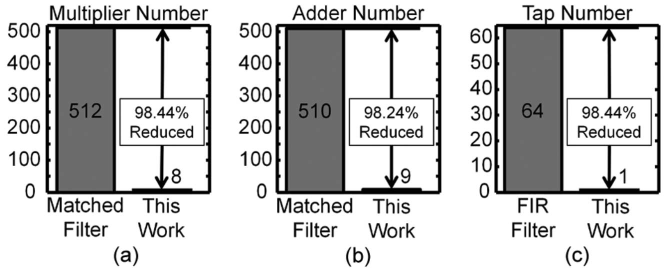

Fig. 8. Complexity improvement of (a) multiplication number of OGC, (b) addition number of OGC, and (c) tap number of equalizer of the proposed Golay-MPIC TDE.

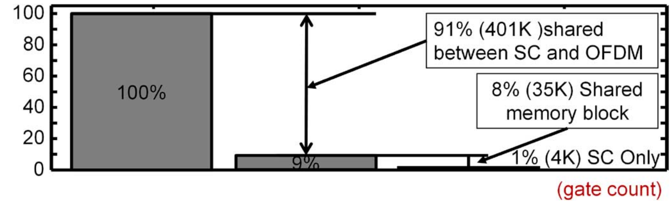

Fig. 9. Hardware reduction of the proposed Golay-MPIC TDE.

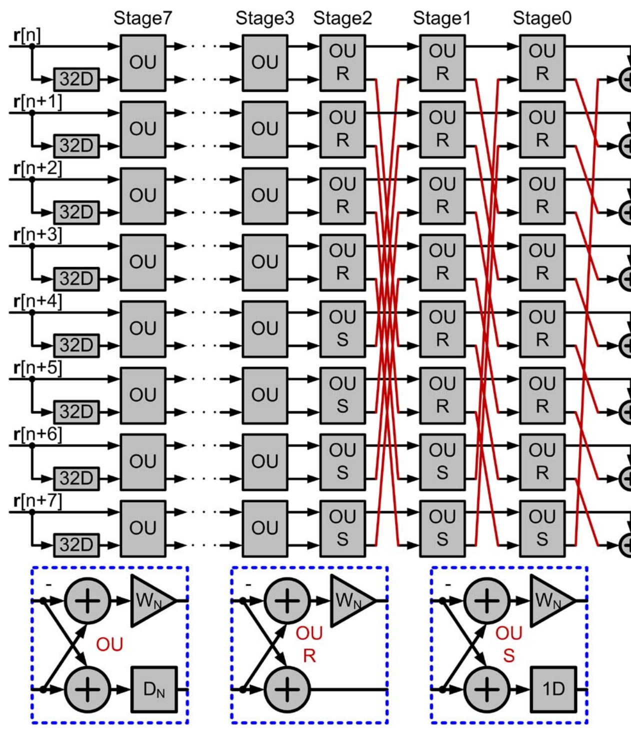

Fig. 10. 8X-parallelism architecture of OGC channel estimation.

where N is the length of specified Golay sequence 256. Therefore, there is 8-stage of OGC unit to perform the channel estimation. In hardware implementation, the multiplier "$\mathrm{W_N}$" can be simplified as bypass circuit or an inverter with the pre-defined Golay sequence. In addition to fulfill the requirement of OGC input, a length of 256 FIFO is implemented by two single port memory blocks from shared memory bank, with interleaved read and write accesses. The $\mathbf{a}_{256}$ with the 256 samples delay and $\mathbf{b}_{256}$ are concurrently sent to the OGC. The delay element "$\mathrm{D_N}$" in each OGC stage has the length of 2^{N} (128, 64, 32, 16, 8, 4, 2, and 1 for stage 7, 6, 5, 4, 3, 2, 1, and 0, respectively). During the CES and PCES fields, the CIR is acquired by the OGC channel estimation and then the indexes and values of two maximum estimated impulse responses are stored in register "h" as shown in Fig. 7. After the channel estimation procedure, the OGC channel estimation is shut down for power saving and the memory is released to other modules. As shown in Fig. 8, the OGC architecture can yield the reduction of multiplications and additions in 98.44% and 98.24%, respectively, as compared with straightforward matched filter approach.

By multiplying the conjugate of $\mathbf{h}[0]$ in (14), the denominator becomes a real number instead of complex number as following:

$$\begin{aligned}\mathbf{x}[i] &= \frac{\mathbf{r}[i]\times\mathbf{h}[0]* - \mathbf{x}_{\mathrm{ini}}[i-\tau]\times\mathbf{h}[\tau]\times\mathbf{h}[0]*}{\mathbf{h}[0]\times\mathbf{h}[0]*}\\ &= \frac{\mathbf{r}[i]\times\mathbf{h}[0]*}{|\mathbf{h}[0]|^2} - \frac{\mathbf{r}[i-\tau]\times\mathbf{h}[0]*}{|\mathbf{h}[0]|^2}\times\frac{\mathbf{h}[\tau]\times\mathbf{h}[0]*}{|\mathbf{h}[0]|^2}\\ &= \hat{\mathbf{r}}[i] - \hat{\mathbf{r}}[i-\tau]\times\frac{\mathbf{h}[\tau]\times\mathbf{h}[0]*}{|\mathbf{h}[0]|^2}\end{aligned} \tag{16}$$

It is clear that, the complex division in (14) is simplified as real division and complex multiplication. According to the pre-defined inversion look-up table (LUT), the real division can be implemented by a multiplier. The MPIC equalization as illustrated in Fig. 7 is employed to implement the (16). The "2nd Path Delay" block is a configurable delay-line to realize the τ delay.

According to the fixed-point analysis, the real- and imaginary-part of equalizer inputs are 9-bit. Therefore, the output of OGC is 18-bit after 9 additions. As a result, the memory size is $144 \times 16 \times 2$ $(\mathrm{bit} \times \mathrm{index} \times \mathrm{block})$ bits for 8X-parallesim. Then the input of absolute power circuit just takes the MSB 9-bit of OCG output and the output of absolute power circuit preserves 15-bit as the input of inversion LUT. The inversion LUT is pre-defined with the approximated resolution to reduce the table size and the output is 13-bit. Finally, the equalizer output is 15-bit for both real and imaginary parts.

The proposed equalizer is feed-forward architecture without feedback loop. Therefore, no additional memory is required to store the received data and it has more stable performance compared with using DFE. The memory is used as a FIFO, with length of 256, for channel estimation. The maximum size of the second path delay-line in MPIC block is 128 determined by the length of post zero-correlation zone.

The hardware reduction of proposed Golay-MPIC TDE is shown in Fig. 9. The hardware sharing parts excluding "Clockwise $\pi/2$ Phase Shifter" can obtain 99% hardware reduction. The gray parts as illustrated in Fig. 7 are jointing used in both SC and OFDM modes. The MEM Bank in OGC channel estimation is shared with the shared memory block in the baseband receiver. The FFT is not an overhead for the system since the FFT is employed to OFDM mode.

F. Architecture Parallelism Design and Synthesis Results

The 8X-parallelism architecture of OGC channel estimation is illustrated in Fig. 10. The "32D" and "1D" represent 32- and 1-sample delay, respectively. Due to processing 8 data at the same time, the arithmatic units are duplicated by 8 times and the length of delay elements are reduced 8 times. As a result, from stage 2 to stage 0, the delay elements are 1/2, 1/4, and 1/8, respectively. The non-integer delay elements can be implemented with the red wire routing as shown in Fig. 10. For stage 2, the bottom 4 OGC units have 1-sample delay used to realize 4-sample delay. For stage 1 and 0, the bottom 2 and last OGC units employ 1-sample delay to realize these delays.

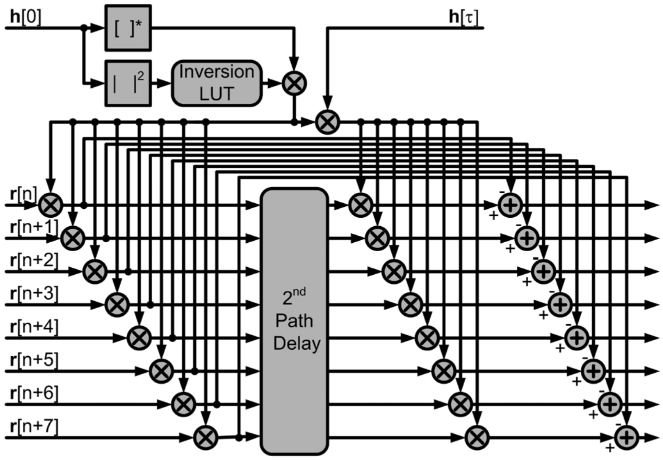

Fig. 11. 8X-parallelism architecture of MPIC equalization.

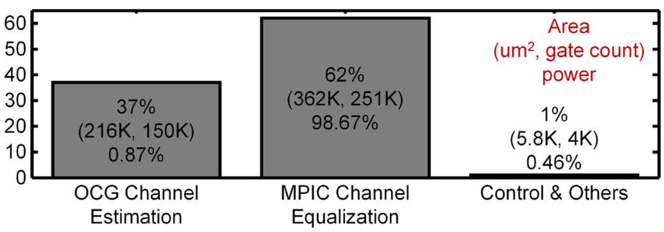

Fig. 12. Area and power breakdown of the proposed Golay-MPIC TDE.

TABLE II
GOLAY-MPIC TDE FOR SC AND OFDM MODE SYNTHESIS RESULT

	Golay-MPIC TDE
Processing	65nm CMOS GP process
Max clock rate	413 MHz
Area (gate count)	584,070 um^2 (405K)
Power (mW)	66.48 mW@220 MHz, SC mode 99.73 mW@330 MHz, OFDM mode 120.88 mW@400 MHz

* The result is synthesized with baseband receiver and excludes the memory bank shared from the shared memory block.

The 8X-parallelism architecture of MPIC equalization is illustrated in Fig. 11. As shown in (16), $\mathbf{h}[0]^*/|\mathbf{h}[0]|^2$ is a common term and can be calculated during the channel estimation period. After the channel estimation, the $\mathbf{h}[0]$ and $\mathbf{h}[\tau]$ are two fixed parameters. Therefore, the MPIC only requires a single hardware instead of 8 duplicates for the common term. The "2nd Path Delay" block is implemented with 8X-parallelism FIFO with 17 samples delay-line and switches. According to the value of τ, the switch selects the corresponding delay data for output.

Synthesis result (together with digital baseband receiver chip) shows the proposed Golay-MPIC TDE can achieve maximum 413 MHz operating clock rate (required clock rate is 330 MHz) by using 65 nm 1P9M CMOS general purpose process. The area of Golay-MPIC TDE is about 584K um^2 (405 K gate count) and the power consumption is 120.88 mW as shown in Table II. Furthermore, The area and power breakdown of proposed Golay-MPIC TDE is illustrated in Fig. 12. The OGC channel estimation, the MPIC equalization and the rests occupy 37%, 62%, and 1% of area, respectively. Besides, the one-shot OGC channel estimation is shut down after CIR estimation and then takes less than 1% of the working power. The MPIC equalization executes in each cycle and takes most of the power consumption.

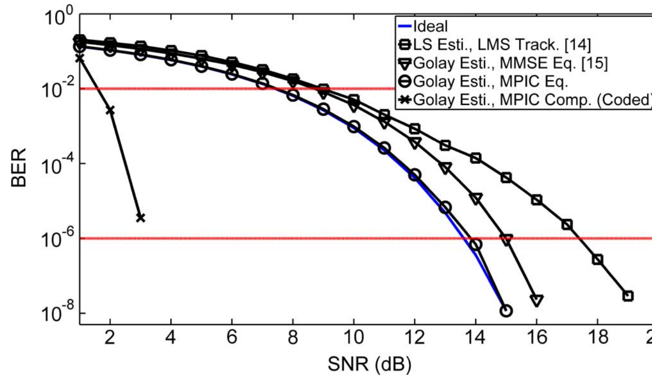

Fig. 13. Performance comparison of SC mode, with $\pi/2$ QPSK modulation in LOS channel.

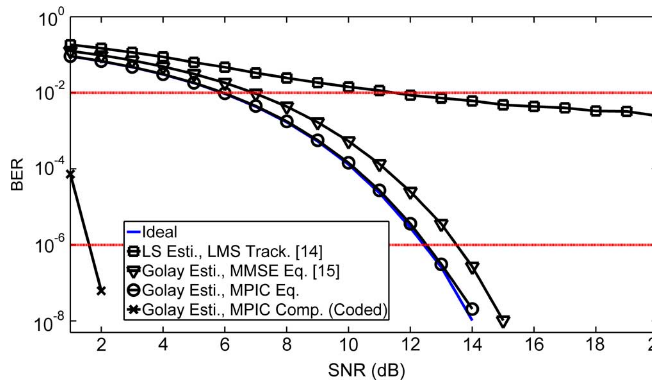

Fig. 14. Performance comparison of OFDM (HSI) mode, with QPSK modulation in LOS channel.

G. Comparison of Performance Simulation

The performance comparisons of different estimation and equalization algorithms in LOS channel are illustrated in Figs. 13 and 14. The performance comparison of SC and OFDM modes are with the modulation schemes $\pi/2$ QPSK and QPSK, respectively. The LS-LMS FDE [14], where is the least-square algorithm for channel estimation and the least-mean square algorithm for channel tracking. The time domain Golay correlator based channel estimation with frequency domain minimum mean-square error (MMSE) equalization (Golay-MMSE) [15] is also illustrated in Figs. 13 and 14. The Golay-MMSE transforms the estimated CIR in time domain to CFR in the frequency domain and induces the MMSE equalization to eliminate the noise effect to enhance the system performance. The ideal curve, obtained by the de-convolution between the ideal CIR and received signal, is used to be a performance reference.

It is clear that the proposed Golay-MPIC TDE has quite the same performance with the ideal case in both SC and OFDM modes. The LS-LMS FDE in SC mode has better performance than that of OFDM mode as expected in [32]. However, the LS channel estimation inherently has the noise enhancement problem. As a result, the initial errors are passed to the succeeding LMS tracking stage, and degrade system performance. Besides, a very small inaccuracy in CIR leads to serious CFR damage after transform the CIR to CFR. Therefore, the Golay-MMSE suffers the performance loss in this situation and has about 1.5 dB to 2 dB performance lost compared with the ideal case. The performance after channel decoding with coding rate 1/2 (762,336) shown that the proposed Golay-MPIC can achieve

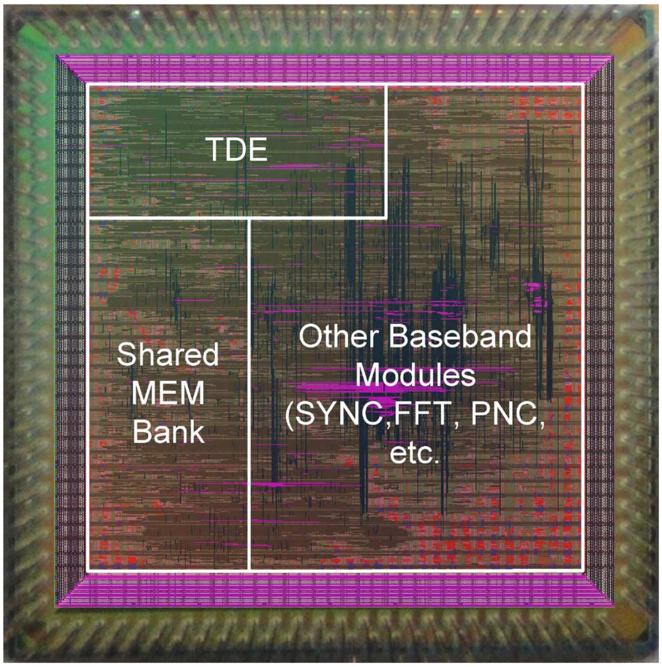

Fig. 15. Fabricated die and layout photo of Golay-MPIC TDE.

the required 10^{-6} BER below 4 dB in SC mode and 2 dB in OFDM mode.

IV. Implementation and Measurement Result

The proposed Golay-MPIC TDE structure is fabricated with standard cell-based design flow using 65 nm 1P9M general purpose process. The design was taped out as a part of the digital baseband receiver, including all-digital synchronization, FFT, phase noise cancellation (PNC), data demodulation and shared memory bank. The structure of digital baseband receiver is designed as 8X-parallesim with feed-forward data path. The proposed Golay-MPIC TDE not only estimates the CIR and equalizes the channel effect, but also perform the fine-boundary detection using the OGC output with the characteristic of Golay sequences. The TDE also removes the common phase rotation, which cannot be eliminated by time domain carrier frequency offset (CFO) de-rotator.

The die and layout photos of digital baseband receiver are shown in Fig. 15. The TDE is located in the upper-left corner. The phase de-rotator module of CFO compensation is placed in the right hand side and sends the phase de-rotated signals to the TDE. The shared memory bank is located in the lower left-corner near the TDE for the purpose of memory sharing. The TDE output goes through the center of the chip to PNC and data demodulation. Considering the restriction of area and pad number, in the fabricated chip, the demapper is for $\pi/2$ QPSK and QPSK for SC and OFDM modes, respectively. Thus, the output of demapper takes 16 pins (2×8) instead of 48 pins (6-bit for 64-QAM with 8X-parallelism).

The area of Golay-MPIC TDE is about 1.05 mm^2. The chip functionality is verified by Agilent 93000 SOC Series Test System, provided by National Chip Implementation Center (CIC). The measurement result shows that the proposed baseband receiver design can operate at the clock rate 220 MHz@1 V for SC mode and 330 MHz@1.1 V for OFDM (HSI) mode. The power consumptions for SC and OFDM modes are 56.71 mW and 91.29 mW, respectively. With 16-QAM demodulation, the data rate of SC mode can reach 7.04 Gb/s. Furthermore, the data rate of OFDM mode can achieve 15.84 Gb/s with 64-QAM demodulation.

The performances of several digital equalizers of 60 GHz band are illustrated in Table III. Comparing to the other designs, the proposed Golay-MPIC TDE can fully support the modulation schemes of 802.15.3c standard. The LS-LMS FDE [14], Golay-MMSE [15] and Golay-DFE [16] can provide QPSK modulation, 16-QAM and BPSK, respectively. For the Golay-DFE [16], the hardware complexity will significantly increase while supporting high-order QAM modulations. Besides, the Golay-DFE only supports the SC transmission.

The structure of the proposed Golay-MPIC TDE has no stability issue while LS-LMS FDE and Golay-DFE have the problem of error propagation. The LS-LMS FDE and Golay-MMSE require additional IFFT for SC mode to transform the equalized data in the frequency domain back to time domain. For LS-LMS FDE, another additional FFT is required to transform the error estimated by LMS tracking to frequency domain. In contrast, the proposed Golay-MPIC TDE does not need the additional FFT or IFFT for supporting both SC and OFDM modes.

Considering the large attenuation caused by atmospheric absorption and reflection, either the multi-antenna beamforming or the single directional antenna is more practicable than the single Omni antenna in 60 GHz environment. From the RF frond-end point of view, a multi-antenna scheme intuitively increases the number of antenna and mixer. On the other hand, from the aspect of transmitter and receiver, the complexity of PAs and ADCs, which are the most challenging modules, can be relaxed by taking the advantage of beamforming. The multipath delay spread is also significantly shortened by using the beamforming technique [1]. Since the Omni antenna apparently requires more taps and more complex ADC and PA, the overall system overhead is significant. As a result, a single directional antenna or a multi-antenna beamforming LOS system still has less hardware cost as compared with that of the NLOS system with Omni antenna. Moreover, the multi-antenna beamforming overhead can be neglected because it is specified in the standards.

Although this proposed Golay-MPIC TDE is implemented for QPSK due to the shuttle area limitation, the measurement result shows the design is able to achieve the required sampling rate, 1.76 GHz for SC and 2.64 GHz for OFDM, as specified in IEEE 802.15.3c. The gate count of 8X-parallism architecture has a little larger than 4X-parallel Golay-MMSE but it has the potential to achieve higher sampling rate. From the power dissipation point of view, the measured power dissipation of proposed Golay-MPIC TDE is superior to LS-LMS FDE and Golay-MMSE for LOS channel case. Cascading with the full mode demapper, the proposed Golay-MPIC TDE is able to achieve the maximum throughput 7.04 Gb/s and 15.84 Gb/s for SC mode with 16-QAM and OFDM mode with 64 QAM modulation, respectively. The power over throughput is illustrated in the table. In summary, the proposed Golay-MPIC TDE supports full modulation modes in 802.15.3c standard, achieves the maximum data rate of 15.84 Gb/s.

V. Conclusion

In this paper, a cost efficient digital equalizer is proposed for digital baseband of 60 GHz RF systems. The low complexity with high accuracy Golay-MPIC TDE is designed for LOS channel (which is the quite common channel situation in 60

TABLE III
CHIP MEASUREMENT COMPARISON

	Golay-MPIC TDE	**LS-LMS FDE [14]**	**Golay-MMSE [15]**	**Golay-DFE [16]**
Implementation type	Fabricated	Synthesis	Fabricated	Fabricated
Support mode	SC and OFDM	SC and OFDM	SC and OFDM	SC
Support modulations	π/2 QPSK, QPSK (π/2 BPSK, π/2 8-PSK, π/2 16-QAM, 16-QAM, 64-QAM)	π/2 QPSK, QPSK	BPSK, QPSK, 16QAM	BPSK
Support channel	LOS(*a)	LOS/NLOS	LOS/NLOS	LOS/NLOS
EQ structure	Golay Estimator, 1 tap MPIC	LS, LMS	Golay Estimator, MMSE	Golay Estimator, 38 taps DFE
Process	65 nm	65 nm	65 nm	65 nm
Core area	1.05 $mm^{2(*b)}$	N/A	1.12 $mm^{2(*c)}$	2.34 mm^2
Gate count	405K	1723K	382K(*d)	N/A
Max sampling rate	2.64 GHz	3.3 GHz	1.76 GHz	2.8 GHz
Power	SC: 56.71 mW@1 V, 220 MHz(*e) OFDM: 91.29 mW@1.1 V, 330 MHz(*e)	211 mW@1.08 V, 400 MHz	SC: 208 mW@1.2 V,440 MHz OFDM: 148 mW@1.2 V, 440 MHz	SC: 3.3 mW+5.6 mW OFDM: N/A
Throughput	SC: 3.52 Gb/s@220 MHz, 1 V, π/2 QPSK (Max: 7.04 Gb/s for 16-QAM) OFDM: 5.28 Gb/s@330 MHz, 1.1 V, QPSK (Max: 15.84 Gb/s for 64-QAM)	6.4 Gb/s@400 MHz, 1.08 V, QPSK	5.84 Gb/s@365 MHz, 1 V, 16QAM 7 Gb/s@440 MHz, 1.2 V, 16QAM	SC: 2.8 Gb/s@770 MHz, 1V, BPSK OFDM: N/A
Power/Data rate (mW/Gb)	SC: 16.11 (8.06 for 16-QAM) OFDM: 17.28 (5.76 for 64-QAM)	32.97	SC: 35.62 OFDM: 21.14	SC: 3.18 OFDM: N/A

*a: Able to support NLOS channel with extension of the taps of MPIC.

*b: Proportional to the chip area breakdown with core area.

*c: Including test circuits and FFT/IFFT.

*d: Including an additional IFFT.

*e: Proportional to the chip power breakdown.

GHz band transmission). The design is examined using the specification of IEEE 802.15.3c. The proposed Golay-MPIC TDE employs Golay sequence aided channel estimation with simplified MPIC equalization. The MPIC algorithm is modified as single-tap to reduce the computational complexity for the purpose to replace the conventional TDE.

From the hardware design point of view, the proposed LOS Golay-MPIC TDE equalizer is fulfilled to operate between SC and OFDM dual modes with 99% hardware sharing. In order to achieve the target of 2.64 GS/s symbol rate, the architecture is realized as feed-forward data path, for easily pipeline insertion, with 8X-parallelism.

The performance simulation indicates that the proposed Golay-MPIC TDE has superior performance in LOS channel compared with other FDE methods at 60 GHz band. The Golay-MPIC TDE can reach the required coded BER of 10^{-6} below 4 dB in SC mode and 2 dB in OFDM mode.

Finally, the design is fabricated as a part of digital baseband receiver. The fabricated area of proposed Golay-MPIC TDE is 1.05 mm^2. The measured power dissipations at SC and OFDM modes are 56.71 mW@220 MHz (1 V) and 91.29 mW@330 MHz (1.1 V), respectively. The maximum throughput can achieve 15.84 Gb/s (2.64 GS/s with 64-QAM modulation).

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