Power-Rail ESD Clamp Circuit With Diode-String ESD Detection to Overcome the Gate Leakage Current in a 40-nm CMOS Process

Federico Agustin Altolaguirre and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— A new silicon controlled rectifier-based power-rail electrostatic discharge (ESD) clamp circuit was proposed with a novel trigger circuit that has very low leakage current in a small layout area for implementation. This circuit was successfully verified in a 40-nm CMOS process by using only low-voltage devices. The novel trigger circuit uses a diode-string based level-sensing ESD detection circuit, but not using MOS capacitor, which has very large leakage current. Moreover, the leakage current on the ESD detection circuit is further reduced, adding a diode in series with the trigger transistor. By combining these two techniques, the total silicon area of the power-rail ESD clamp circuit can be reduced three times, whereas the leakage current is three orders of magnitude smaller than that of the traditional design.**

***Index Terms*— Electrostatic discharge (ESD), gate leakage, power-rail clamp circuit, silicon controlled rectifier (SCR).**

I. Introduction

ELECTROSTATIC discharge (ESD) has become a major reliability concern in IC industry [1]. ESD consist of high voltages and large currents discharges as the result of charge balance between bodies. Such kind of discharges can damage the internal devices of the ICs. To protect the ICs from ESD damage, some on-chip ESD protections have to be added into silicon chip and placed around the I/O periphery. These ESD protections detect ESD stresses and discharge them through safe paths, thus avoiding ESD damage. The typical whole-chip ESD protection scheme with active power-rail ESD clamp circuit [2] is shown in Fig. 1, which has been widely used in the modern IC products, and also included in the foundries I/O cell libraries. With such ESD protection scheme, the active power-rail ESD clamp circuit plays an important role to effectively conduct ESD current away from the IC without causing ESD damage on the internal circuits.

With the continuous shrink in the CMOS technology, the gate oxide thickness has been scaled down to less than 2 nm.

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F. A. Altolaguirre is with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan.

M.-D. Ker is with the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the Department of Electronics, I-Shou University, Kaohsiung 610054, Taiwan (e-mail: mdker@ieee.org).

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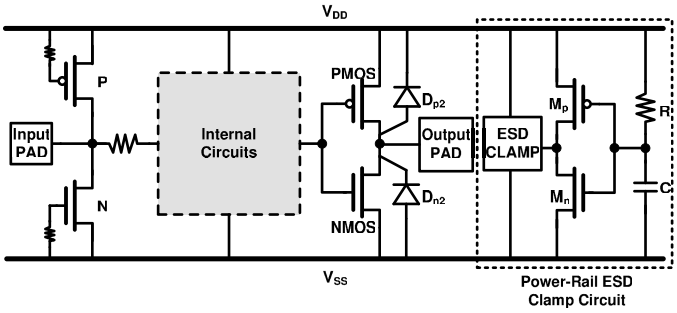


Fig. 1. Whole-chip ESD protection scheme realized with the active power-rail ESD clamp circuit.

TABLE I
GATE LEAKAGE CURRENT ON MOS CAPACITORS

Generation	MOS Type	t_{ox}	Gate leakage current at 1V (W/L = $1\mu m/1\mu m$)
90-nm	NMOS	∼2.3nm	∼11nA
	PMOS	∼2.5nm	∼3nA
65-nm	NMOS	∼2.0nm	∼140nA
	PMOS	∼2.2nm	∼80nA
40-nm	NMOS	∼1.9nm	∼260nA
	PMOS	∼2.1nm	∼95nA

With such a thin oxide, the gate leakage current [3]–[5] impacts drastically in the CMOS circuits, and it has to be accounted during design phase [6], [7]. The gate leakage current has been modeled and included in the BSIM4 SPICE model [8]. Although the high-K materials and metal gate alleviate the gate leakage effect [9], [10], these materials have not been included in the 90-, 65-, and 40-nm CMOS processes. A comparison of the leakage current among these processes can be found in Table I.

The gate leakage issue impacts drastically in the traditional ESD detection circuit, whereas a large MOSFET is used as a capacitor for ESD transient detection. The gate leakage through this MOSFET becomes unacceptable, especially for low-power designs. Previous works have explored different solutions to the leakage issue [11]–[16]. In [11], the leaky MOSFET capacitor is replaced by a metal-over-metal (MOM) capacitor to reduce the leakage current, at the expense of area overhead. In [12], stacked diodes are used to reduce the voltage

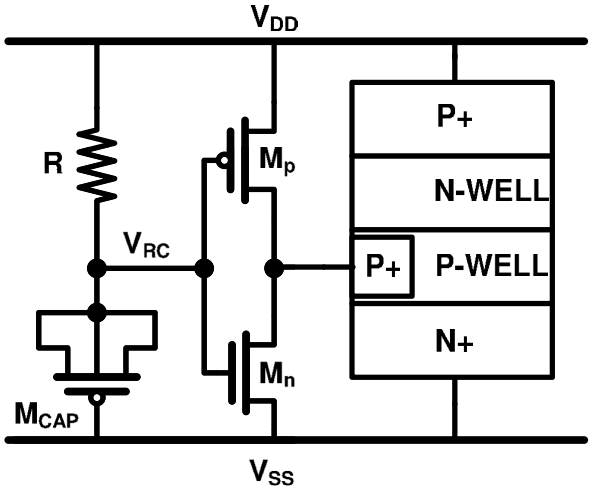


Fig. 2. Traditional power-rail ESD clamp circuit, where an SCR is used as the main ESD clamp device.

drop across the capacitor to reduce the gate leakage current. Previous works [13], [14] are similar in concept to [12], with the difference that they use feedback to detect whether the circuit is under normal circuit operation or ESD stress and control the capacitor voltage drop accordingly. In [15] and [16], parasitic capacitances are used to create the RC transient detection circuit, thus avoiding explicit capacitors and therefore reducing both area and leakage. Other high-voltage tolerant power-rail ESD clamp circuits reported to solve the gate oxide reliability issue in the ESD protection circuit [17], [18]. However, those previous works did not consider the impact of the gate leakage current when those circuits were implemented in more advanced CMOS processes. With the exception of some previous works, area efficiency was not of main concern, and research focus was on reducing the gate leakage current at any price. But, in the 40-nm CMOS process, silicon area becomes more expensive, and therefore achieving small area is of main concern.

In this paper, a new power-rail ESD clamp circuit is proposed and successfully verified on a 40-nm CMOS process to overcome the leakage current issue while also maintaining very small silicon area. In addition, this paper uses a level-sensitive ESD detection circuit as opposed to the previous works [13]–[15], which used transient-sensitive ESD detection circuits. Level-sensitive ESD detection is fundamental for hot plug-in applications, where the $V_{\rm DD}$ may have very fast variations that can mis-trigger the ESD protection circuits. Moreover, the level-sensitive ESD detection circuit does not need capacitors, resulting in a very small implementation area.

II. Impact of Gate Leakage on the Traditional Power-Rail ESD Clamp Circuit

The traditional power-rail ESD clamp circuit (shown in Fig. 2) employs an RC delay to detect the fast transient nature of ESD. In the older CMOS technologies, the main ESD clamp device was typically a MOSFET. However, in 40-nm CMOS, it is not practical to use such a device due to the large leakage current. Instead, a silicon controlled rectifier (SCR) is used, as described with the device of P+/N-WELL/P-WELL/N+ in Fig. 2. Moreover, the SCR can offer the highest ESD robustness within the smallest silicon area [19]. Older technologies avoid the use of SCR because the holding voltage of SCR was less than the power supply voltage, thus making the SCR device very sensitive to latch-up issue. The transistor $M_{\rm CAP}$ as a capacitor, together with the resistor R, forms the ESD detection circuit to detect the transient waveform during the ESD events. The transistors M_p and M_n control the SCR trigger procedure.

TABLE II
Device Sizes for the Traditional Power-Rail ESD Clamp Circuit

Device	R	M_{CAP}	M_p	M_n
Size	$50k\Omega$	$20\mu m/20\mu m$	$100\mu m/100nm$	$1\mu m/100nm$

During a positive ESD stress zapping at $V_{\rm DD}$ (with $V_{\rm SS}$ grounded), the rising voltage is faster than the RC time constant formed by R and $M_{\rm CAP}$. Therefore, the node $V_{\rm RC}$ is initially kept at ~0 V. The voltage difference between $V_{\rm DD}$ and $V_{\rm RC}$ turns M_p on to trigger the SCR on, and the ESD current is safely discharged by the SCR. Under normal circuit operation with $V_{\rm DD}$ at the stable operating voltage, $V_{\rm RC}$ should be ideally equal to $V_{\rm DD}$. But, the high leakage current caused by $M_{\rm CAP}$ causes a voltage drop across R and therefore $V_{\rm RC}$ is lower than $V_{\rm DD}$. With a lower $V_{\rm RC}$ voltage level, more circuit leakage current will conduct through M_p and M_n to cause a high leakage situation in the traditional power-rail ESD clamp circuit. Such a leakage problem in the power-rail ESD clamp circuit must be solved in the IC products for low-power applications.

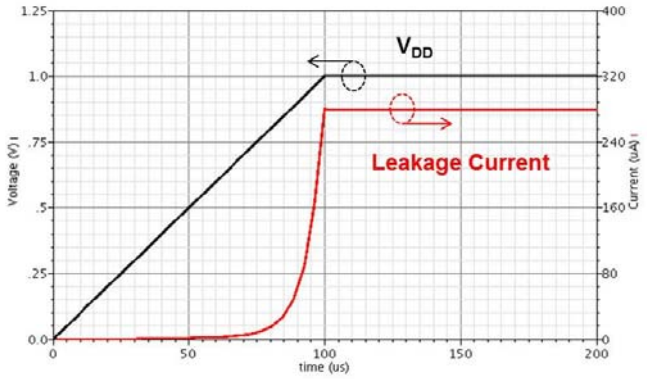
Fig. 3 shows the simulation results for the traditional power-rail ESD clamp circuit of Fig. 2, with device sizes as shown in Table II. To simulate the SCR substrate resistance, a 50 Ω resistor is placed between the trigger point and $V_{\rm SS}$. The simulated standby leakage current with 1 V bias and $T = 25$ °C is as large as 270 μA.

III. Proposed Power-Rail ESD Clamp Circuit

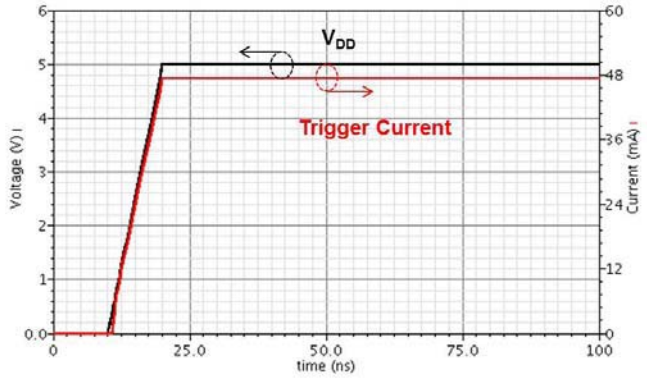
A. Low-Leakage and Small-Area ESD Detection Circuit

As it has been shown previously, the ESD detection circuit (R and $M_{\rm CAP}$ in Fig. 2) is the largest source of leakage current and also the source of area overhead. Therefore, the design of a more efficient ESD detection circuit is of main concern. The proposed circuit in this paper detects ESD transients by their high voltage level instead of the fast rise time. This can be implemented with a diode string and a resistor, as shown in Fig. 4, which will be referenced as design A.

The operation of this circuit is as follows: under normal circuit operation, the operating voltage is lower than the diode string threshold voltage ($V_{\rm th}$) and therefore there is no current flowing through R, and so M_p is turned off; under a positive-to-$V_{\rm SS}$ ESD stress, when the $V_{\rm DD}$ voltage overpasses $V_{\rm th}$ the diode string starts conducting some current that cause a voltage drop across R, thus turning M_p on to trigger the SCR.



(a)



(b)

Fig. 3. Simulation results on the traditional ESD clamp circuit in a 40-nm CMOS process under (a) normal V_{DD} power-on transition with a rise time of 0.1 ms and (b) ESD-like stress condition at V_{DD} with a rise time of 10 ns (V_{SS} grounded).

The diodes are implemented as P+/N-well diodes. The diode string threshold voltage for m diodes is given by [20]–[22]

$$V_{\text{th}}(I) = mV_D(I) - nV_T \times \left[\frac{m(m-1)}{2}\right] \times \ln(\beta + 1) \tag{1}$$

$$V_D(I) = nV_T \times \ln\left(\frac{I}{AI_S}\right) \tag{2}$$

where I is the current flowing through the diode string, V_D is the diode forward turn-on voltage, V_T is the thermal voltage, n is an ideality factor, β is the gain of the parasitic vertical pnp transistor, I_S is the saturation current of the p-n junction, and A is the area of the p-n junction diode. Under high temperature, β increases and V_D decreases (V_D has a negative thermal coefficient). These two variations makes V_{th} in (1) to decrease with temperature. The number of diodes (m) in the diode string is then decided according to the operating voltage, selecting the lowest number of diodes so that V_{th} is higher than $V_{\text{DD}} + 10\%$ at the highest operating temperature. Too few diodes would cause large leakage currents and mistriggerings under certain PVT variations; and too many diodes would cause some extra leakage in the diode string and also an excessively high V_{th}, which may lead to ESD failure. For $V_{\text{DD}} = 1$ V and $T = 125$ °C, the value of m is chosen with the aid of SPICE simulations, and it is chosen to be 3 in a 40-nm CMOS process. The diodes are fabricated with a

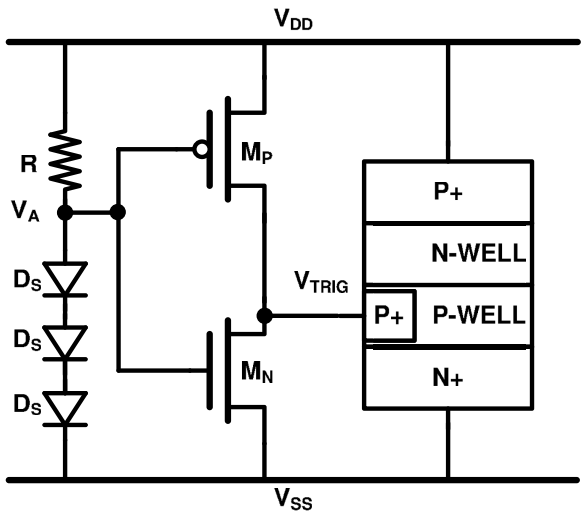


Fig. 4. Power-rail ESD clamp circuit using the diode-string based ESD detection circuit (design A).

minimum area of 1 μm^2 to keep the leakage current of the diode string to a minimum. The resistor R value has to be large enough to cause a significant voltage drop with the low current of the diode string but also small enough to avoid area overhead. The value of 5 kΩ offers a good compromise. According to simulations, the value of V_{th} varies between 1.8 and 2.6 V for temperatures varying from 25 °C to 125 °C. Fig. 5 shows the simulation results for the design A with device sizes as specified in Table III. The simulated leakage current with 1 V bias and $T = 25$ °C is only ~300 nA. The reduction of the leakage current compared with the traditional design is clearly evident.

B. Ultralow Leakage Power-Rail ESD Clamp Circuit

Even though the leakage current from the ESD detection circuit has been minimized, there is still a somehow large leakage current in the power-rail ESD clamp circuit. Observing the current paths in the simulations, it was noted that almost all the remaining leakage current is due to M_p. At low temperature, the main leakage mechanism is gate tunneling between the gate-drain overlap. At high temperature, the main leakage mechanism is junction leakage from bulk to drain. Both leakage mechanisms have a large dependency with the applied voltage. Therefore, adding a voltage drop between M_p drain and the SCR trigger point (V_{TRIG}) would reduce the leakage current by effectively reducing both V_{GD} and V_{BD}. Notice that this extra voltage drop would also reduce the SCR trigger current.

The first option is to add a resistor to cause the desired voltage drop. But due to the small leakage current, this resistor should be very large (in the order of kilo-ohms), which would cause an unacceptable voltage drop under ESD stress. The best option is clearly to use a diode (as shown in Fig. 6). Because of the exponential I–V characteristic, the output diode (D_O) voltage drop will be enough to reduce the leakage current without causing great impact on the SCR trigger current. The circuit shown in Fig. 6 will be referenced as design B.

Fig. 7 shows the simulation results for the design B with device sizes as specified in Table III. The simulated leakage

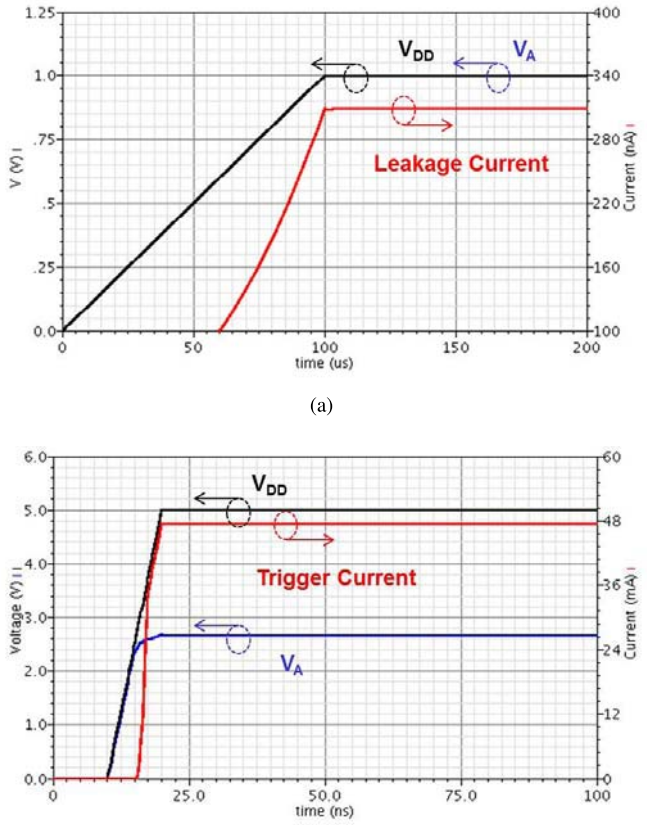


Fig. 5. Simulation results on the design A under (a) normal V_{DD} power-on transition with a rise time of 0.1 ms and (b) ESD-like stress condition at V_{DD} with a rise time of 10 ns (V_{SS} grounded).

TABLE III
DEVICE SIZES FOR THE PROPOSED POWER-RAIL ESD CLAMP CIRCUITS

Device	R	M_p	M_n	D_S	D_O
Size	$5k\Omega$	$100\mu m/100nm$	$1\mu m/100nm$	$1\mu m \times 1\mu m$	$20\mu m \times 1\mu m$

current with 1 V bias and $T = 25$ °C is as small as ~52 nA. The reduction of the leakage current compared with the design A is five times. Comparing Fig. 5(a) with Fig. 7(a), the reduction in the SCR trigger current caused by the addition of the output diode is ~ 20%.

IV. EXPERIMENTAL RESULTS

A test chip was fabricated in a 40-nm CMOS process, including several test circuits to prove in silicon. The SCR layout used in all the test circuits is the same as shown in Fig. 8, with 7-μm height and 40-μm width. Fig. 9 shows the test circuits microphotography using scanning electron microscopy (SEM).

The traditional power-rail ESD clamp circuit from Fig. 2, with device sizing as specified in Table II, and designs A (Fig. 4) and B (Fig. 6), with device sizing as specified in Table III, are included in the test chip. Also, design A is implemented with two, three, and four diodes in the diode string to compare leakage current and ESD behavior.

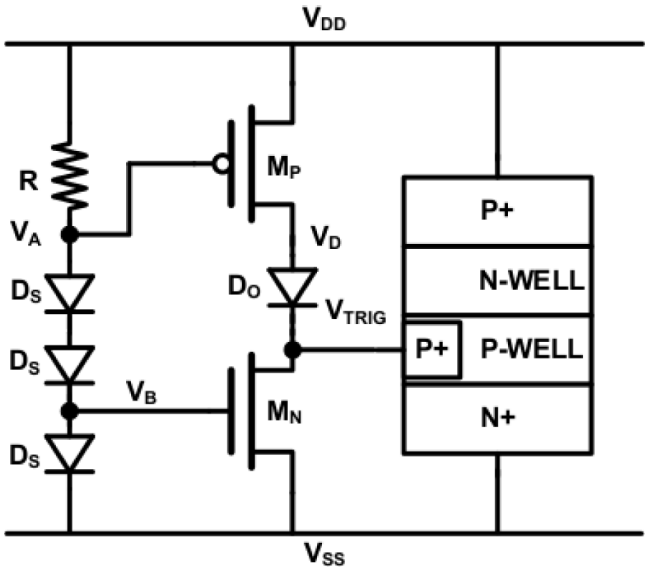


Fig. 6. Power-rail ESD clamp circuit using the diode-string based ESD detection circuit and the output diode (design B).

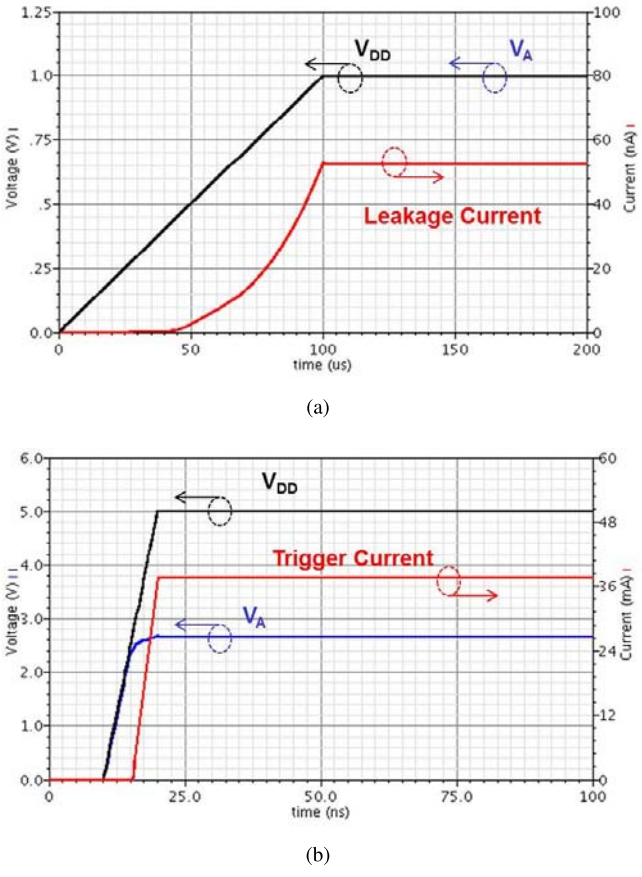


Fig. 7. Simulation results on the design B under (a) normal V_{DD} power-on transition with a rise time of 0.1 ms and (b) ESD-like stress condition at V_{DD} with a rise time of 10 ns (V_{SS} grounded).

A. Leakage Current

The leakage current is measured on-die with ultra-low leakage probes at controlled temperature. The traditional power-rail ESD clamp circuit leakage current at $T = 25$ °C with

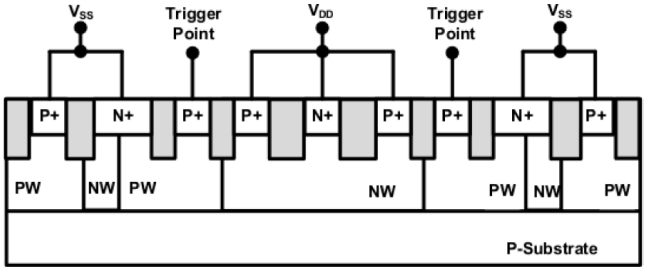
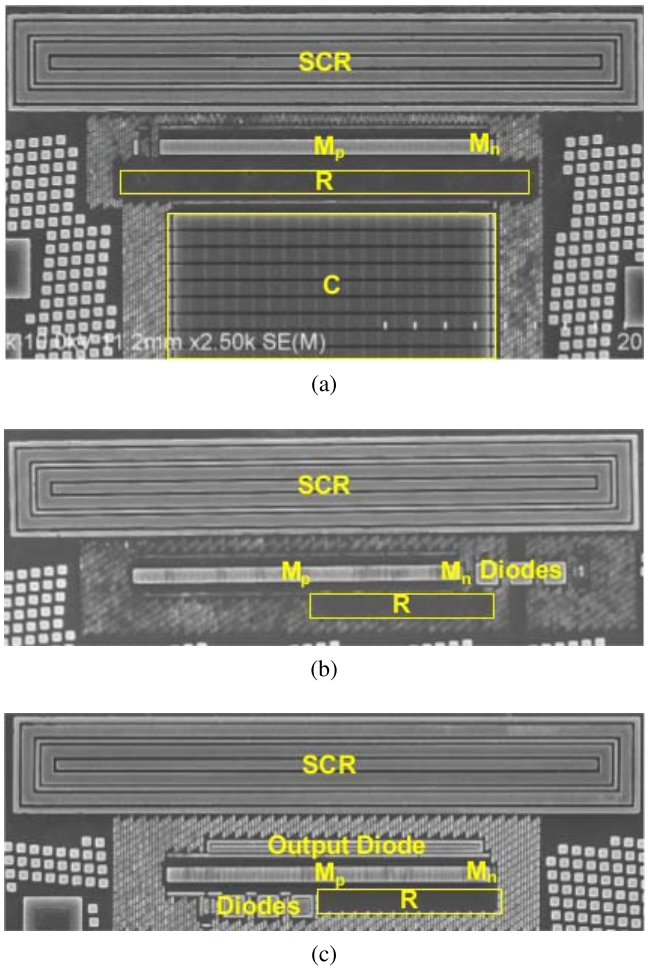


Fig. 8. Sectional cross-view of the SCR used in this paper. Gray areas: STI.

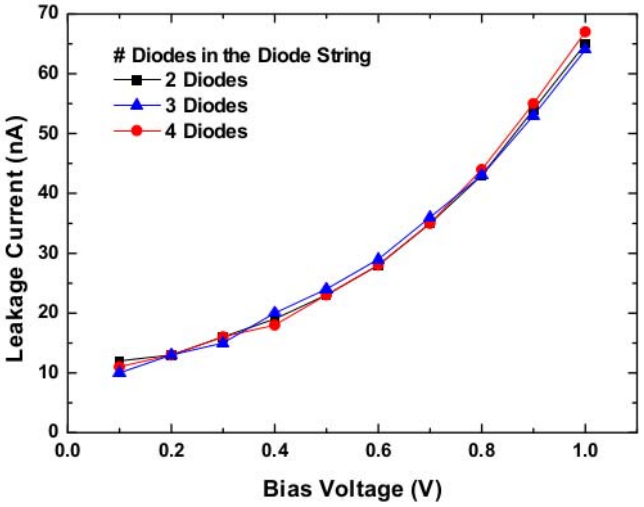


(a)

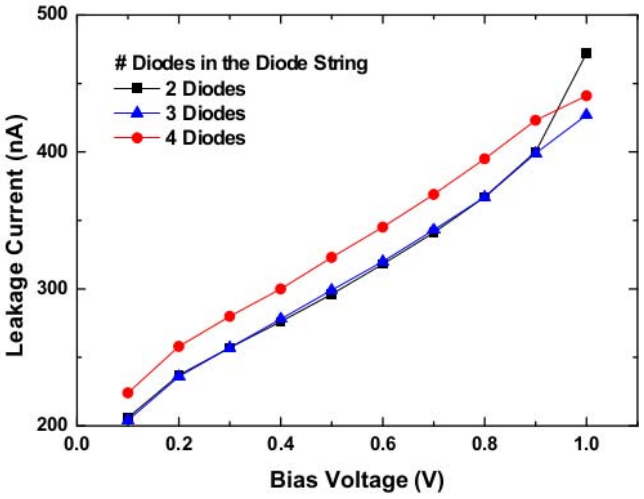
(b)

(c)

Fig. 9. SEM images of the fabricated power-rail ESD clamp circuits (after total delayer). (a) Traditional power-rail ESD clamp circuit. (b) design A. (c) design B.



(a)



(b)

Fig. 10. Leakage measurements for the design A with different numbers of diodes in the diode string, under different bias conditions and controlled temperature of (a) 25 °C and (b) 125 °C.

1 V bias is 13.6 μA, and 72 μA for $T = 125$ °C, also with 1 V bias.

Fig. 10 shows a comparison between different numbers of diodes in the diode string and their effect on the leakage current of the design A. Fig. 10(a) shows the leakage current measurements for $T = 25$ °C, and Fig. 10(b) shows the leakage current measurements for $T = 125$ °C. At low temperature, the leakage current is practically not affected by the number of diodes, and the overall leakage current is given by the gate leakage current of M_p. At high temperature, the effect of the diode string can be seen as the circuit with four diodes has effectively larger leakage current, with only an exception at 1 V bias, whereas the circuit with two diodes has larger leakage current due to the lower triggering point. These measurements confirm that three diodes is the best solution for minimizing the leakage current in the ESD detection circuit when standard supply voltage is used (0.9V $\pm$ 10% for the 40-nm CMOS process).

Fig. 11 shows a comparison between the fabricated power-rail ESD clamp circuits. The addition of the output diode shows a clear reduction in the leakage current of the power-rail ESD clamp circuit, especially for high temperatures. The leakage current of Design B presents a significant breakpoint around 0.5 V. This breakpoint is attributed to the extra voltage drop across the output diode, which reduces the bulk-drain voltage of M_p and therefore reduces the leakage current. The broken-like curve of the design B leakage current makes this circuit very useful for ultralow voltage applications, whereas supply voltages lower than 0.6 V could be usually used.

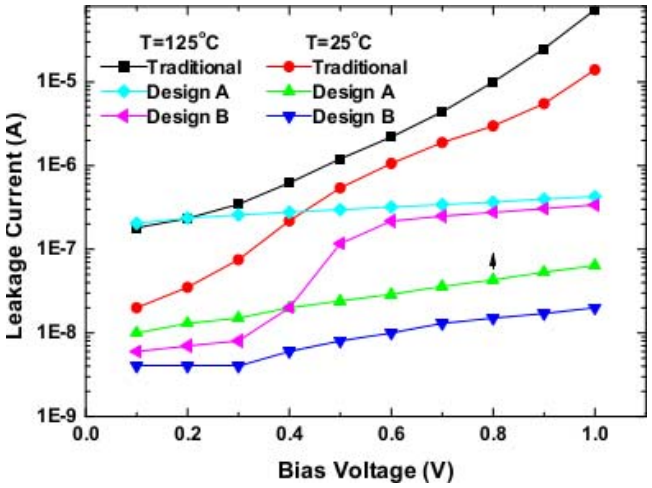


Fig. 11. Leakage current comparison between the fabricated power-rail ESD clamp circuits under different bias conditions and controlled temperatures.

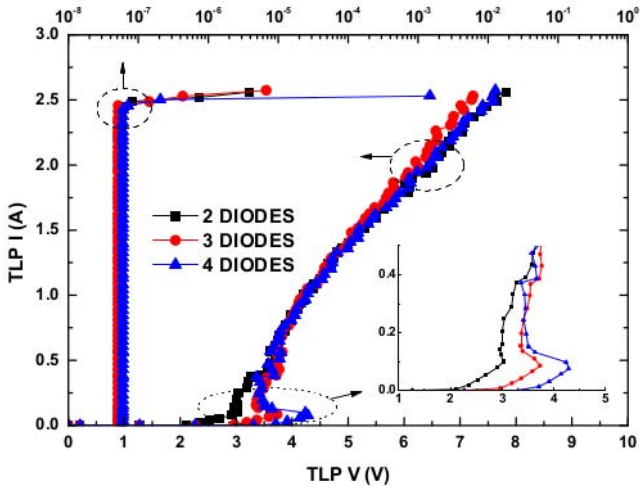


Fig. 12. TLP IV curves of the design A with different numbers of diodes in the diode-string based ESD detection circuit. The turning-point voltage V_{T1} is highlighted.

B. Transmission Line Pulsing

Transmission line pulsing (TLP) is an important ESD verification tool [23]. A TLP generator is used with pulse width of 100 ns and rise-time of 2 ns to investigate the turning point voltage (V_{T1}) and second breakdown current (I_{T2}).

The first TLP measurement concerns the effect of different numbers of diodes in the diode string based ESD detection circuit on the ESD performance. Fig. 12 shows the measurement results for the TLP IV curves of the design A with different numbers of diodes. The V_{T1} voltage is 3, 3.7, and 4.3 V for two, three, and four diodes, respectively. The gate oxide breakdown voltage for the 40-nm CMOS process is around 5 V. Therefore, these circuits can be effectively used to protect transistor gates. There is no significant variation in the I_{T2} among the circuits.

A comparison of the TLP IV curves among the traditional design and designs A and B is shown in Fig. 13. The V_{T1} voltage for designs A and B is practically the same. There is, though, a significant difference with the traditional

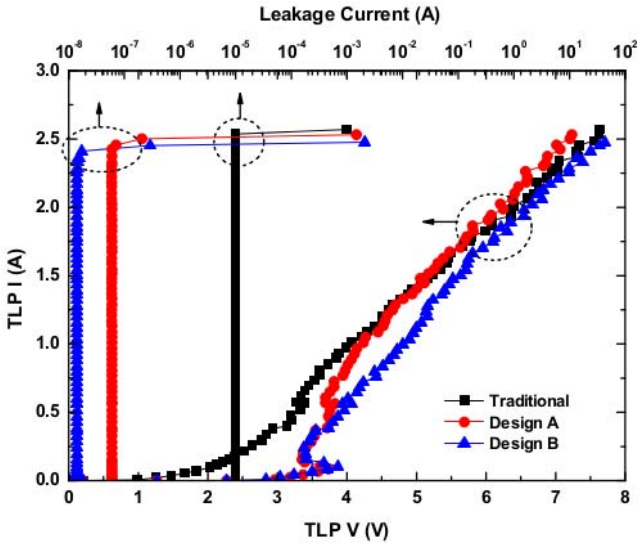


Fig. 13. TLP IV curves of the fabricated power-rail ESD clamp circuits.

power-rail ESD clamp circuit, which does not exhibit the breakpoint voltage. This is attributed to the higher leakage current flowing through the capacitor and the SCR trigger circuit, which also lowers the holding voltage for small currents. Notice that for TLP currents higher than 0.5 A the holding voltages are similar. The second breakdown current is ~2.5 A for all the circuits.

C. Turn-On Verification

Turn-on behavior of SCR-based ESD protection circuits is an important index for ESD protection [24]. To verify the turn-on speed, a 5 V pulse with 100-ns width and a rise time of 10 ns is applied to the device under test (DUT). Then, the transient waveform at the pad is observed to measure the turn-on speed. All the measured circuits performed the turn-on speed of ~10 ns. Some previous work has showed that the turn-on speed of SCR can be increased by blocking the STI formation inside the SCR [25].

D. ESD Robustness

In order to measure the ESD robustness of the circuits, the human body model (HBM) [26] and machine model (MM) [27] are used to stress the tested circuits and measure the failure voltages. The capacitor is charged to the high ESD voltage and then discharge to the DUT through the ESD resistance. After each discharge, the DC IV curve is measured and compared with the original curve. If there is a deviation higher than 30%, the DUT is considered damaged. The recorded ESD voltages are the maximum discharged voltages for which the DUT does not fail, i.e., the last voltage level before the failure voltage.

The traditional power-rail ESD clamp circuit fabricated in this paper can withstand 4.5-kV HBM and 200 V MM. The design A achieves the same ESD levels, disregarding the number of diodes in the ESD-detection circuit. The design B can withstand a higher HBM level of 6.5 kV whereas the MM level is also 200 V.

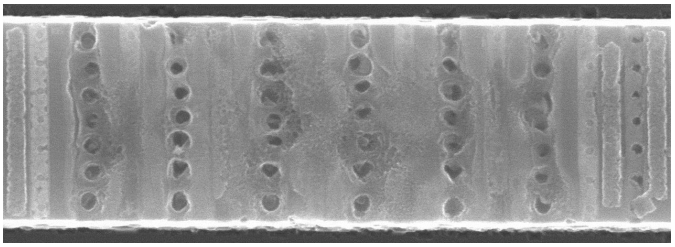


Fig. 14. Failure in the traditional power-rail ESD clamp circuit after 5-kV HBM ESD stress. The failure is located at M_p, but not on the SCR device.

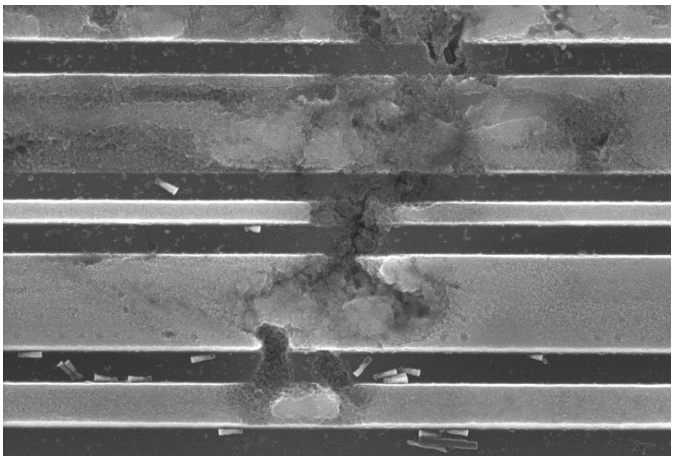


Fig. 15. Failure in the proposed power-rail ESD clamp circuit after 7-kV HBM ESD stress. The failure is located at the SCR device.

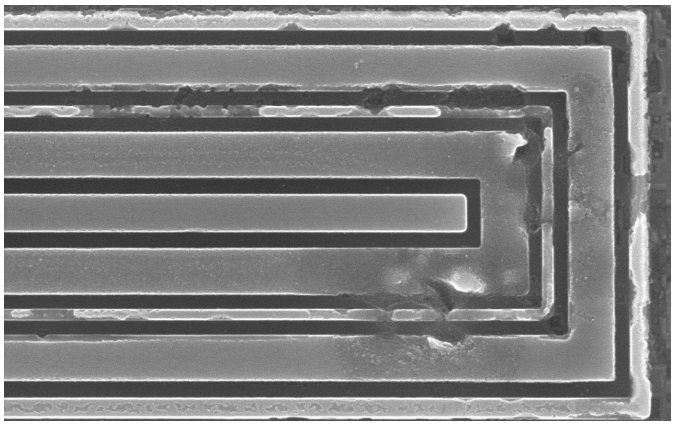


Fig. 16. Failure after 250 V MM ESD stress, which is located at the SCR device. The failure location on SCR is the same for all the tested circuits.

TABLE IV
COMPARISON AMONG THE POWER-RAIL ESD CLAMP CIRCUITS

Design	Leakage @ 1V bias		ESD Level	
	T=25°C	T=125°C	HBM	MM
Traditional	13.6μA	72μA	4.5kV	200V
Design A	62nA	425nA	4.5kV	200V
Design B	20nA	340nA	6.5kV	200V

Failure analysis (FA) is performed using SEM to find the failure point on the tested devices. After HBM/MM tests, the dies are delayered to expose the silicon and then are observed though SEM to find failures. Fig. 14 shows the damage observed on the traditional power-rail ESD clamp circuit after HBM stress. The damage is located on the trigger transistor (M_p). The same failure spot is observed on the design A. Fig. 15 shows the HBM failure for the design B. In this case, the damage is observed on the SCR. Fig. 16 shows a typical damage after MM stress. The failure spot is recurrent in all the tested circuits and it happens mostly on the SCR corners.

FA analysis show that the failure on the traditional power-rail ESD clamp circuit and design A is due to a high trigger current flowing through M_p. This could be solved by increasing M_p width, at the expense of adding more leakage current. On the other side, design B can withstand higher HBM voltages, and also the failure is located on the SCR and not on M_p. This is due to the fact that the output diode limits the trigger current to some extent, which still allows the SCR to turn-on correctly while keeping M_p safe from HBM damage.

MM failure is process and layout dependent. To increase the MM level, the SCR width should be increased, or use dummy gates [25]. Nonetheless, 200 V MM is the recommended level for the IC industry.

The overall performance of the realized circuits is summarized in Table IV.

V. DISCUSSIONS

There was noticed a large mismatch in the leakage current of the power-rail ESD clamp circuit between simulations and measurements. For example, the simulated leakage current of design A with $T = 25$ °C and 1 V bias was ~300 nA, whereas the measured leakage current (under the same bias conditions) for this circuit was of ~60 nA. After further simulations, it was noticed that the selection of corner process parameters (FF and SS libraries) can result in large difference on the simulated gate leakage currents, even more than 100% variation between simulations can be found. A total of five dies were measured, and the reported values in this paper are the most representatives.

In Section III, the output diode was discussed as an improvement on the leakage current of the power-rail ESD clamp circuit. More diodes in series could be added to the output diode to further reduce the leakage current, but the SCR trigger current would be drastically reduced, and the power-rail ESD clamp circuit may not be fully functional with such realization. To prove this, another test circuit was included implementing the design B with the same device sizes but using two output diodes instead of one. The measured leakage current with $T = 25$ °C and 1 V bias was ~1 nA, but the circuit failed at lower ESD stresses (both HBM and MM). On design phase, when trying to minimize the leakage current, the designer has to be always aware that correct functionality has to be preserved.

Figs. 12 and 13 show a somehow excessive voltage at high currents. The thin-oxide gate breakdown voltage for the used 40-nm CMOS process is ~6 V. If the SCR is used to protect a gate, it would be expected to fail at 6 V. The TLP current for 6 V is approximately 1.8 A, which gives more than 2.5-kV HBM ESD robustness. If higher ESD protection is needed,

the SCR width should be enlarged to satisfy the required low on-resistance.

VI. Conclusion

A novel power-rail ESD clamp circuit has been proposed and verified on silicon using a 40-nm CMOS process. The diode-string based ESD detection circuit can achieve accurate ESD detection while maintaining low silicon area and low leakage current. The number of diodes on the diode-string is determined according to the power-supply voltage, and it has to be maintained to a minimum. A larger number of diodes has been proved to increase leakage current, especially under high temperatures, and also increase the TLP turning point, thus decreasing the overall ESD performance.

The addition of the output diode further reduces the leakage current, and due to the diode characteristics, it makes the design especially suitable for ultralow-voltage applications. In addition, the output diode does not impact negatively on the ESD robustness. On the contrary, it increases the HBM level by protecting the trigger transistor (M_p).

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Federico Agustin Altolaguirre is currently pursuing the Ph.D. degree with National Chiao-Tung University, Hsinchu, Taiwan.

His current research interests include electrostatic discharge protection design and IO design.

Ming-Dou Ker (F'08) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1993.

He is currently the Distinguished Professor with the Department of Electronics Engineering, NCTU, and also as the Dean of the College of Photonics in NCTU.