Comparative Leakage Analysis of GeOI FinFET and Ge Bulk FinFET

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***Abstract*— We present a comparative leakage analysis of germanium-on-insulator (GeOI) FinFET and germanium on bulk substrate FinFET (Ge bulk FinFET) at device and circuit levels. Band-to-band tunneling (BTBT) leakage-induced bipolar effect is found to result in an amplified BTBT leakage for GeOI FinFET. Device and circuit designs to mitigate the amplified BTBT leakage of GeOI FinFETs are suggested. The effectiveness of various high threshold voltage technology options including increasing channel doping, increasing gate length and drain-side underlap for leakage reduction is analyzed.**

***Index Terms*— Band-to-band tunneling (BTBT) leakage, FinFET, germanium, germanium-on-insulator (GeOI).**

I. Introduction

FinFET has emerged as the prime candidate for extremely scaled MOSFETs due to its superior control of short-channel effects (SCEs) [1]–[3]. Germanium device offers high mobility [4]–[8]. However, due to its high permittivity and low bandgap, germanium device suffers from SCE and severe band-to-band tunneling (BTBT) leakage. Combining the advantages of the FinFET structure and the high mobility of Ge becomes a promising approach for future high-performance MOSFETs [9]–[12]. Si-on-insulator (SOI) FinFET and Si bulk FinFET have been studied [13]–[15], and the results showed that Si FinFET on bulk substrate with an optimized punch through stopper (PTS) doping [16] underneath the channel region can exhibit comparable performance and leakage with that on SOI substrate. However, a comparative leakage analysis between germanium-on-insulator (GeOI) FinFET and Ge bulk FinFET has rarely been seen.

In this work, the BTBT leakage current in the GeOI FinFET is shown to be amplified due to the bipolar effect, and various device design strategies for mitigating the bipolar gain (β) and leakage current of GeOI FinFETs are examined. This work is organized as follows. Section II describes the device design, simulation methodology, and device characteristics. Section III investigates the device and circuit designs to suppress the amplified BTBT leakage due to the BTBT-induced bipolar effect. Section IV is the conclusion.

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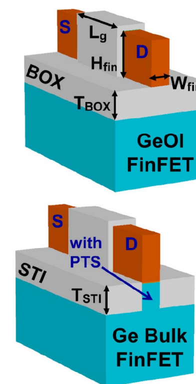

	GeOI FinFET	Ge Bulk FinFET
L_g (nm)	18	18
W_{fin} (nm)	7	7
H_{fin} (nm)	16	16
EOT (nm)	0.8	0.8
T_{BOX} (nm)	10	--
T_{STI} (nm)	--	10
N_{ch} (cm^{-3})	1e16	1e16
N_{SD} (cm^{-3})	5.5e19	5.5e19
N_{PTS} (cm^{-3})	--	5e17

Fig. 1. Schematic view of GeOI and Ge bulk FinFETs, and device parameters used in this work. For Ge bulk FinFET, the PTS doping (N_{PTS}) is adjusted to have comparable subthreshold swing compared with the GeOI FinFET.

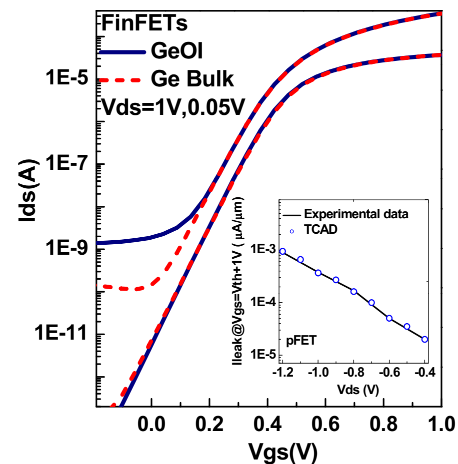

Fig. 2. I_{ds} versus V_{gs} characteristics of GeOI and Ge bulk FinFETs. Ge bulk FinFET uses PTS to control the subthreshold leakage. GeOI FinFET shows different I_{off} compared with the Ge bulk FinFET at $V_{ds} = 1$ V. Inset: BTBT leakage current calibration at various V_{ds} [19].

II. Device Design and TCAD Simulation Methodology

Fig. 1 shows the schematics of the GeOI and Ge bulk FinFETs and the device parameters used in this work. The PTS doping (N_{PTS}) of the Ge bulk FinFET is adjusted to have comparable subthreshold swing compared with the GeOI FinFET, as shown in Fig. 2.

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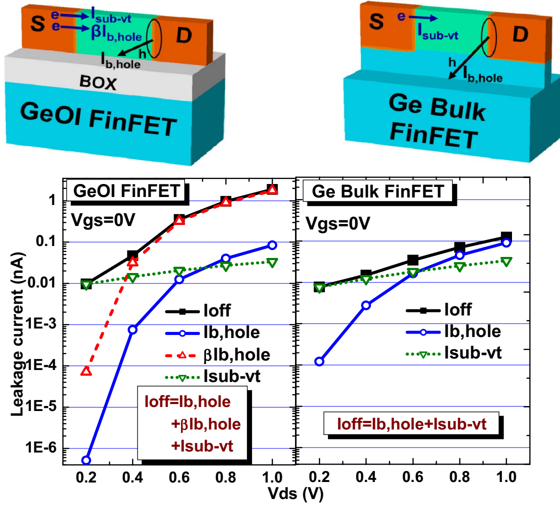

Fig. 3. Leakage components for GeOI FinFET and Ge bulk FinFET at various V_{ds}. The BTBT induced bipolar leakage ($\beta \times I_{b,\mathrm{hole}}$) is only observed in the GeOI FinFET.

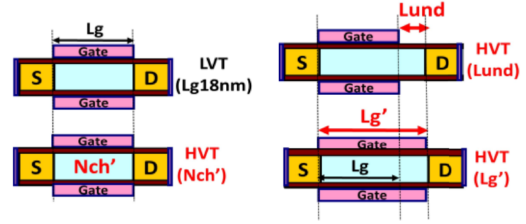

Fig. 4. Schematics of LVT, and HVT FinFETs options using drain-side underlap ($L_{\mathrm{und}} = 4$ nm), increasing channel doping ($N_{\mathrm{ch}'} = 2\mathrm{e}18\ \mathrm{cm}^{-3}$), and increasing gate length ($L_g' = 22$ nm).

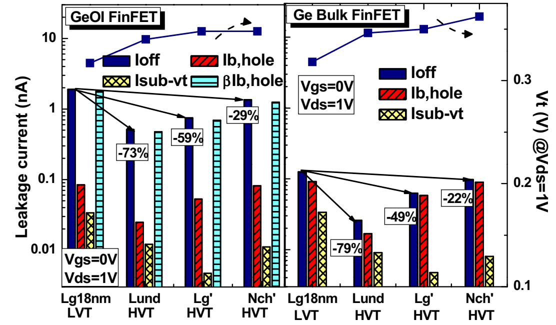

Fig. 5. Leakage comparisons of LVT and HVT FinFET options for GeOI and Ge bulk FinFETs at $V_{\mathrm{ds}} = 1$ V. For GeOI and Ge bulk FinFETs at $V_{\mathrm{ds}} = 1$ V, using HVT (L_{und}) is the most effective way to reduce I_{off}.

The BTBT model [17], [18] is calibrated with the experimental data at various V_{ds} in [19], as shown in the inset of Fig. 2. The bandgap widening due to quantum confinement is considered for the 7-nm fin width (W_{fin}) GeOI and Ge bulk FinFETs. The GeOI/Ge bulk FinFETs and circuits are analyzed using TCAD mixed-mode simulations [20].

Si bulk FinFET with optimized doping shows similar intrinsic device performance (I_{off} versus I_{on}) compared with the SOI FinFET at high and low V_{ds} [13], [14]. Fig. 2 shows that the GeOI FinFET exhibits comparable DIBL, subthreshold swing, and leakage at $V_{\mathrm{ds}} = 0.05$ V as compared with the Ge bulk FinFET with PTS. However, the leakage currents are different between the GeOI FinFET and the Ge bulk FinFET at $V_{\mathrm{ds}} = 1$ V.

Fig. 3 shows the leakage components for the GeOI FinFET and Ge bulk FinFET at $V_{\mathrm{gs}} = 0$ V and $V_{\mathrm{ds}} = 1$ V. The leakage components of the GeOI FinFETs include the BTBT hole current $\mathrm{I}_{\mathrm{b,hole}}$, the amplified BTBT current ($\beta \times I_{b,\mathrm{hole}}$) due to bipolar effect [21], and the subthreshold leakage current ($I_{\mathrm{sub-vt}}$), while the leakage components of Ge bulk FinFETs only include the BTBT hole current ($I_{b,\mathrm{hole}}$), and the subthreshold leakage current ($I_{\mathrm{sub-vt}}$).

For Ge bulk FinFET, as BTBT occurs, $I_{b,\mathrm{hole}}$ flows into the substrate contact and hole concentration in the channel is much lower than the GeOI FinFET. Therefore, the BTBT-induced bipolar effect is not observed in the Ge bulk FinFETs. The total leakage I_{off} for Ge bulk FinFET equals the sum of $I_{b,\mathrm{hole}}$ and $I_{\mathrm{sub-vt}}$. The leakage components of the GeOI FinFET and Ge bulk FinFET at various V_{ds} are shown in Fig. 3. The I_{off} of GeOI FinFET is dominated by the BTBT-induced bipolar current ($\beta \times I_{b,\mathrm{hole}}$) at $V_{\mathrm{ds}} > 0.4$ V. For Ge bulk FinFET, the I_{off} is dominated by the BTBT leakage $I_{b,\mathrm{hole}}$ at $V_{\mathrm{ds}} > 0.6$ V, and by the subthreshold leakage ($I_{\mathrm{sub-vt}}$) at $V_{\mathrm{ds}} < 0.6$ V. Therefore, the BTBT-induced bipolar leakage needs to be considered for GeOI FinFET when it is compared with the Ge bulk FinFET.

III. Mitigation of BTBT-Induced Bipolar Leakage in GeOI FinFETs

Power-performance optimization often requires devices with multiple threshold voltages (V_{t}) [22]–[24]. High threshold voltage (HVT) transistors are typically employed for non-critical paths to reduce the leakage, while low threshold voltage (LVT) transistors are used for the critical paths. Several kinds of device design can be used to achieve HVT transistors. Asymmetric gate-to-source/drain underlap devices have been used in the static random access memory (SRAM) cell to adjust the threshold voltages and improve the cell leakage and stability [25], [26]. Increasing gate length was used in a microprocessor design [27]. Increasing the channel doping increases the total depletion charge in the device channel, hence increasing the V_t. Fig. 4 shows the schematics of (LVT, $L_g = 18$ nm) and different HVT FinFETs options including drain-side underlap ($L_{\mathrm{und}} = 4$ nm), increasing channel doping ($N_{\mathrm{ch}}' = 2\mathrm{e}18\ \mathrm{cm}^{-3}$), and increasing gate length ($L_g' = 22$ nm). The effectiveness of the HVT options to suppress the BTBT-induced bipolar leakage in the GeOI FinFET is examined.

Fig. 5 shows the leakage comparisons of LVT and HVT FinFET options for the GeOI and Ge bulk FinFETs at $V_{\mathrm{ds}} = 1$ V. The leakage current of GeOI FinFET is dominated by the bipolar current ($\beta \times I_{b,\mathrm{hole}}$), and the leakage current of Ge bulk FinFET is dominated by the BTBT current $I_{b,\mathrm{hole}}$ at $V_{\mathrm{ds}} = 1$ V. For GeOI and Ge bulk FinFETs at $V_{\mathrm{ds}} = 1$ V, drain-side underlap [HVT (L_{und})] shows significantly larger reduction (73% and 79%) in I_{off} compared with the increasing gate length [HVT (L_g')] and increasing channel doping [HVT (N_{ch}')], as shown in Fig. 5. This is because as drain-side

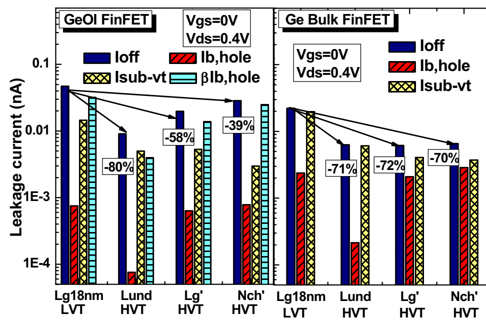

Fig. 6. Leakage comparisons of LVT and HVT FinFET options for GeOI and Ge bulk FinFETs at V_{ds} = 0.4 V. For GeOI FinFETs at V_{ds} = 0.4 V, using HVT (L_{und}) is the most effective way to reduce I_{off}, while for Ge bulk FinFET at V_{ds} = 0.4 V, using HVT (L_{und}), HVT (Lg'), and HVT (N'_{ch}) shows comparable reduction in I_{off}.

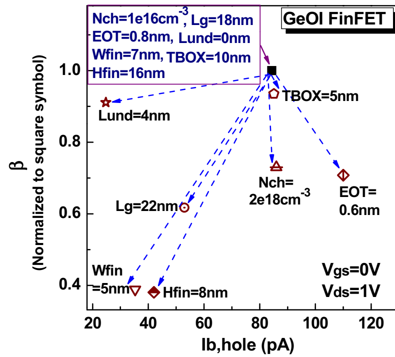

Fig. 7. Reducing W_{fin}, H_{fin}, and EOT, and increasing N_{ch} and L_g can be used to reduce the bipolar gain of BTBT in GeOI FinFET.

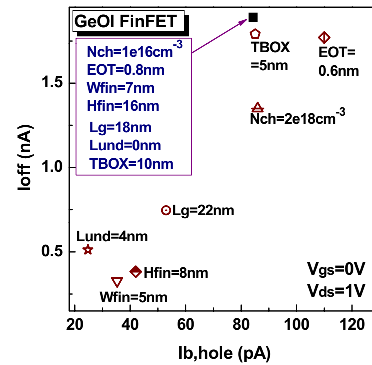

Fig. 8. Reducing T_{box} and EOT shows less reduction in the I_{off} of GeOI FinFETs.

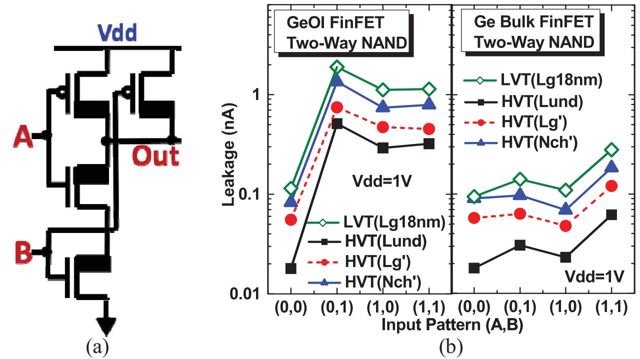

Fig. 9. (a) Schematic of HVT (L_{und}) two-way NAND. The underlap region is marked with thick line. (b) Leakage comparisons of two-way NAND with GeOI and Ge bulk FinFETs for various input patterns at V_{dd} = 1 V.

underlap length (L_{und}) increases, the BTBT width increases, thus reducing the $I_{b,hole}$ and bipolar current ($\beta \times I_{b,hole}$) for the Ge bulk and GeOI FinFETs. Using HVT (N'_{ch}) is the least effective way to reduce the I_{off} of the GeOI and Ge bulk FinFETs at V_{ds} = 1 V.

As V_{ds} scales down to 0.4 V (Fig. 6), the I_{off} of LVT GeOI FinFET is dominated by the bipolar current ($\beta \times I_{b,hole}$), therefore, using HVT (L_{und}) is the most effective to reduce I_{off}. On the other hand, for Ge bulk FinFET at V_{ds} = 0.4 V, using HVT (L_{und}), HVT (L'_g), and HVT (N'_{ch}) shows the comparable reduction in I_{off} because the I_{off} of Ge bulk FinFET is dominated by the subthreshold leakage (I_{sub-vt}), and I_{sub-vt} strongly depends on the threshold voltage. The effectiveness of using HVT (L_{und}), HVT (L'_g), and HVT (N'_{ch}) to reduce the leakage of the Ge bulk FinFET is different between V_{ds} = 1 V and V_{ds} = 0.4 V because the leakage of Ge bulk FinFET is dominated by the BTBT current at V_{ds} = 1 V and by the subthreshold leakage current at V_{ds} = 0.4 V.

Fig. 7 shows the impact of different device design on the bipolar gain (β) and the BTBT current $I_{b,hole}$ of GeOI FinFET. The bipolar gain of the GeOI FinFET can be effectively suppressed by reducing the fin width (W_{fin}), fin height (H_{fin}) and EOT, and increasing channel doping (N_{ch}) and gate length (L_g). Using drain-side underlap (L_{und}) and reducing buried oxide thickness (T_{BOX}) show smaller impact in reducing the bipolar gain. This is because the body potential can be well controlled by gate as W_{fin}, H_{fin} and EOT are reduced, thus reducing the bipolar gain. Although using L_{und} shows small impact on reducing the bipolar gain, the I_{off} of GeOI FinFET can be effectively reduced using L_{und}, because L_{und} significantly reduce the BTBT leakage $I_{b,hole}$ as shown in Fig. 8. Reducing T_{BOX} and EOT show less reduction in the I_{off} of GeOI FinFETs since the BTBT leakage cannot be effectively suppressed by T_{BOX} and EOT reduction.

The HVT options shown in Fig. 4 are used to reduce the leakage of GeOI FinFET and Ge bulk FinFET two-way NAND circuits, as shown in Fig. 9. The schematic view of HVT (L_{nud}) two-way NAND is shown in Fig. 9(a), where the underlap region is marked with black thick line. The underlap region is only placed at the drain junction, which has the significant band overlap and BTBT. Fig. 9(b) shows the GeOI FinFET and Ge bulk FinFET two-way NAND leakages with various input pattern at V_{dd} = 1 V. For input pattern (A,B) = (1,1), the leakage of GeOI FinFET two-way NAND is dominated by the BTBT-induced bipolar leakage ($\beta \times I_{b,hole}$) of two parallel off pFETs. For (A,B) = (0,0), the leakage of two-way NAND is dominated by the two stacked off nFETs, and the leakage of the GeOI FinFET two-way NAND with (A,B) = (0,0) is reduced by one order of magnitude compared with GeOI FinFET two-way NAND with (A,B) = (1,1). Therefore, the amplified BTBT leakage of GeOI FinFET can be suppressed by transistor stacking [28]. For GeOI and Ge bulk FinFETs two-way NAND, using HVT (L_{und}) shows lower leakage current than using HVT (L'_g) and HVT(N'_{ch}).

IV. CONCLUSION

The BTBT leakage triggered parasitic lateral bipolar effect needs to be considered for the GeOI FinFET. Using drain-side underlap is a more effective strategy to reduce leakage for GeOI and Ge bulk FinFETs compared with increasing gate length and channel doping. The bipolar gain of GeOI FinFETs can be suppressed by reducing the fin width, fin height and EOT, increasing channel doping and gate length, and by transistor stacking.

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