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Effect of nickel concentration on source/drain series resistance and channel resistance of Ni-metal-induced crystallization thin-film transistors

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ABSTRACT

The Ni-metal-induced crystallization (MIC) of amorphous Si (α-Si) has been employed to fabricate low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs). Most studies have focused only on reducing Ni contamination because Ni residues cause high leakage current in MIC–TFTs. Also of concern is the source/drain (S/D) series resistance, which degrades the device performance (driving ability) that might vary with the Ni concentration in MIC–TFTs. Improving the driving ability of MIC–TFTs requires a detailed understanding of how Ni residues affect S/D series resistance. This study investigates how Ni concentration affects S/D series resistance by using the transmission line method. The results of this study provide further insight into how Ni concentration and resistance are related. The results show that the S/D series resistance and channel resistance decreased with a reduction in Ni concentration in MIC poly-Si because of better crystalline quality and lower degradation of the donor concentration. This phenomenon was caused by the Ni concentration forming less $NiSi_2$ nucleation sites to generate a large grain size; Ni atoms serve as acceptor-like dopants in silicon, which counteract with the effects of n-type doping, subsequently reducing the donor concentration in the S/D region.

1. Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been widely applied to high-resolution integrated active-matrix organic light-emitting diodes, which exhibit good electrical properties and can be used to realize of glass substrates [1]. In various fabrications for LTPS, metal-induced crystallization (MIC) is promising for use because of its low cost, good uniformity, low crystallization temperature (approximately 500 °C) and short crystallization time (0.5 to 5 h) [2,3]. However, Ni and $NiSi_2$ residues in poly-Si film increase the leakage current and shift the threshold voltage [4,5]. As is well known, the leakage current can be reduced by lowering the Ni concentration by employing certain technologies such as the gettering method [6], metal-induced crystallization through a cap layer (MICC) [7], and ultra-thin Ni films by atomic layer deposition [8].

Whereas most studies have focused only on reducing Ni contamination to improve the leakage current, lowering the Ni concentration may change the source/drain (S/D) series resistance of MIC–TFTs. Inevitably, the S/D series resistance negatively influences the device performance, especially the on-state current and mobility [9–14]. This phenomenon is a serious issue because of the increased ratio of the S/D series resistance of short-channel devices. Therefore, improving the performance of MIC–TFTs requires a detailed understanding of how the Ni concentration affects S/D series resistance. However, exactly how Ni concentration and series resistance are related at the S/D region has not been examined.

In this study, the S/D series resistance of MIC–TFTs was extracted using the transmission line method [9]. The S/D resistance included contact resistance, sheet resistance, and S/D parasitic resistance. Exactly how Ni concentration affects the S/D series resistance of MIC–TFTs is also examined using the conventional MIC and MICC to represent high and low Ni concentration devices, respectively. The cap layer was formed using chemical oxide (CF–MIC), which is simpler and more economical than plasma-enhanced chemical vapor deposition (PECVD) SiN_x. The study results demonstrate that the S/D series resistance and channel resistance decreased with the reduction of Ni concentration in MIC poly-Si.

2. Experimental details

This study investigated N-channel poly-Si TFTs. A 100-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by employing a low-pressure chemical vapor deposition (LPCVD) system using SiH_4 as the precursor gas at 550 °C. To form chemical oxide filter MIC poly-Si films (CF–MIC), the samples were dipped into a mixed solution of H_2SO_4 and H_2O_2 for 20 min to form a chemical oxide filter layer on top of α-Si. A 5-nm-thick Ni film was then deposited

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onto the chemical oxide/α-Si by using an e-gun evaporator, as shown in Fig. 1(a). For nickel-induced crystallization of α-Si, the heat treatment of the sample was performed at 500 °C for 1 h in a N_2 atmosphere, which is referred from the MILC growth rate (1 μm/h at 500 °C) [15]. Moreover, annealing at 500 °C for 1 h can ensure full crystallization of a-Si. The unreacted Ni film and chemical oxide layer were then removed by wet etching, as shown in Fig. 1(b). The cross-sectional image of the chemical oxide layer, shown in Fig. 1(c), was obtained by field-emission transmission electron microscopy (FE-TEM, Jem-2100F, Jeol) operated at 200 keV. Preparation of the TEM sample was polished using a grinder and then damaged using ion-beam milling in the precision ion polishing system.

TFT devices were fabricated using standard IC processes. The islands of poly-Si regions on the wafers were defined by reactive ion etching using CF_4- and SF_6-reactive gases (manufactured by SAMCO, Japan; type: RIE-10N). After the cleaning process, a 100-nm-thick tetraethyl orthosilicate/O_2 oxide layer was deposited as the gate insulator at 350 °C by PECVD. Thereafter, a 100-nm-thick poly-Si film was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned 35 keV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form the S/D and gate. Dopant activation was performed at 600 °C for 24 h, followed by deposition of the passivation layer and a definition of contact holes. A 500-nm-thick Al layer was then deposited by thermal evaporation, and patterned as the electrode. Finally, the sintering process was performed at 400 °C for 30 min in a N_2 ambient. The final TFT device is shown in Fig. 1(d).

After fabrication of the device, the transfer characteristics of the TFTs were measured at room temperature by using a KEITHLEY 4200 semiconductor parameter analyzer. The S/D series resistance of the TFTs was extracted using the transmission line method [9]. For comparison, a conventional MIC TFT without a chemical oxide layer was also fabricated and measured. The TLM method is generally used to determine the series resistance to conducting materials. However, in this work, the TLM test structure was employed to measure the series resistance of a top-gate TFT device used to induce electrons into the channel. The extraction of S/D series resistance in these gated structures differs slightly from that of the conventional TLM method because the measurement is performed at various gate voltages.

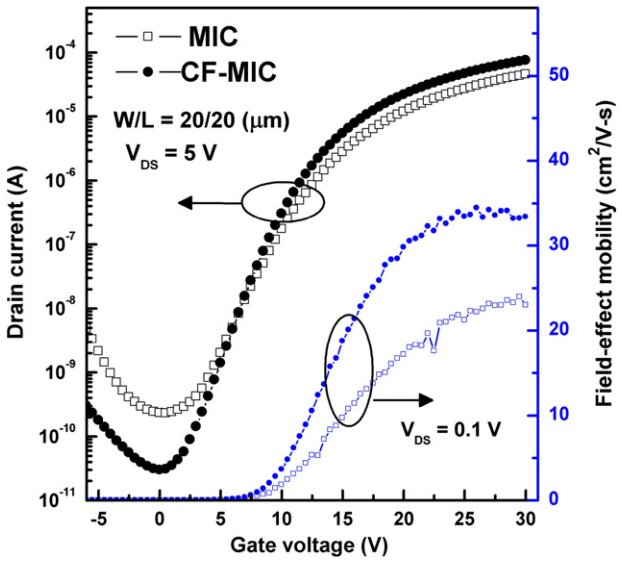

Fig. 2. Typical I_D–V_G transfer characteristics and filed-effect mobility of conventional MIC and CF–MIC (W/L = 20/20 μm).

3. Results and discussion

Fig. 2 shows the drain-current versus gate-voltage (I_D–V_G) transfer characteristics and field-effect mobility (μ_{FE}) of MIC and CF–MIC TFT devices. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_{DS} = 0.1 V. The TFT channel length and width were 20 μm and 20 μm respectively. According to this figure, CF–MIC TFTs have excellent electrical characteristics, especially low off-state leakage current and high field-effect mobility. The leakage current improvement was attributed to the reduction of Ni concentration in the CF–MIC films. This improvement is due to Ni residues (Ni-related defects) in the poly-Si film serving as deep-level traps to promote the thermionic emission-dominated leakage current in the off-state region [16–18]. In addition, the Ni concentrations in poly-Si films were

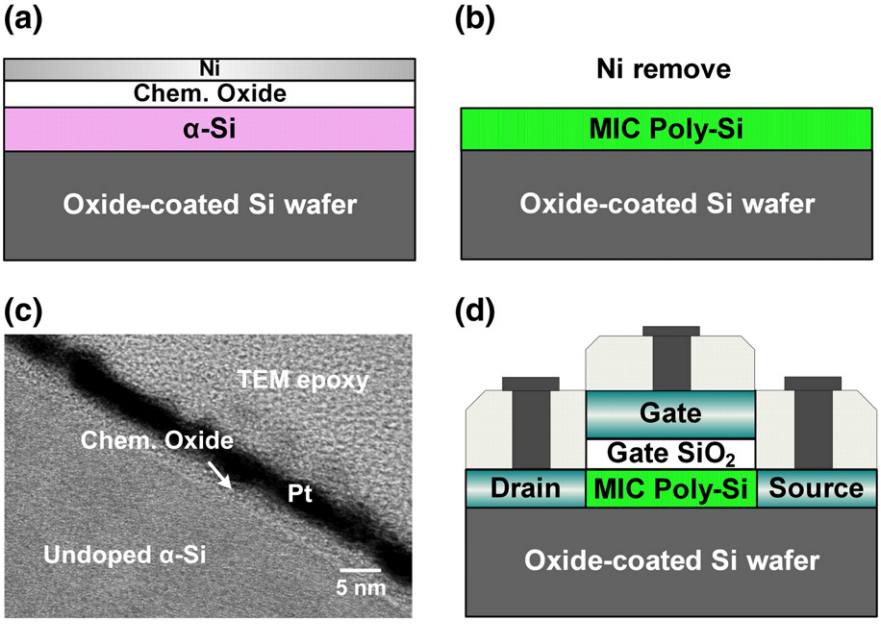

Fig. 1. Schematic illustration of CF–MIC TFT process: (a) the chemical oxide layer between α-Si layer and Ni layer, (b) removing of remained Ni film and chemical oxide, (c) typical structure of top-gate TFT device, and (d) TEM image of chemical oxide layer.

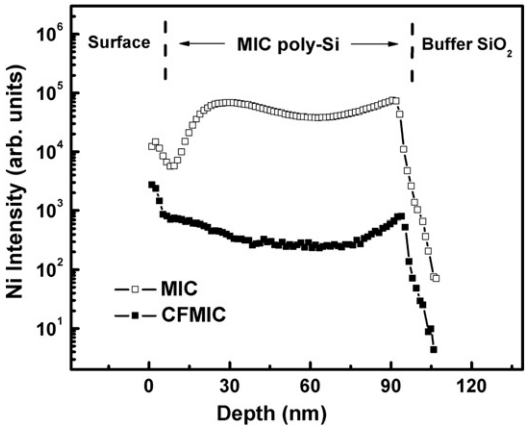

Fig. 3. SIMS depth profiles of nickel and in the structure of poly-Si film after MIC process.

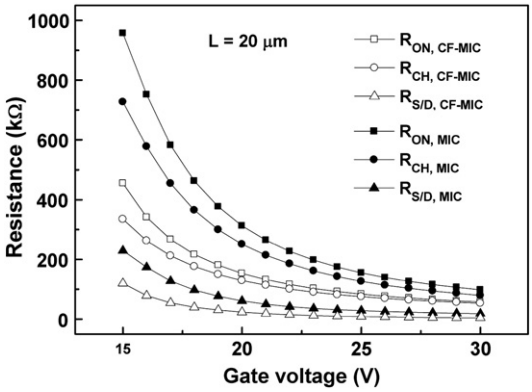

Fig. 5. The extracted S/D series resistance and channel resistance as a function of the gate voltage (W/L = 20/20 μm).

analyzed using the secondary-ion mass spectroscopy (SIMS) depth profile (SIMS, IMS-7F, CAMECA) operated at 5 keV of accumulated energy with oxygen primary ions and detected Ni ions per depth of 0.15 nm. As shown in Fig. 3, the Ni concentration was reduced by two orders of magnitude in the CF–MIC over that of conventional MIC poly-Si because the chemical oxide layer reduced the content of Ni atoms into the channel layer during the MIC annealing process. With the reduction of the Ni concentration, the minimum leakage current decreased, and therefore, the on/off current ratio increased [6]. Moreover, the field-effect mobility also increased from 23.5 to 32.3 $cm^2\ V^{-1}\ s^{-1}$ because of lower impurity scattering of Ni-related defects and better crystallinity of CF-MIC poly-Si film.

In addition to basic transfer characteristics, the other important issue of MIC–TFTs is the S/D series resistance, which might be changed with Ni concentration. The transmission line method was employed to investigate the S/D series resistance ($R_{S/D}$), which is a standard approach for the extraction of $R_{S/D}$ by fitting the ON-resistance (R_{ON}) as a function of the channel length. In the linear region of the TFT output characteristics (low drain voltage and high gate voltage), R_{ON} is assumed to consist of channel resistance (R_{CH}) and $R_{S/D}$. The ON-resistance can be estimated using the following equations:

$$R_{ON} = (\partial V_D/\partial I_D) = R_{CH} + R_{S/D} \quad (1)$$

$$R_{CH} = L/[W\mu_o C_i(V_G - V_t)] \quad (2)$$

where C_i is the gate oxide capacitance per unit area; μ_o is the intrinsic carrier mobility without an S/D resistance effect; and W, L, and V_t are the device channel width, length, and the intrinsic threshold voltage, respectively.

Fig. 4 shows the ON-resistance data of MIC TFTs and CF–MIC TFTs as a function of the channel length. The ON-resistance of TFTs was evaluated at $V_D = 0.1$ V of the TFT output characteristics. The transistors have a fixed channel width of 20 μm. The results showed that the ON-resistance increased with the device channel length; a large ON-resistance in the high Ni concentration device (MIC TFT) was also observed. By linear fitting for different gate voltages, the interception with the y-axis indicated the S/D series resistance of TFTs. Fig. 5 shows the extracted S/D series resistance and channel resistance as a function of the gate voltage. Consequently, the S/D series resistance and channel resistance of the CF–MIC TFT were lower than those of the conventional MIC TFT. In the S/D region, the device with a high Ni concentration (MIC TFT) exhibited a larger S/D series resistance than that of CF–MIC TFT. The S/D series resistance can be affected by the crystalline quality and dopant concentration in the S/D region. First, regarding crystalline quality, samples were annealed at 600 °C for dopant activation and recrystallization after ion implantation because the poly-Si in the S/D region was amorphized by a heavily doped implantation at a dosage of $5\times10^{15}\ cm^{-2}$ [19]. Fig. 6 shows the Raman spectra of undoped and heavily doped poly-Si films after dopant activation at 600 °C for 24 h. This figure shows a poly-Si peak at 520 cm^{-1}. In contrast, no a-Si peak appears at 480 cm^{-1}, indicating that all samples are transferred to the polycrystalline structure. The heavily doped poly-Si films show a lower Raman spectral intensity because recrystallization of a-Si with Ni at 600 °C is not oriented, and growth is limited by the formation of solid-state crystallization (SPC), subsequently lowering crystallinity in the S/D region. Furthermore, the crystallinity of "CF–MIC + SPC" is superior to that of "MIC + SPC" because the lower number of nucleation sites of $NiSi_2$ causes a larger grain size in CF–MIC poly-Si films with a low Ni concentration [20]. However, the crystallinity of the S/D region is

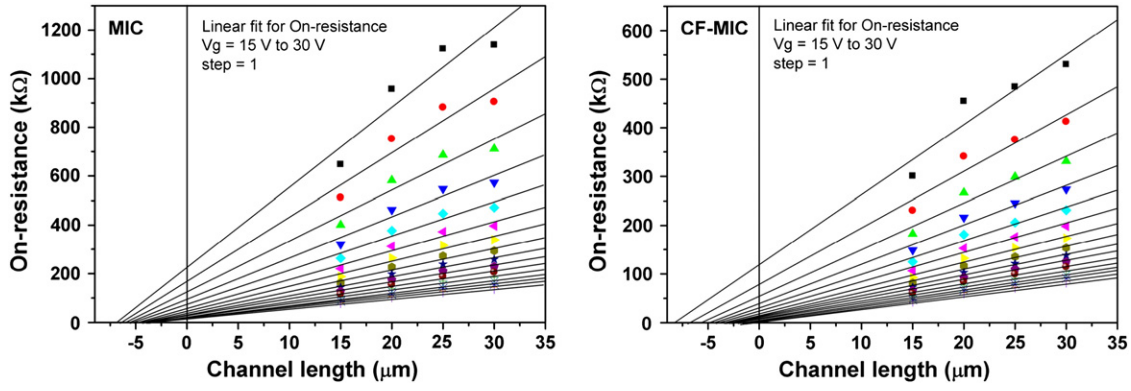

Fig. 4. Measured on-resistance of conventional MIC TFT and CF–MIC TFT as a function of channel length. The transistors have a channel width of 20 μm.

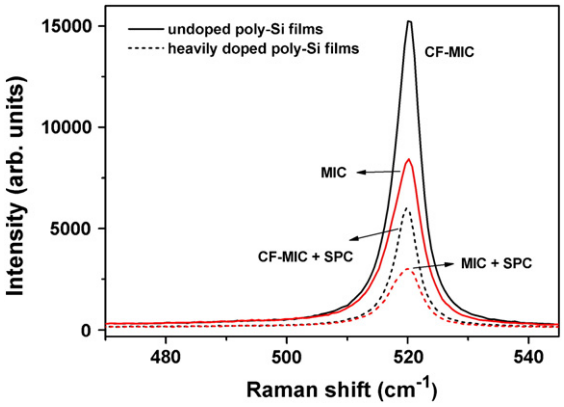

Fig. 6. Raman spectra of undoped and heavily doped MIC poly-Si films after dopant activation at 600 °C for 24 h.

not different in a general recrystallization without Ni because of the only SPC mechanism. Second, the variation in S/D series resistance can also be attributed to the dopant concentration. As is well known, heavily doped implantation can significantly reduce the resistance of Si films. However, Ni atoms serve as acceptor-like dopants in silicon [21], which counteract the effects of phosphorous doping and ultimately reduce the donor concentration in the S/D region. Hall measurements showed that the carrier concentration decreased from 2.518×10^{15} to 8.594×10^{14} cm^{-2}, and that the sheet resistance increased from 205.7 to 261.9 Ω/cm^2 with increased Ni contents. Therefore, a high Ni concentration reduces the conductivity of the S/D region, leading to a large S/D series resistance in MIC–TFTs. As mentioned, CF–MIC has a lower S/D series resistance than that of MIC because of a lower Ni concentration.

Moreover, in the channel region, the MIC TFT also shows a larger channel resistance (R_{CH}) because of the high trap-state density and impurity scattering (Ni-related defects). According to Fig. 6, CF–MIC presents a crystalline quality superior to that of MIC at the channel region. The effective trap-state density (N_t) uses the Levinson and Proano method, which can estimate N_t from the slope of the linear segment of $\ln[I_D/(V_G-V_{FB})]$ vs. $1/(V_G-V_{FB})^2$ at a low V_D and high V_G, where V_{FB} is defined as the gate voltage that yields the minimum drain current at $V_D=0.1$ V [22,23]. The N_t of the CF–MIC TFT is 4.65×10^{12} cm^{-2}, which is smaller than that of the MIC TFT (6.08×10^{12} cm^{-2}). These results imply that the defects are minimized in the CF–MIC TFT because of the reduced Ni concentration. As mentioned, the Ni atoms are obstructers of performance and S/D conductivity of the MIC–TFTs. These results confirmed that it is an efficient means to improve the electrical characteristics of a channel and S/D region by reducing the Ni concentration in MIC–TFTs.

4. Conclusion

This study investigated how Ni concentration affects S/D series resistance by using the transmission line method. For comparison, high and low Ni concentration devices were formed using MIC–TFTs with and without a chemical oxide layer, respectively. This finding provides further insight into how the Ni concentration and resistance of MIC–TFTs are related. Consequently, the channel resistance and S/D series resistance decreased with the reduction of the Ni concentration in MIC poly-Si because of improved crystalline quality and a lower degradation of the donor concentration. This phenomenon was caused by the low Ni concentration forming less $NiSi_2$ nucleation sites, resulting in a large grain size; Ni atoms serve as acceptor-like dopants in silicon, which counteract the effects of n-type doping, subsequently reducing the donor concentration in the S/D region. In brief, the results of this study demonstrate that the Ni residues obstruct the performance and S/D conductivity of MIC–TFTs.

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References

[1] M. Stewart, R.S. Howell, L. Pires, M.K. Hatalis, IEEE Trans. Electron Devices 48 (2001) 845.
[2] L. Pereira, H. Aguas, R.M.S. Martins, P. Vilarinho, E. Fortunato, R. Martins, Thin Solid Films 451–452 (2004) 334.
[3] J.F. Li, X.W. Sun, M.B. Yu, G.J. Qi, X.T. Zeng, Appl. Surf. Sci. 240 (2005) 155.
[4] D. Murley, N. Young, M. Trainor, D. McCulloch, IEEE Trans. Electron Devices 48 (2001) 1145.
[5] G.A. Bhat, H.S. Kwok, M. Wong, Solid State Electron. 44 (2000) 1321.
[6] C.M. Hu, Y.C. Sermon Wu, C.C. Lin, IEEE Electron Device Lett. 28 (2007) 1000.
[7] W.S. Sohn, J.H. Choi, K.H. Kim, J.H. Oh, S.S. Kim, J. Jang, J. Appl. Phys. 94 (2003) 4326.
[8] B.S. Lim, A. Rahtu, R.G. Gordon, Nat. Mater. 2 (2003) 749.
[9] K. Chan, E. Bunte, D. Knipp, H. Stiebig, Semicond. Sci. Technol. 22 (2007) 1213.
[10] S. Luan, G.W. Neudeck, J. Appl. Phys. 72 (1992) 766.
[11] C.Y. Chen, J. Kanicki, Solid-State Electron. 42 (1998) 705.
[12] Z. Tang, M.S. Park, S.H. Jin, C.R. Wie, IEEE Trans. Electron Devices 57 (2010) 1093.
[13] J.S. Lee, S. Chang, H. Bouzid, S.M. Koo, S.Y. Lee, Phys. Status Solidi A 207 (2010) 1694.
[14] S. Chung, J. Jeong, D. Kim, Y. Park, C. Lee, Y. Hong, J. Disp. Technol. 8 (2012) 48.
[15] M. Qin, M.C. Poon, L.J. Fan, M. Chan, C.Y. Yuen, W.Y. Chan, Thin Solid Films 406 (2002) 17.
[16] K.R. Olasupo, M.K. Hatalis, IEEE Trans. Electron Devices 43 (1996) 1218.
[17] C.P. Chang, Y.C. Sermon Wu, IEEE Electron Device Lett. 30 (2009) 130.
[18] M. Yazaki, S. Takenaka, H. Ohshima, Jpn. J. Appl. Phys. 31 (1992) 206.
[19] W.P. Maszara, G.A. Rozonyi, J. Appl. Phys. 60 (1986) 2310.
[20] M.H. Lai, Y.C. Sermon Wu, C.P. Chang, Mater. Chem. Phys. 126 (2011) 69.
[21] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, 3rd edition, (2007) p. 23.
[22] J. Levinson, G. Este, M. Rider, P.J. Scanlon, F.R. Shepherd, W.D. Westwood, J. Appl. Phys. 53 (1982) 1193.
[23] R.E. Proano, R.S. Misage, D.G. Ast, IEEE Trans. Electron Devices 36 (1989) 1915.